## FUNCTIONAL DESCRIPTION

The XRK4991 is a 3.3V High-Speed Low-Voltage Programmable Skew Clock Buffer. It is intended for high-performance computer systems and offers user selectable control over system clock functions to optimize timing. Eight outputs, arranged in four banks, can each drive 50Ω terminated transmission lines while delivering minimal and specified output skews and full-swing Low Voltage TTL logic levels.

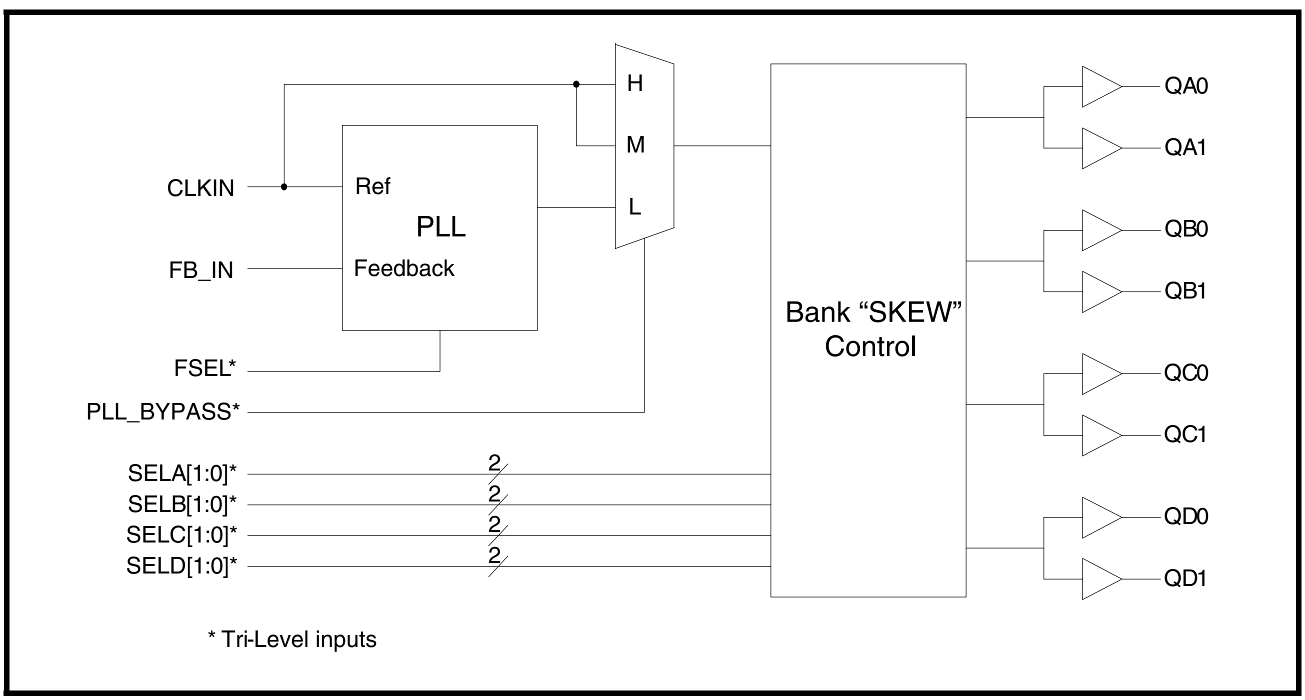
Each bank (two outputs per bank) can be individually selected for one of nine delay or function configurations through two dedicated tri-level inputs. These outputs are able to lead or lag the CLKIN input reference clock by up to 6 time units from their nominal "zero" skew position. The integrated PLL allows external load and transmission line delay effects to be canceled achieving zero delay capability. Combining the zero delay capability with the selectable output skew functions, output-to-output delays of up to ±12 time units can be created.

The XRK4991's divide functions (divide-by-two and divide-by-four) allow distribution of a low-frequency clock that can be multiplied by two or four at the clock destination. This feature facilitates clock distribution while allowing maximum system clock flexibility.

### FEATURES

- 3.75- to 85-MHz output operation
- All output pair skew <100 ps typical
- Three skew grades
  - -2 : $t_{SKEW0}$<250ps
  - -5 : $t_{SKEW0}$<500ps
  - -7 : $t_{SKEW0}$<700ps
- Selectable output functions
  - Skew adjustments of +/- 6$t_U$ (up to 18 ns)
  - Inverted and non-inverted
  - Operation at 1/2 and 1/4 input frequency
  - Operation at 2x and 4x input frequency
- Cycle-Cycle Jitter
  - < 25 ps (rms)
  - < 200 ps (pk-pk)
- Zero input-to-output delay
- 50% duty-cycle outputs
- LVTTL outputs drive 50Ω terminated lines
- Operates from a single 3.3V supply
- 32-pin PLCC package
- Green packaging
- Lead free lead frame available

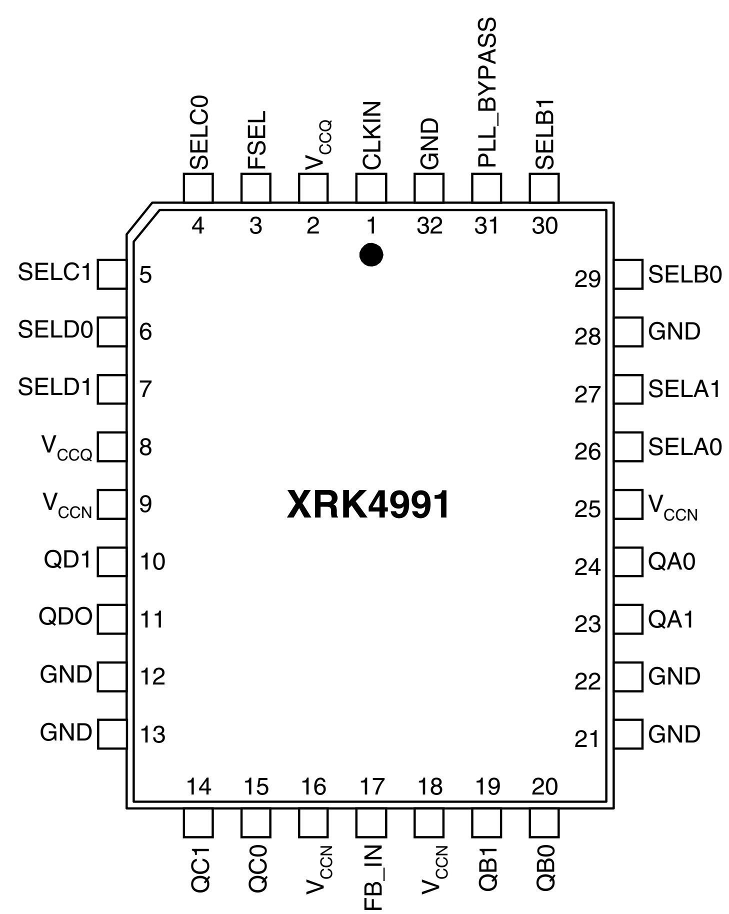
FIGURE 1. BLOCK DIAGRAM OF THE XRK4991



## PRODUCT ORDERING INFORMATION

| PRODUCT NUMBER | ACCURACY | TEMPERATURE RANGE | LEAD FREE |
|---|---|---|---|
| XRK4991IJ-2 | 250 ps | -40°C to +85°C | |
| XRK4991CJ-2 | 250 ps | 0°C to +70°C | |
| XRK4991IJ-2F | 250 ps | -40°C to +85°C | √ |
| XRK4991CJ-2F | 250 ps | 0°C to +70°C | √ |
| XRK4991IJ-5 | 500 ps | -40°C to +85°C | |
| XRK4991CJ-5 | 500 ps | 0°C to +70°C | |
| XRK4991CJ-7 | 750 ps | 0°C to +70°C | |
| XRK4991IJ-5F | 500 ps | -40°C to +85°C | √ |
| XRK4991CJ-5F | 500 ps | 0°C to +70°C | √ |
| XRK4991CJ-7F | 750 ps | 0°C to +70°C | √ |

**FIGURE 2. PIN OUT OF THE XRK4991**



## PIN DESCRIPTIONS

| PIN NAME | PIN # | TYPE | DESCRIPTION |
|---|---|---|---|
| CLKIN | 1 | I | Reference clock input. |
| FB_IN | 17 | I | PLL's feedback input. (Normally connected to one of the eight outputs) |
| FSEL | 3 | I | Tri-level frequency range select. See Table 1 |
| PLL_BYPASS | 31 | I | Tri-level select. See PLL_BYPASS section. |
| SELA0<br>SELA1 | 26<br>27 | I | Tri-level select inputs for Bank A outputs (QA0, QA1). See Table 2. |
| SELB0<br>SELB1 | 29<br>30 | I | Tri-level select inputs for Bank B outputs (QB0, QB1). See Table 2. |
| SELC0<br>SELC1 | 4<br>5 | I | Tri-level select inputs for Bank C outputs (QC0, QC1). See Table 2. |
| SELD0<br>SELD1 | 6<br>7 | I | Tri-level select inputs for Bank D outputs (QD0, QD1). See Table 2. |
| QA0<br>QA1 | 24<br>23 | O | Bank A output pair. See Table 2. |
| QB0<br>QB1 | 20<br>19 | O | Bank B output pair. See Table 2. |
| QC0<br>QC1 | 15<br>14 | O | Bank C output pair. See Table 2. |
| QD0<br>QD1 | 11<br>10 | O | Bank D output pair. See Table 2. |
| $V_{CCN}$ | 9<br>16<br>18<br>25 | PWR | Power supply for output drivers. |
| $V_{CCQ}$ | 2<br>8 | PWR | Power supply for internal circuitry. |
| GND | 12<br>13<br>21<br>22<br>28<br>32 | PWR | Ground. |

**TABLE 1: FREQUENCY RANGE SELECT AND $t_U$ CALCULATION [1]**

| FSEL[2] | $f_{NOM}$ (MHz) MIN | $f_{NOM}$ (MHz) MAX | $t_U = 1 / (f_{NOM} \times N)$ WHERE N = | APPROXIMATE FREQUENCY (MHZ) AT WHICH $t_U$ = 1.0ns |
|---|---|---|---|---|
| LOW | 15 | 30 | 44 | 22.7 |
| MID | 25 | 50 | 26 | 38.5 |
| HIGH[3] | 40 | 85 | 16 | 62.5 |

### SKEW SELECT CONTROL

The skew select control consists of four independent banks. Each bank has two low-skew, high-fanout drivers (Qx0, Qx1), and two corresponding tri-level function select (SELx0, SELx1) inputs. The nine possible output states for each bank are shown in Table 2 as determined by each bank's select inputs. All timing measurements are made with respect to the CLKIN input with the output connected to the FB_IN input configured for 0 $t_U$ operation.

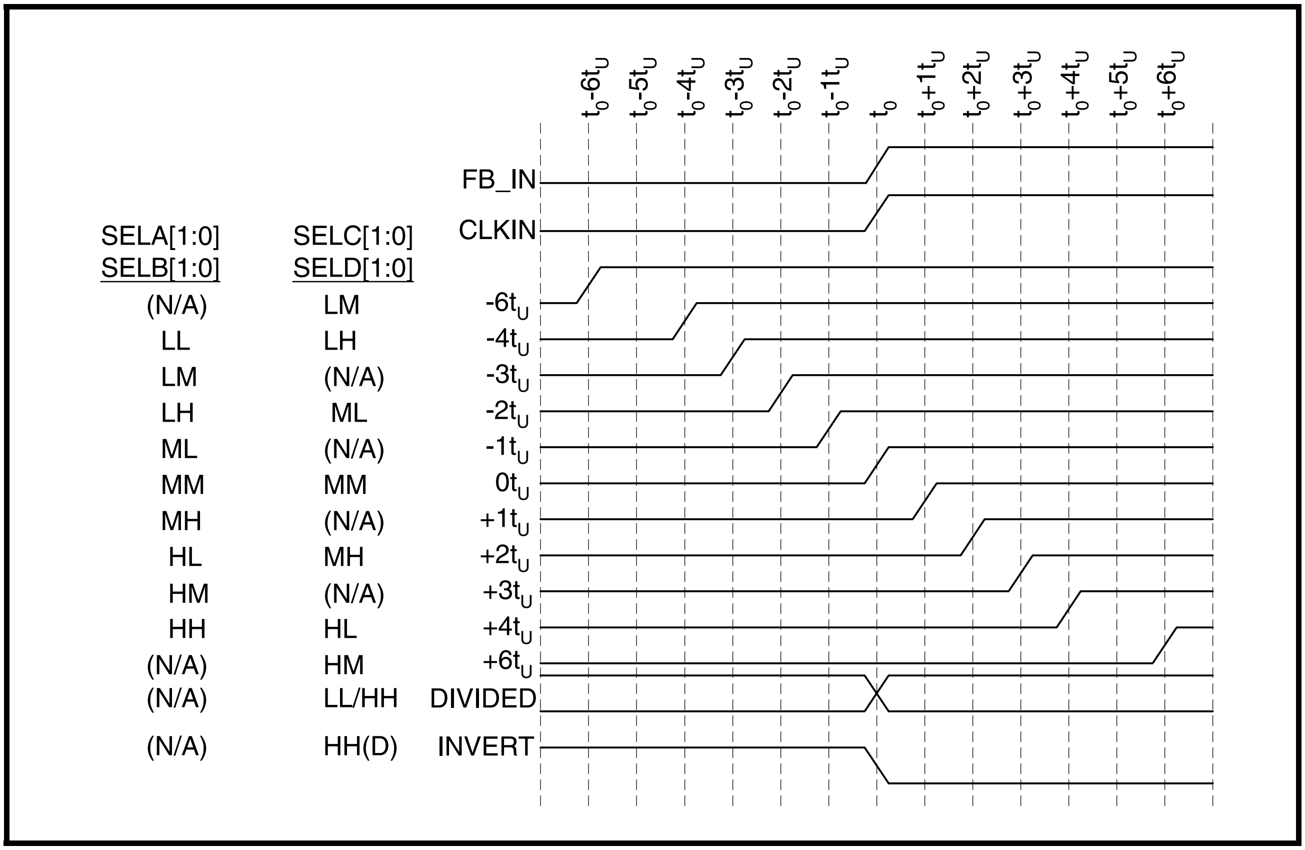
**TABLE 2: PROGRAMMABLE SKEW CONFIGURATIONS [1]**

| FUNCTION SELECT INPUTS | | OUTPUT FUNCTIONS | | |
|---|---|---|---|---|
| SELx1 | SELx0 | QA[1:0], QB[1:0] | QC[1:0] | QD[1:0] |
| LOW | LOW | $-4t_U$ | ÷ 2 | ÷ 2 |
| LOW | MID | $-3t_U$ | $-6t_U$ | $-6t_U$ |
| LOW | HIGH | $-2t_U$ | $-4t_U$ | $-4t_U$ |
| MID | LOW | $-1t_U$ | $-2t_U$ | $-2t_U$ |
| MID | MID | $0t_U$ | $0t_U$ | $0t_U$ |
| MID | HIGH | $+1t_U$ | $+2t_U$ | $+2t_U$ |
| HIGH | LOW | $+2t_U$ | $+4t_U$ | $+4t_U$ |
| HIGH | MID | $+3t_U$ | $+6t_U$ | $+6t_U$ |
| HIGH | HIGH | $+4t_U$ | ÷ 4 | Inverted |

***NOTES:***

1. *For all tri-level (three-state) inputs, HIGH indicates a connection to $V_{CC}$, LOW indicates a connection to GND, and MID indicates an open connection. Internal termination circuitry holds an unconnected input to $V_{CC}/2$.*
2. *The level to be set on FSEL is determined by the "normal" operating frequency ($f_{NOM}$) of the PLL. Nominal frequency ($f_{NOM}$) always appears at QA0 and the other outputs when they are operated in their undivided modes (see Table 2). The frequency appearing at the CLKIN and FB_IN inputs will be $f_{NOM}$ when the output connected to FB_IN is undivided. The frequency of the CLKIN and FB_IN inputs will be $f_{NOM} \div 2$ or $f_{NOM} \div 4$ when the part is configured for a frequency multiplication.*
3. *When the FSEL pin is selected HIGH, the CLKIN input must not transition upon power-up until $V_{CC}$ has reached 2.8V.*

FIGURE 3. TYPICAL OUTPUTS WITH FB_IN CONNECTED TO A ZERO-SKEW OUTPUT




### *PLL_BYPASS*

The PLL_BYPASS input is a tri-level input. In normal system operation, this pin is connected to ground.

In normal operation (tied LOW) all outputs will function based only on the connection of their own function select inputs (SELx[1:0]) and the waveform characteristics of the PLL.

If the PLL_BYPASS input is forced to its MID or HIGH state the device will operate in PLL bypass mode, with the phase locked loop disconnected, and CLKIN waveforms will directly control all outputs. Relative output to output timing is controlled by the SELx[1:0], the same as in normal mode.

# ELECTRICAL SPECIFICATIONS

## *ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---|
| Storage Temperature | –65°C to +150°C |
| Ambient Temperature with Power Applied | –55°C to +125°C |
| Supply Voltage to Ground Potential | –0.5V to +7.0V |
| DC Input Voltage | –0.5V to +7.0V |
| Output Current into Outputs (LOW) | 64 mA |
| Static Discharge Voltage (per MIL-STD-883, Method 3015) | >3000V |
| Latch-Up Current. | >200 mA |

## *OPERATING RANGE*

| RANGE | AMBIENT TEMPERATURE | VCC |
|---|---|---|
| Industrial | -40°C to +85°C | 3.3 ± 10% |
| Commercial | 0°C to +70°C | 3.3 ± 10% |

## ***ELECTRICAL CHARACTERISTICS*** *OVER THE 3.3V ± 10% OPERATING RANGE*

| SYMBOL | DESCRIPTION | MIN | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.4 | | V | $V_{CC}$ = Min., $I_{OH}$ = -18mA |
| $V_{OL}$ | Output LOW Voltage | | 0.45 | V | $V_{CC}$ = Min., $I_{OL}$ = 35mA |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | $V_{CC}$ | V | (CLKIN and FB_IN inputs only) |
| $V_{IL}$ | Input LOW Voltage | -0.5 | 0.8 | V | |
| $V_{IHH}$ | tri-level Input HIGH Voltage (FSEL, SELx[1:0], Test) [4] | 0.87*$V_{CC}$ | $V_{CC}$ | V | Min. ≤ $V_{CC}$ ≤ Max. |
| $V_{IMM}$ | tri-level Input MID Voltage (FSEL, SELx[1:0], Test) [4] | 0.47*$V_{CC}$ | 0.53 * $V_{CC}$ | V | Min. ≤ $V_{CC}$ ≤ Max. |
| $V_{ILL}$ | tri-level Input LOW Voltage (FSEL, SELx[1:0], Test) [4] | 0.0 | 0.13 * $V_{CC}$ | V | Min. ≤ $V_{CC}$ ≤ Max. |
| $I_{IH}$ | Input HIGH Leakage Current (CLKIN and FB_IN inputs only) | | 20 | µA | $V_{CC}$ = Max., $V_{IN}$ = Max. |
| $I_{IL}$ | Input LOW Leakage Current (CLKIN and FB_IN inputs only) | -20 | | µA | $V_{CC}$ = Max., $V_{IN}$ = 0.4V |
| $I_{IHH}$ | Input HIGH Current (FSEL, SELx[1:0], Test) | | 200 | µA | $V_{IN}$ = $V_{CC}$ |
| $I_{IMM}$ | Input MID Current (FSEL, SELx[1:0], Test) | -50 | 50 | µA | $V_{IN}$ = $V_{CC}$/2 |
| $I_{ILL}$ | Input LOW Current (FSEL, SELx[1:0], Test) | | -200 | µA | $V_{IN}$ = GND |

***ELECTRICAL CHARACTERISTICS*** *OVER THE 3.3V ± 10% OPERATING RANGE*

| SYMBOL | DESCRIPTION | | MIN | MAX | UNIT | CONDITION |
|---|---|---|---|---|---|---|
| $I_{OS}$ | Short Circuit Current [5] | | | -200 | mA | $V_{CC}$ = Max,<br>$V_{OUT}$ = GND (25° only) |
| $I_{CCQ}$ | Operating Current Used by Internal Circuitry | Com'l | | 95 | mA | $V_{CCN} = V_{CCQ}$ = Max.,<br>All Inputs Selects Open |
| | | Ind | | 100 | | |
| $I_{CCN}$ | Output Buffer Current per Output Pair [6] | | | 19 | mA | $V_{CCN} = V_{CCQ}$ = Max.,<br>$I_{OUT}$ = 0 mA<br>Inputs Selects Open, $f_{MAX}$ |
| PD | Power Dissipation per Output Pair [7] | | | 104 | mW | $V_{CCN} = V_{CCQ}$ = Max.,<br>$I_{OUT}$ = 0 mA<br>Input Selects Open, $f_{MAX}$ |

***CAPACITANCE***[8]

| SYMBOL | DESCRIPTION | MAX. | UNIT | CONDITION |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 10 | pF | $T_A$ = 25°C,<br>f=1MHz, $V_{CC}$=3.3V |

***NOTES:***

4. *These inputs are normally wired to $V_{CC}$, GND or left unconnected (actual threshold voltages vary as a percentage of $V_{CC}$). Internal termination resistors hold unconnected inputs at $V_{CC}/2$. If these inputs are switched, the function and timing of the outputs may glitch and the PLL may require an additional $t_{LOCK}$ time before all data sheet limits are achieved.*
5. *XRK4991 should be tested one output at a time, output shorted for less than one second, less than 10% duty cycle. Room temperature only.*
6. *Total output current per output pair can be approximated by the following expression that includes device current plus load current:*

   *XRK4991: $I_{CCN} = \{(4+0.11F) + [(835-3F)/Z + (.0022FC)]N\} \times 1.1$*

   *Where:*

   *F = frequency in MHz*

   *C = capacitive load in pF*

   *Z = line impedance in ohms*

   *N = number of loaded outputs; 0, 1, or 2*
7. *Total power dissipation per output pair can be approximated by the following expression that includes device power dissipation plus power dissipation due to the load circuit:*

   *$PD = \{(22 + 0.61F) + [(1550 + 2.7F)/Z) + .0125FC]N\} \times 1.1$*

   *See note 6 for variable definition.*
8. *Applies to CLKIN and FB_IN inputs only.*

**FIGURE 4. AC TEST LOAD**

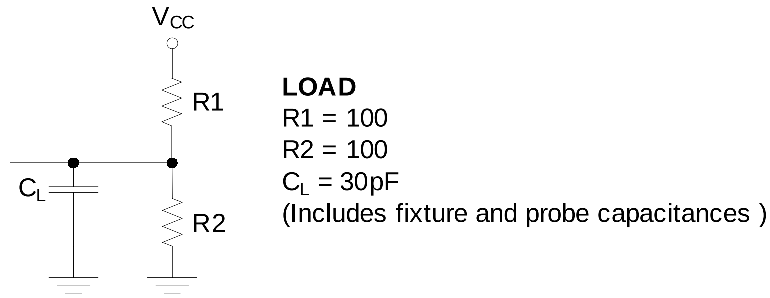
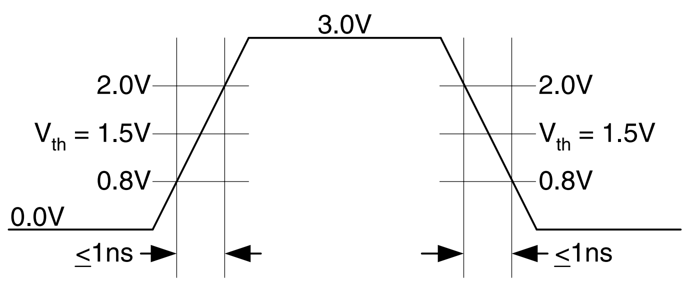



**FIGURE 5. INPUT TEST WAVEFORM**




### ***SWITCHING CHARACTERISTICS*** *OVER THE OPERATING RANGE [2,9]*

| SYMBOL | DESCRIPTION | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{NOM}$ | Operating Clock Frequency in MHz | FSEL = LOW [1, 2] | 15 | 30 | MHz |
| | | FSEL = MID [1, 2] | 25 | 50 | |
| | | FSEL = HIGH [1, 2, 3] | 40 | 85 | |

***SWITCHING CHARACTERISTICS*** *OVER THE 3.3V ± 10% OPERATING RANGE [2,9]*

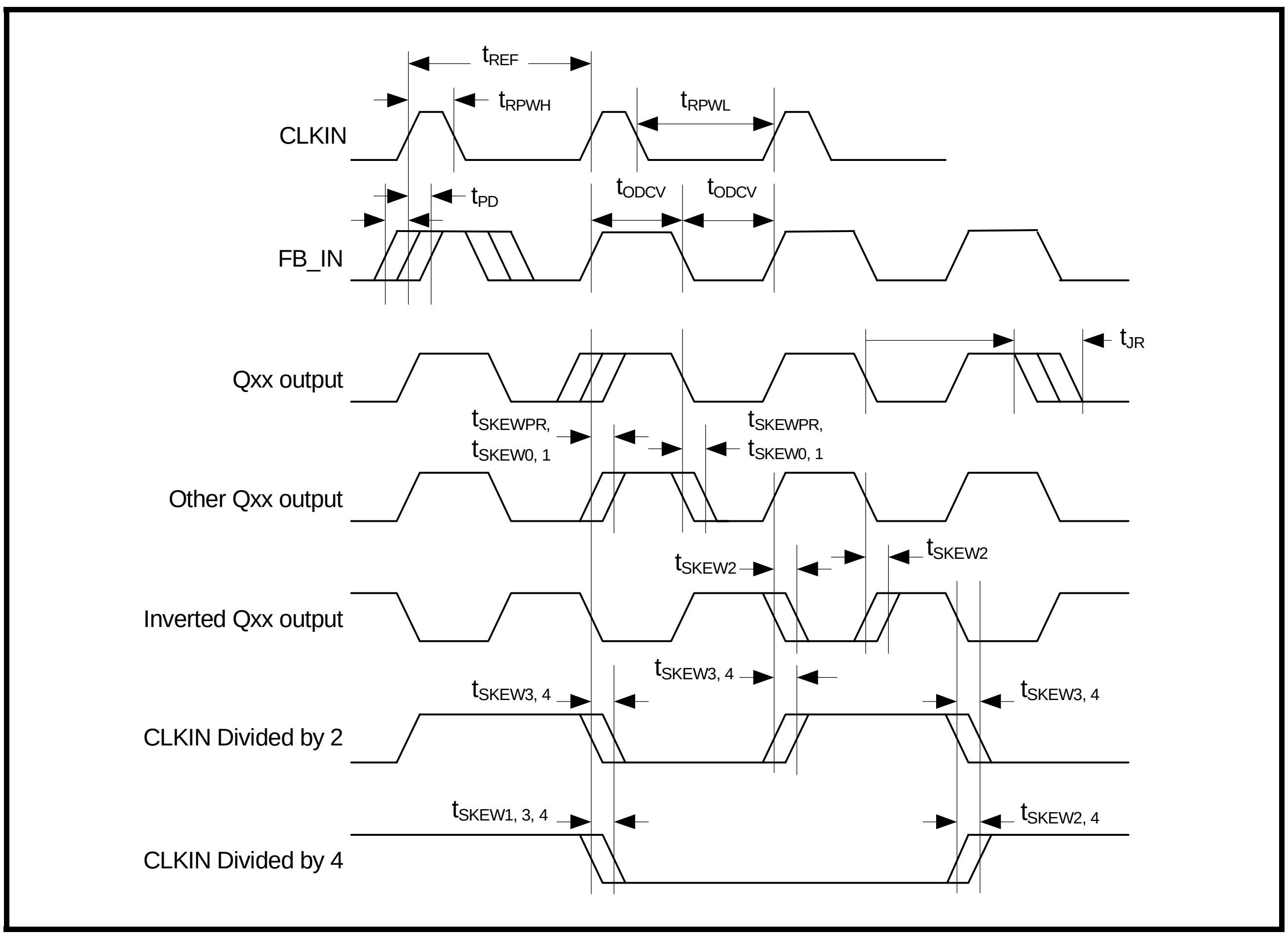
| SYMBOL | DESCRIPTION | | XRK4991-2 | | | XRK4991-5 | | | XRK4991-7 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{RPWH}$ | CLKIN Pulse Width HIGH | | 4 | | | 4 | | | 4 | | | ns |
| $t_{RPWL}$ | CLKIN Pulse Width LOW | | 4 | | | 4 | | | 4 | | | ns |
| $t_u$ | Programmable Skew Unit | | See Table 1 | | | | | | | | | |
| $t_{SKEWPR}$ | Zero Output Matched-Pair Skew (Qx[1:0]) [10, 11] | | | 0.05 | 0.2 | | 0.1 | 0.25 | | 0.1 | 0.25 | ns |
| $t_{SKEW0}$ | Zero Output Skew (All Outputs) [10, 12] | | | 0.1 | 0.25 | | 0.25 | 0.5 | | 0.3 | 0.75 | ns |
| $t_{SKEW1}$ | Output Skew (Rise-Rise, Fall-Fall, Same Class Outputs) [10, 13] | | | 0.25 | 0.5 | | 0.6 | 0.7 | | 0.6 | 1 | ns |
| $t_{SKEW2}$ | Output Skew (Rise-Fall, Nominal-Inverted, Divided-Divided) [10, 13] | | | 0.3 | 1 | | 0.5 | 1 | | 1 | 1.5 | ns |
| $t_{SKEW3}$ | Output Skew (Rise-Rise, Fall-Fall, Different Class Outputs) [10, 13] | | | 0.25 | 0.5 | | 0.5 | 0.7 | | 0.7 | 1.2 | ns |
| $t_{SKEW4}$ | Output Skew (Rise-Fall, Nominal-Divided, Divided-Inverted [10, 13] | | | 0.5 | 0.9 | | 0.5 | 1 | | 1.2 | 1.7 | ns |
| $t_{DEV}$ | Device-to-Device Skew [14, 15] | | | | 0.75 | | | 1.25 | | | 1.65 | ns |
| $t_{PD}$ | Propagation Delay, CLKIN Rise to FB_IN Rise | | -0.25 | 0 | 0.25 | -0.5 | 0 | 0.5 | -0.7 | 0 | 0.7 | ns |
| $t_{ODCV}$ | Output Duty Cycle Variation [16] | | -0.65 | 0 | 0.65 | -1 | 0 | 1 | -1.2 | 0 | 1.2 | ns |
| $t_{PWH}$ | Output HIGH Time Deviation from 50% [17] | | | | 2.0 | | | 2.5 | | | 3 | ns |
| $t_{PWL}$ | Output LOW Time Deviation from 50% [17] | | | | 1.5 | | | 3 | | | 3.5 | ns |
| $t_{ORISE}$ | Output Rise Time [17, 18] | | 0.15 | 1 | 1.2 | 0.15 | 1 | 1.5 | 0.15 | 1.5 | 2.5 | ns |
| $t_{OFALL}$ | Output Fall Time [17, 18] | | 0.15 | 1 | 1.2 | 0.15 | 1 | 1.5 | 0.15 | 1.5 | 2.5 | ns |
| $t_{LOCK}$ | PLL Lock Time [19] | | | | 0.5 | | | 0.5 | | | 0.5 | ms |
| $t_{JR}$ | Cycle-to-Cycle Output Jitter | RMS [14] | | | 25 | | | 25 | | | 25 | ps |
| | | Peak-to-Peak [14] | | | 200 | | | 200 | | | 200 | |

***NOTES:***

9. *Test measurement levels for the XRK4991 are TTL levels (1.5V to 1.5V). Test conditions assume signal transition times of 2 ns or less and output loading as shown in the AC Test Loads and Waveforms unless otherwise specified.*
10. *SKEW is defined as the time between the earliest and the latest output transition among all outputs for which the same $t_U$ delay has been selected when all are loaded with 30pF and terminated with 50Ω to $V_{CC}/2$ (XRK4991).*

11. *$t_{SKEWPR}$ is defined as the skew between a pair of outputs (Qx0 and Qx1) when all eight outputs are selected for $0t_U$.*
12. *$t_{SKEW0}$ is defined as the skew between outputs when they are selected for $0t_U$. Other outputs are divided or inverted but not shifted*
13. *There are three classes of outputs: Nominal (multiple of $t_U$ delay), Inverted (QD[1:0] only with SELD0 = SELD1 = HIGH), and Divided (QC[1:0] and QD[1:0] only in Divide-by-2 or Divide-by-4 mode).*
14. *Guaranteed by statistical correlation. Tested initially and after any design or process changes that may affect these parameters.*
15. *$t_{DEV}$ is the output-to-output skew between any two devices operating under the same conditions ($V_{CC}$ ambient temperature, air flow, etc.)*
16. *$t_{ODCV}$ is the deviation of the output from a 50% duty cycle. Output pulse width variations are included in $t_{SKEW2}$ and $t_{SKEW4}$ specifications.*
17. *Specified with outputs loaded with 30pF for the XRK4991-5 and -7 devices. Devices are terminated through 50Ω to $V_{CC}/2$. $t_{PWH}$ is measured at 2.0V. $t_{PWL}$ is measured at 0.8V.*
18. *$t_{ORISE}$ and $t_{OFALL}$ measured between 0.8V and 2.0V.*
19. *$t_{LOCK}$ is the time that is required before synchronization is achieved. This specification is valid only after $V_{CC}$ is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at CLKIN or FB_IN until $t_{PD}$ is within specified limits*

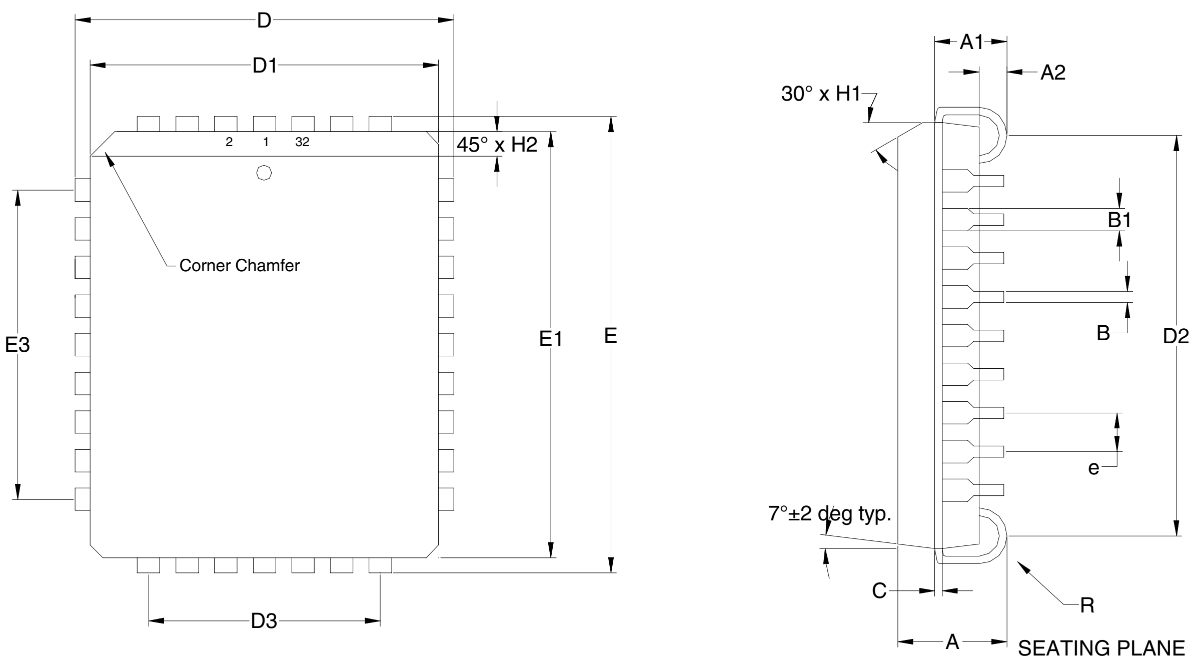
**FIGURE 6. AC TIMING DIAGRAMS**



# PACKAGE DIMENSIONS

## 32 LEAD PLASTIC LEADED CHIP CARRIER (PLCC)

***Rev. 1.00***




| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| **SYMBOL** | **MIN** | **MAX** | **MIN** | **MAX** |
| A | 0.120 | 0.140 | 3.05 | 3.56 |
| A1 | 0.075 | 0.095 | 1.91 | 2.41 |
| A2 | 0.020 | --- | 0.51 | --- |
| B | 0.013 | 0.021 | 0.33 | 0.53 |
| B1 | 0.026 | 0.032 | 0.66 | 0.81 |
| C | 0.008 | 0.013 | 0.19 | 0.32 |
| D | 0.485 | 0.495 | 12.33 | 12.58 |
| D1 | 0.448 | 0.454 | 11.39 | 11.54 |
| D2 | 0.400 | 0.440 | 10.17 | 11.18 |
| D3 | 0.300 typ. | | 7.62 typ. | |
| E | 0.585 | 0.595 | 14.87 | 15.11 |
| E1 | 0.545 | 0.557 | 13.85 | 14.15 |
| E2 | 0.500 | 0.540 | 12.71 | 13.72 |
| E3 | 0.400 typ. | | 10.16 typ. | |
| e | 0.050 BSC | | 1.27 BSC | |
| H1 | 0.023 | 0.029 | 0.58 | 0.74 |
| H2 | 0.042 | 0.048 | 1.07 | 1.22 |
| R | 0.025 | 0.045 | 0.64 | 1.14 |

*Note: The control dimension is in inches.*

## *REVISION HISTORY*

| REVISION # | DATE | DESCRIPTION |
|---|---|---|
| 1.0.0 | June 17, 2005 | Initial Release to Production |
| | | |
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Datasheet June 2005.