GD54/74LS109A

DUAL POSITIVE-EDGE-TRIGGERED J-$\overline{K}$ FLIP-FLOPS

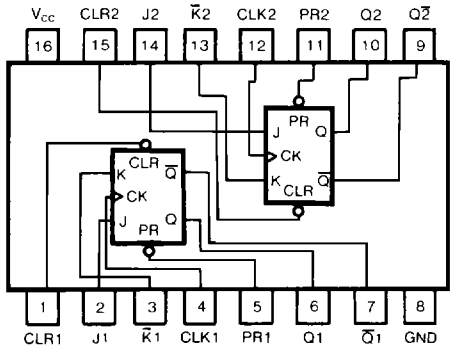
Feature

- Positive Edge-Triggering
- Direct Set and reset inputs
- J and $\overline{K}$ inputs
- Q and $\overline{Q}$ outputs

Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Pin Configuration



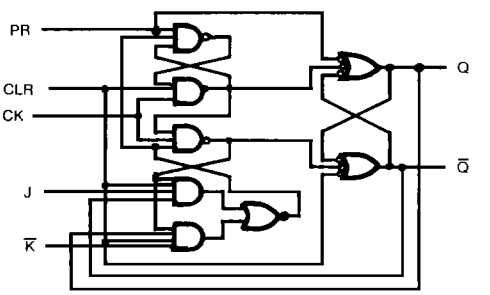
Suffix-Blank. Plastic Dual In Line Package
Suffix-J . Ceramic Dual In Line Package

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_o	$\overline{Q}_o$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_o	$\overline{Q}_o$

X = Either Low or High Logic Level
↑ = Rising Edge of Pulse
* = This configuration is nonstable, that is it will not persist when preset and/or clear inputs return to their inactive (high) state.
Q_o = The output logic level of Q before the indicated input conditions were established
Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse

Functional Block Diagram



Absolute Maximum Ratings

- Supply voltage, V_{CC} 7V
- Input voltage 7V
- Operating free-air temperature range 54LS ..... −55°C to 125°C
  74LS ..... 0°C to 70°C
- Storage temperature range ..... −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	54	4.5	5	5.5	V
		74	4.75	5	5.25	
I_{OH}	High-level output current	54,74			−400	μA
I_{OL}	Low-level output current	54			4	mA
		74			8	
f_{clock}	Clock frequency		0		25	MHz
t_W	Pulse Width	Clock High	18			ns
		Preset Low	15			
		Clear Low	15			
t_{SU}	Setup Time	Data High	30↑			ns
		Data Low	20↑			
t_H	Hold Time		0↑			ns
T_A	Operating free-air temperature	54	−55		125	°C
		74	0		70	

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		74	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	J,$\overline{K}$				0.1	mA
			Clock				0.1	
			Preset				0.2	
			Clear				0.2	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	J,$\overline{K}$				20	μA
			Clock				20	
			Preset				40	
			Clear				40	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	J,$\overline{K}$				−0.4	mA
			Clock				−0.4	
			Present				−0.8	
			Clear				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	8	mA

Note 1: All typical values are at V_{CC}=5V, T_A=25°C

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O=2.25V and 2.125V for 54 and 74 series, respectively with the minimum and and maximum limits reduced by one half from their stated values. This is very useful when using automastic test equipment

Note 3. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded

Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$, $R_L=2k\Omega$	25	33		MHz
t_{PLH}	Clock	Q or $\overline{Q}$			17	25	ns
t_{PHL}					22	30	ns
t_{PLH}	Clear	$\overline{Q}$			17	25	ns
t_{PHL}		Q			22	30	
t_{PLH}	Preset	Q			16	25	ns
t_{PHL}		$\overline{Q}$			22	30	

* f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-level output.
t_{PLH} = propagation delay time, high-to-low-level output