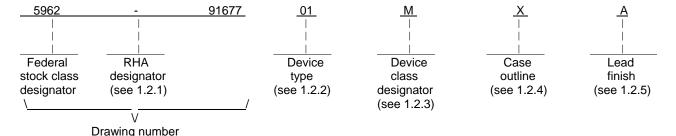
LTR								F	REVISI	ONS										
						DESCF	RIPTIC						DA	TE (YI	R-MO-	-DA)		APPF	ROVE)
A	Boile	erplate	e upda	odate, part of 5 year review. ksr							07-0	01-29		Joseph Rodenbeck						
THE ORIGIN	IAL FIR																			
REV SHEET		ST SI	HEET	OF TH	IIS DF	RAWIN	IG HAS	S BEE	N REF	PLACE	D.									
SHEET	A	A	A	A	A	A	A	A	A	PLACE	D.									
SHEET REV SHEET	15			A 18	A 19		A 21	A 22	A 23											
SHEET REV SHEET REV STATU	15 JS	A	A	A 18 RE	A 19	A	A 21 A	A 22 A	A 23 A	A	A	A 6	A	A	A	A 10	A 11	A 12	A 13	A 14
SHEET REV SHEET	15 JS	A	A	A 18 RE SH	A 19 V EET	A 20	A 21 A 1	A 22 A 2	A 23		A 5	6 EFEN	7	8 UPPL	9 - Y CE	10	11 COL	12 LUMB	13	A 14
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA	15 S ANDAF	A 16	A	A 18 RE SH PRE	A 19 V EET EPARE Je	A 20 ED BY D BY	A 21 A 1	A 22 A 2	A 23 A	A	A 5	6 EFEN	7 ISE SI	8 UPPL	9 .Y CE	10	11 R COL 218-3	12 LUMB	13	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICRO DR THIS D AVA	JS S NNDAF OCIRO AWIN DRAWIN	A 16 RD CUIT G NG IS E	A	A 18 RE SH PRE	A 19 V EET EPARE Je ECKEI Ra	A 20 ED BY effery D D BY symono	A 21 A 1	A 22 A 2 ling	A 23 A	A 4	A 5	6 EFEN CO	7 ISE SI OLUM	8 UPPL IBUS ip://wv	9 Y CE, OHIO ww.ds	10 ENTER O 432 ECC.dla	11 R COL 218-3: I.mil	12 LUMB 990	13 US	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICRO DR THIS D AV FOR U	JS S NDAF OCIRO AWIN DRAWIN AILABL JSE BY NCIES	RD CUIT G NG IS E ALL NTS OF TH	A 17	A 18 RE SH PRE	A 19 V EET EPARE Je ECKEI Ra PROV Mi	A 20 ED BY bymono (ED BY bymono)	A 21 A 1 D. Bowld Monry A. Frye	A 22 A 2 ling	A 23 A 3	A 4 MI DI PC	A 5 CR GIT	6 CCOCAL,	ISE SI OLUM htt IRC , CN FO,	8 UPPL MBUS tp://ww	9 LY CE, OHIO ww.ds T, M	10 ENTER O 432 ECC.dla	11 R COL 218-3: L.mil	12 LUMB 990 2Y,	13 US	
SHEET REV SHEET REV STATU OF SHEETS PMIC N/A STA MICRO DR THIS D AVA FOR U DEPA AND AGE DEPARTME	JS S NDAF OCIRO AWIN DRAWIN AILABL JSE BY NCIES	A 16 RD CUIT G NG IS E ALL NTS OF TH DEFE	A 17	A 18 RE SH PRE CHE	A 19 V EET EPARE Je ECKEI Ra PROV Mi	ED BY Iffery D BY Ightheritance Ightheritance	A 21 A 1 D. Bowled Monray A. Frye PROVA	A 22 A 2 ling	A 23 A 3	A 4 4 DI PC SI SI	A 5 CR GIT ORT	OC AL, ON	ISE SI OLUM htt IRC , CN FO,	BUPPL MBUS Ep://ww CUIT MOS MC	9 LY CE, OHIO ww.ds T, M S, 8	inter O 432 sec.dla IEM K X	11 218-3: i.mil IOR 9 [12 LUMB 990 2Y,	13 US	14

1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.
 - 1.2 PIN. The PIN is as shown in the following example:



- 1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	<u>1</u> /	Circuit function	Access time
01			8K x 9 dual port CMOS FIFO	80 ns
02			8K x 9 dual port CMOS FIFO	50 ns
03			8K x 9 dual port CMOS FIFO	30 ns

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class

Device requirements documentation

M Vendor self-certification to the requirements for MIL-STD-883 compliant,

non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A

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Q or V Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	<u>Descriptive designator</u>	<u>Terminals</u>	Package style
Χ	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Υ	CDIP3-T28 or GDIP4-T28	28	Dual-in-line
Z	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

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1.3 Absolute maximum ratings. 2/

Supply voltage range ----- -0.5 V dc to +7.0 V dc

DC output current ----- 50 mA

Thermal resistance, junction-to-case (θJ_C):

Cases X, Y, and Z ------ See MIL-STD-1835 Junction temperature (T_J) ------ +150°C 3/

1.4 Recommended operating conditions.

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil;quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Non-Government publications</u>. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201; http://www.jedec.org.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

- 2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.
- $\underline{4}$ / For XI input, $V_{IH} = 2.8 \text{ V dc}$
- 5/ 1.5 V dc undershoots are allowed for 10 ns once per cycle.

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2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.
 - 3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.
- 3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.
- 3.5 <u>Marking</u>. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.
- 3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.
- 3.6 <u>Certificate of compliance</u>. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change for device class M.</u> For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.
- 3.9 <u>Verification and review for device class M.</u> For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 <u>Microcircuit group assignment for device class M.</u> Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

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4. VERIFICATION

- 4.1 <u>Sampling and inspection</u>. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.
- 4.2 <u>Screening</u>. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.
 - (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D for circuit, see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
- 4.3 <u>Qualification inspection for device classes Q and V</u>. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE I. <u>Electrical performance characteristics</u>.

Test	Symbol	Conditions $\underline{1}/$ -55°C \leq T _C \leq +125°C	Group A	Device	Limit		Unit
		V _{CC} = 4.5 V to 5.5 V unless otherwise specified	subgroups	type	Min	Max	
Input leakage current	ILI	V _{IN} =0.4 V to V _{CC}	1,2,3	All	-10	10	μA
Output leakage current	lLO	$\overline{R} \ge V_{IH}$ $V_{OUT} = 0.4 \text{ V to V}_{CC}$	1,2,3	All	-10	10	μA
Output logic "1" voltage	VOH	I _{OH} = -2.0 mA	1,2,3	All	2.4		V
Output logic "0" voltage	VOL	IOH = 8.0 mA	1,2,3	All		0.4	V
Active power supply current 2/	ICC1	$f = f_S$ maximum, $V_{CC} = 5.5 \text{ V}$	1,2,3	01 02 03		90 135 225	mA
Standby current 2/	I _{CC2}	$\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT} = V_{IH},$	1,2,3	All		20	mA
Power down current 2/	I _{CC3}	All inputs = V _{CC} - 0.2 V	1,2,3	All		12	mA
Input capacitance	C _{IN}	V _{IN} = 0 V, f = 1 MHz, T _A = 25°C, (see 4.4.1e)	4	All		10	pF
Output capacitance	COUT	V _{OUT} = 0 V, f = 1 MHz, T _A = 25°C, (see 4.4.1e)	4	All		10	pF
Functional testing		See 4.4.1c	7, 8A, 8B	All			
				01		10	
Shift frequency	fs		9,10,11	02		15	MHz
				03		25	
				01	100		
Read cycle time	t _{RC}		9,10,11	02	65		ns
				03	40		

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 ${\sf TABLE\ I.\ } \ \underline{\sf Electrical\ performance\ characteristics} \ \hbox{-}\ Continued.$

Test	Symbol	Conditions 1/	Group A	Device	Limi	ts	Unit
		$ \begin{array}{c} -55^{\circ}\text{C} \leq \text{T}_{\text{C}} \leq +125^{\circ}\text{C} \\ \text{V}_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V} \\ \text{unless otherwise specified} \end{array} $	subgroups	types	Min	Max	
Access time	t _A		9,10,11	01		80	ns
				02		50	
				03		30	
Read recovery time	t _{RR}		9,10,11	01	20		ns
				02	15		
				03	10		
Read pulse width	t _{RPW}		9,10,11	01	80		ns
<u>3</u> /				02	50		-
				03	30		
Read low to data	t _{RLZ}		9,10,11	01,02	10		ns
bus low Z 4/				03	5.0		
Write high to data bus low Z 4/5/	t _{WLZ}		9,10,11	01	20		ns
bus low 2 4/ <u>4</u> / <u>5</u> /				02	15		-
				03	5.0		
Data valid from read high	t _{DV}		9,10,11	All	5.0		ns
Read high to data	t _{RHZ}		9,10,11	01,02		30	ns
bus high Z 4/				03		20	
Write cycle time	t _{wc}		9,10,11	01	100		ns
				02	65		
				03	40		
Write pulse width	t _{WPW}		9,10,11	01	80		ns
. <u>3</u> /				02	50		
				03	30		
Write recovery time	t _{WR}		9,10,11	01	20		ns
				02	15		-
				03	10	-	

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions 1/	ditions 1/ Group A	Device	Limi	ts	Unit
		Conditions $\underline{1}/$ -55°C \leq T _C \leq +125°C V _{CC} = 4.5 V to 5.5 V unless otherwise specified	subgroups	types	Min	Max	
Data setup time	t _{DS}		9,10,11	01	40		ns
				02	30		
				03	18		
Data hold time	t _{DH}		9,10,11	01	10		ns
				02	5.0		.
				03	0		
Reset cycle time	t _{RSC}		9,10,11	01	100		ns
				02	65		
				03	40		
Reset pulse width	t _{RS}		9,10,11	01	80		ns
<u>3</u> /				02	50		
				03	30		1
Reset setup time	t _{RSS}		9,10,11	01	80		ns
<u>4</u> /				02	50		
				03	30		-
Reset recovery time	t _{RSR}		9,10,11	01	20		ns
				02	15		
				03	10		-
Retransmit cycle time	t _{RTC}		9,10,11	01	100		ns
				02	65		
				03	40		-
Retransmit pulse width <u>3</u> /	t _{RT}		9,10,11	01	80		ns
width <u>3</u> /				02	50		
				03	30		_
Retransmit setup	t _{RTS}		9,10,11	01	80		ns
time <u>4</u> /				02	50		
				03	30		

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 ${\sf TABLE\ I.\ } \ \underline{\sf Electrical\ performance\ characteristics} \ \hbox{-}\ Continued.$

Test Syı	Symbol	Conditions 1/	Group A	Device			Unit
		$ \begin{array}{c} -55^{\circ}C \leq T_{C} \leq +125^{\circ}C \\ V_{CC} = 4.5 \text{ V to } 5.5 \text{ V} \\ \text{unless otherwise specified} \end{array} $	subgroups	types	Min	Max	
Retransmit recovery	t _{RTR}		9,10,11	01	20		ns
time				02	15		
				03	10		
Reset to empty flag	t _{EFL}		9,10,11	01		100	ns
low				02		65	.]
				03		40	
Reset to HF and FF high	t _{HFH} ,		9,10,11	01	-	100	ns
riigii	t _{FFH}			02		65	.
				03		40	ļ
Read low to empty flag low	t _{REF}		9,10,11	01		60	ns
				02		45	
				03		30	
Read high to full	t _{RFF}		9,10,11	01		60	ns
flag high				02		45	
				03		30	
Read pulse width	t _{RPE}		9,10,11	01	80	<u> </u>	ns
after EF high				02	50		
				03	30		
Write high to empty	t _{WEF}		9,10,11	01		60	ns
flag high				02		45	
				03		30	
Write low to full flag	t _{WFF}		9,10,11	01		60	ns
low				02		45	
				03		30	
Write low to half-full	t _{WHF}		9,10,11	01		100	ns
flag low	1			02		65	
				03		40	

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TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions 1/	Group A	Device	Limit	<u>s</u>	Unit
		$ \begin{array}{c} -55^{\circ}\text{C} \leq \text{T}_{\text{C}} \leq +\overline{1}25^{\circ}\text{C} \\ \text{V}_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V} \\ \text{unless otherwise specified} \end{array} $	subgroups	types	Min	Max	
Read high to half-full flag high	t _{RHF}		9,10,11	01		100	ns
nag nign				02		65	
				03		40	
Write pulse width	t _{WPF}		9,10,11	01	80		ns
after FF high				02	50		
				03	30		
Read/write low to	t _{XOL}		9,10,11	01		80	ns
XO low				02		50	
				03		30	
Read/write high to	t _{XOH}		9,10,11	01		80	ns
XO high				02		50	
				03		30	
\overline{XI} pulse width $\underline{3}$ /	t _{XI}		9,10,11	01	80		ns
				02	50		
				03	30		
XI recovery time	t _{XIR}		9,10,11	All	10		ns
XI setup time	t _{XIS}		9,10,11	01,02	15		ns
				03	10		

 $[\]underline{1}$ / AC measurements assume transition time \leq 5 ns, input and output timing reference levels = 1.5 V, input levels are from ground to 3.0 V, and output load C_L = 30 pF. See figure 3.

- $\underline{4}/$ If not tested, shall be guaranteed to the limits specified in table I.
- 5/ Only applies to read data flow-through mode.

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 $[\]underline{2}$ / I_{CC} measurements are made with outputs open (only capacitive loading).

 $[\]underline{3}$ / Pulse widths less than minimum are not allowed.

Device types	Al	I
Case outlines	X, Y	Z
Terminal number	Terminal	symbol
1	W	NC
2	D ₈	$\overline{\mathbb{W}}$
3	D_3	D ₈
4	D_2	D_3
5	D ₁	D_2
6	D_0	D_1
7	XI	D_0
8	FF	XI
9	Q_0	FF
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	\overline{R}	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	R
19	Q_7	Q_4
20	XO/HF	Q_5
21	EF	Q_6
22	RS	Q_7
23	FL/RT	XO/HF
24	D ₇	EF
25	D_6	RS
26	D_5	FL/RT
27	D_4	NC
28	V _{CC}	D_7
29		D_6
30		D_5
31		D_4
32		V_{CC}

FIGURE 1. <u>Terminal connections</u>.

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RESET AND RETRANSMIT SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

		Inputs		Internal	status	Outputs		
Mode	 RS	— RT	_ XI	Read pointer	Write pointer	— EF	 FF	— HF
Reset	0	Х	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	Х	Х	X
Read/write	1	1	0	Increment 1/	Increment 1/	X	Х	X

X = logic "don't care" state 1/ Pointer will increment if appropriate flag is high.

RESET AND FIRST LOAD DEPTH EXPANSION/COMPOUND EXPANSION MODE

	Inputs		Internal status		Outputs		
Mode	 RS	 RT	_ XI	Read pointer	Write pointer	— EF	_ FF
Reset first device	0	0	<u>1</u> /	Location zero	Location zero	0	1
Reset all other devices	0	1	<u>1</u> /	Location zero	Location zero	0	1
Read/write	1	Х	<u>1</u> /	X	X	Х	Х

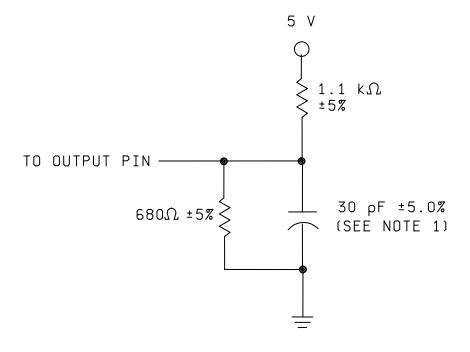
X = logic "don't care" state

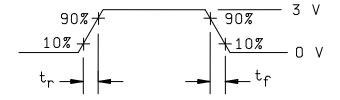
1/ XI is connected to XO of previous device.

FIGURE 2. Truth table.

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OUTPUT LOAD CIRCUIT (OR EQUIVALENT)





NOTE 1: C_L includes scope and jig capacitance.

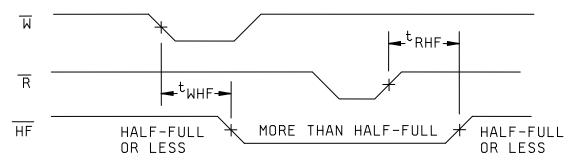
AC test conditions

Input pulse levels Input rise and fall times Input timing reference levels	GND to 3.0 V <u><</u> 5.0 ns 1.5 V
Output reference levels	1.5 V

FIGURE 3. Output load circuit.

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HALF-FULL FLAG TIMING



EXPANSION OUT TIMING

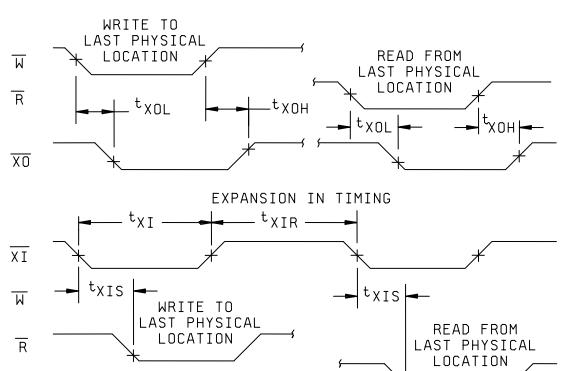


FIGURE 4 Timing waveforms.

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RESET TIMING trick tric

ASYNCHRONOUS WRITE AND READ OPERATION TIMING

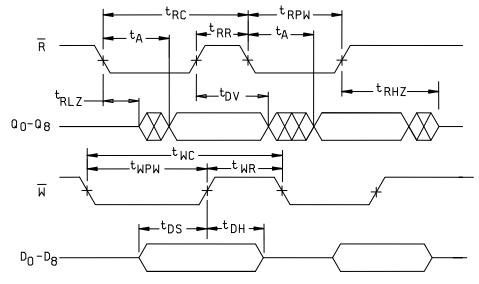
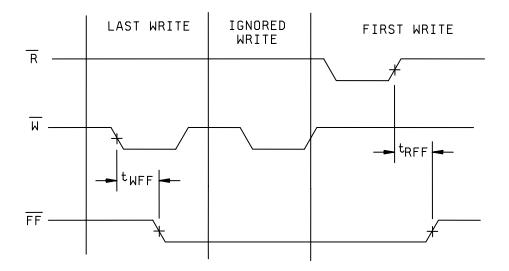


FIGURE 4. Timing waveforms - Continued.

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FULL FLAG FROM LAST WRITE TO FIRST READ



EMPTY FLAG FROM LAST READ TO FIRST WRITE TIMING

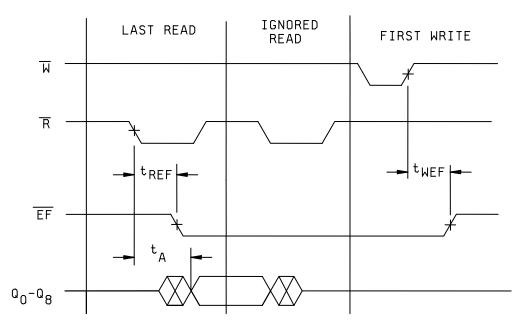


FIGURE 4. Timing waveforms - Continued.

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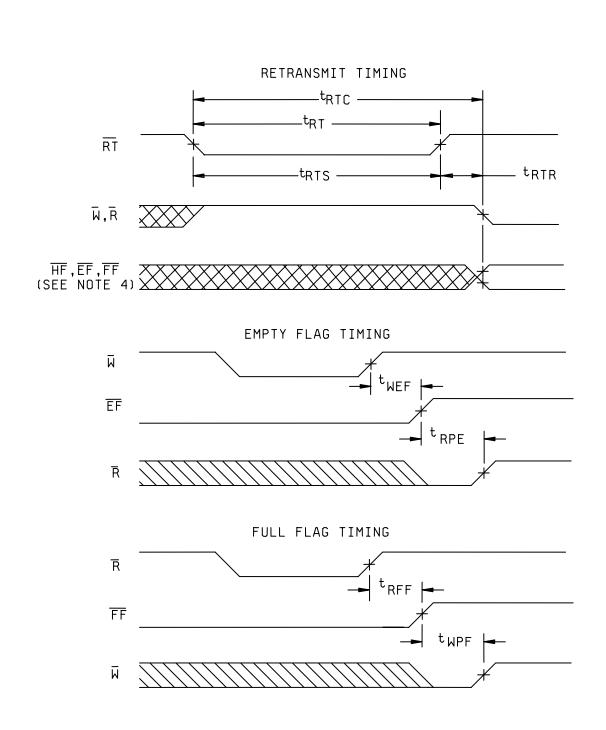


FIGURE 4. Timing waveforms - Continued.

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WRITE DATA FLOW - THROUGH MODE TIMING

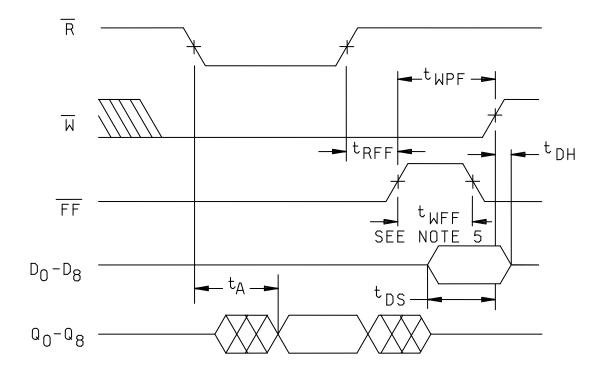
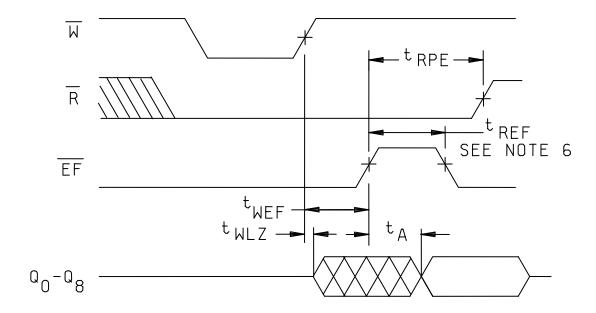


FIGURE 4. <u>Timing waveforms</u> - Continued.

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NOTES:

- 1. $C_L = 30 \text{ pF}$ and includes scope and jig capacitance.
- 2. EF, FF, and HF may change status during reset, but flags will be valid at t_{RSC} .
- 3. \overline{W} and $\overline{R} = V_{IH}$ around the rising edge of \overline{RS} .
- 4. EF, FF, and HF may change status during retransmit, but flags will be valid at t_{RTC} .
- 5. For FIFO full condition only, a write cannot begin until completion of a read. Therefore, t_{WFF} references the rising edge of \overline{FF} .
- 6. For FIFO empty condition only, a read cannot begin until completion of a write. Therefore, t_{REF} references the rising edge of \overline{EF} .

FIGURE 4. Timing waveforms - Continued.

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TABLE IIA. Electrical test requirements. 1/2/3/4/5/6/7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	(in accord	roups lance with 535, table III)
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B Δ	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

TABLE IIB. Delta limits at +25°C.

	Device types	
Test <u>1</u> /	All	
I _{CC2} standby	±10% of specified value in table I	
I _{LI} , I _{LO}	±10% of specified value in table I	

^{1/} The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta Δ .

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 ^{1/} Blank spaces indicate tests are not applicable.
 2/ Any or all subgroups may be combined when using high-speed testers.
 3/ Subgroups 7 and 8 functional tests shall verify the truth table.

^{4/ *} indicates PDA applies to subgroup 1 and 7.

<u>5</u>/ ** see 4.4.1e.

 $[\]underline{6}$ / Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).

<u>7</u>/ See 4.4.1d.

4.4 <u>Conformance inspection</u>. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

- 4.4.1 Group A inspection.
 - a. Tests shall be as specified in table IIA herein.
 - b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
 - c. For device class M, subgroups 7, 8A, and 8B tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7, 8A, and 8B shall include verifying the functionality of the device.
 - d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.
 - e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.
- 4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.
- 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - b. $T_A = +125$ °C, minimum.
 - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.
 - 4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.
- 4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).
 - a. End-point electrical parameters shall be as specified in table IIA herein.
 - b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

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4.5 <u>Delta measurements for device class V.</u> Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.
 - 6.1.2 Substitutability. Device class Q devices will replace device class M devices.
- 6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.
- 6.3 <u>Record of users</u>. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.
- 6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.
- 6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.
- 6.5.1 <u>Timing limits</u>. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
_/////	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
XXXXXX	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

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6.6 Sources of supply.				
6.6.1 <u>Sources of supply for device classes Q and V</u> . Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.				
6.6.2 <u>Approved sources of supply for device class M</u> . Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.				
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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-01-29

Approved sources of supply for SMD 5962-91677 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9167701MXA	0C7V7 <u>3</u> /	CY7C460A-80DMB IDT7205L80DB
5962-9167701MYA	0C7V7 <u>3</u> /	CY7C460A-80/MYA IDT7205L80TDB
5962-9167701MZA	0C7V7 <u>3</u> /	CY7C460A-80LMB IDT7205L80LB
5962-9167702MXA	61772 0C7V7	IDT7205L50DB CY7C460A-50DMB
5962-9167702MYA	61772 0C7V7	IDT7205L50TDB CY7C460A-50/MYA
5962-9167702MZA	61772 0C7V7	IDT7205L50LB CY7C460A-50LMB
5962-9167703MXA	61772 0C7V7	IDT7205L30DB CY7C460A-30DMB
5962-9167703MYA	61772 0C7V7	IDT7205L30TDB CY7C460A-30/MYA
5962-9167703MZA	61772 0C7V7	IDT7205L30LB CY7C460A-30LMB

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ <u>Caution</u>. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source.

STANDARD MICROCIRCUIT DRAWING BULLETIN - Continued.

Vendor CAGEVendor namenumberand address

61772 Integrated Device Technology, Inc.

2975 Stender Way Santa Clara, CA 95054

0C7V7 QP Semiconductor

2945 Oakmead Village Court Santa Clara, CA 95051

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