8-Bit Bus Register Transceivers and Latch Transceivers

SN54/74LS546 SN54/74LS547 SN54/74LS566 SN54/74LS567

Features/Benefits

- **Bidirectional transceivers utilizing registers or latches**
- **Faster than other LS-TTL registers/latches**
- **Independent registers/latches for A bus and B bus**
- **Data can be swapped between internal registers/latches**
- **8-bit data paths match byte boundaries**
- **'LS546/547/566/567 can replace two 'LS374/373/534/533 devices**
- **Independent clock/gate enables for rank A and rank B**
- **High drive capability: I_{OL} = 32 mA (COM), 24 mA (MIL)**
- **24-pin SKINNYDIP® saves space**
- **Three-state outputs drive bus lines**
- **The clock, clock-enable, and latch-enable inputs typically have 300 mV hysteresis**

There are independent clock and clock enable controls for the two directions namely CKA, CKB, CKEA, CKEB for 'LS546/'LS566, and independent gate enable control GA1, GA2, GB1 and $\overline{GB2}$ for 'LS547/'LS567. The CKA/B and $\overline{CKEA/B}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can govern the internal latches, A/B to pass or hold data.

Description

These devices are comprised of a pair of 8-bit registers ('LS546, 'LS566), or a pair of 8-bit latches ('LS547, 'LS567).

The direction of operation is controlled by $\overline{OEAB}$ and $\overline{OEBA}$. When $\overline{OEAB}$ is Low and $\overline{OEBA}$ is High, the operation of the registers/latches is A-to-B direction; when $\overline{OEAB}$ is High and $\overline{OEBA}$ is low, the operation of the registers/latches is B-to-A direction; when $\overline{OEAB}$ and $\overline{OEBA}$ both are High, the A, B buses both are inputs, data will be stored into registers/latches; when $\overline{OEAB}$ and $\overline{OEBA}$ both are Low, the A, B buses both are outputs, data will transfer from internal registers/latches to A, B buses.

There are independent clock and clock enable controls for the two directions: namely CKA, CKB, $\overline{CKEA}$ and $\overline{CKEB}$ for 'LS546/'LS566, and independent gate enable control GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ for 'LS547/'LS567. The CKA/B and $\overline{CKEA/B}$ can control the internal registers A/B to load data or hold data. Similarly, the GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ govern the internal latches, A/B to pass or hold data.

The 'LS546/'547 provide non-inverting polarity; the 'LS566/'LS567 provide inverting polarity. The 'LS546/'LS547/'LS566/'LS567 all have 3-state outputs, and have 32-mA output drive I_{OL} (COM) over the commercial temperature range and 24-mA output drive I_{OL} (MIL), over the military temperature range.

All of the devices are packaged in the popular 24-pin SKINNYDIP package.

Ordering Information

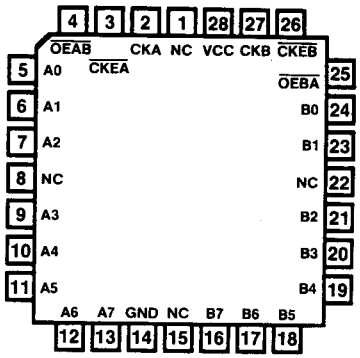
PART NUMBER	PACKAGE	TEMPERATURE	POLARITY	TYPE	POWER
SN54LS546	JS, W, L (28)	Mil	Non-invert	Register	LS
SN74LS546	NS, JS, NL (28)	Com			
SN54LS547	JS, W, L (28)	Mil		Latch	
SN74LS547	NS, JS, NL (28)	Com			
SN54LS566	JS, W, L (28)	Mil	Invert	Register	
SN74LS566	NS, JS, NL (28)	Com			
SN54LS567	JS, W, L (28)	Mil		Latch	
SN74LS567	NS, JS, NL (28)	Com			

SKINNYDIP® is a registered trademark of Monolithic Memories.

TWX: 910-338-2376
2175 Mission College Blvd. Santa Clara, CA 95054-1592 Tel: (408) 970-9700 TWX: 910-338-2374
Monolithic Memories

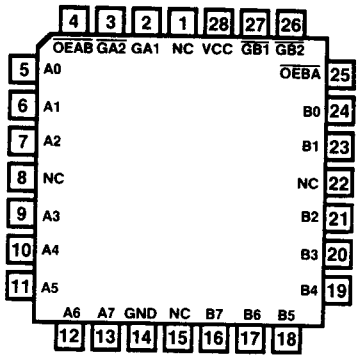
Pin Configurations

SN74LS546



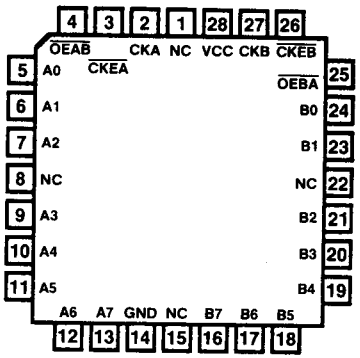
Plastic Chip Carrier

SN74LS547



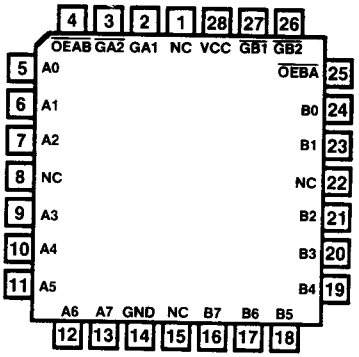
Plastic Chip Carrier

SN74LS566



Plastic Chip Carrier

SN74LS567

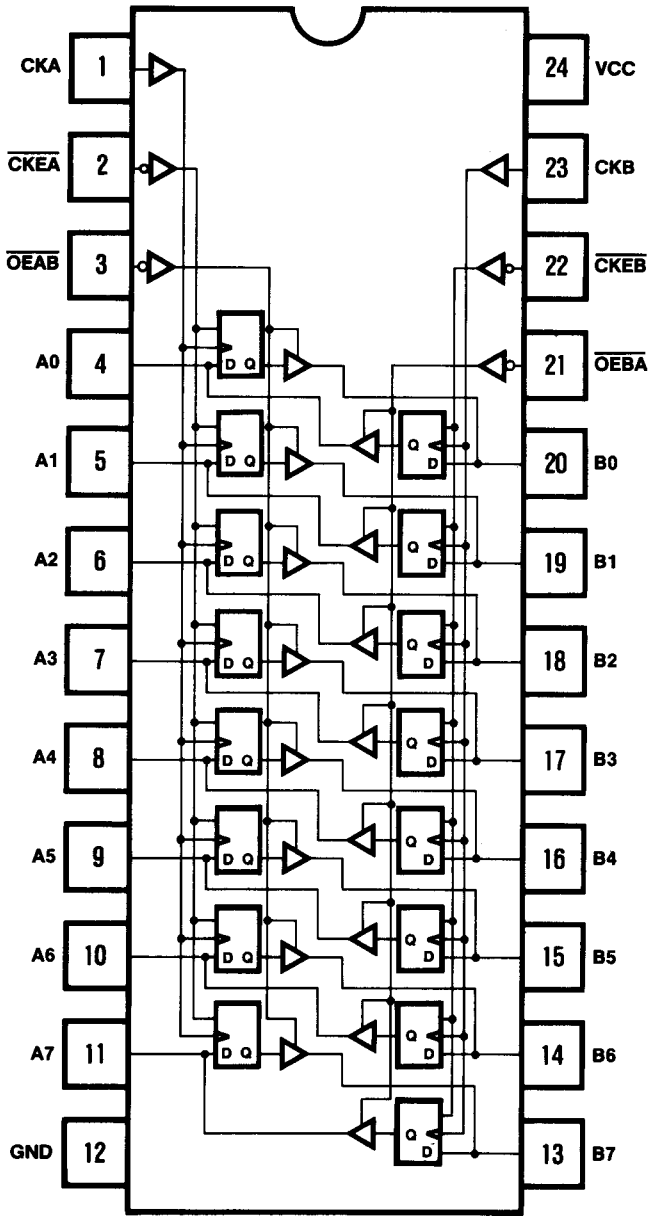


Plastic Chip Carrier

13

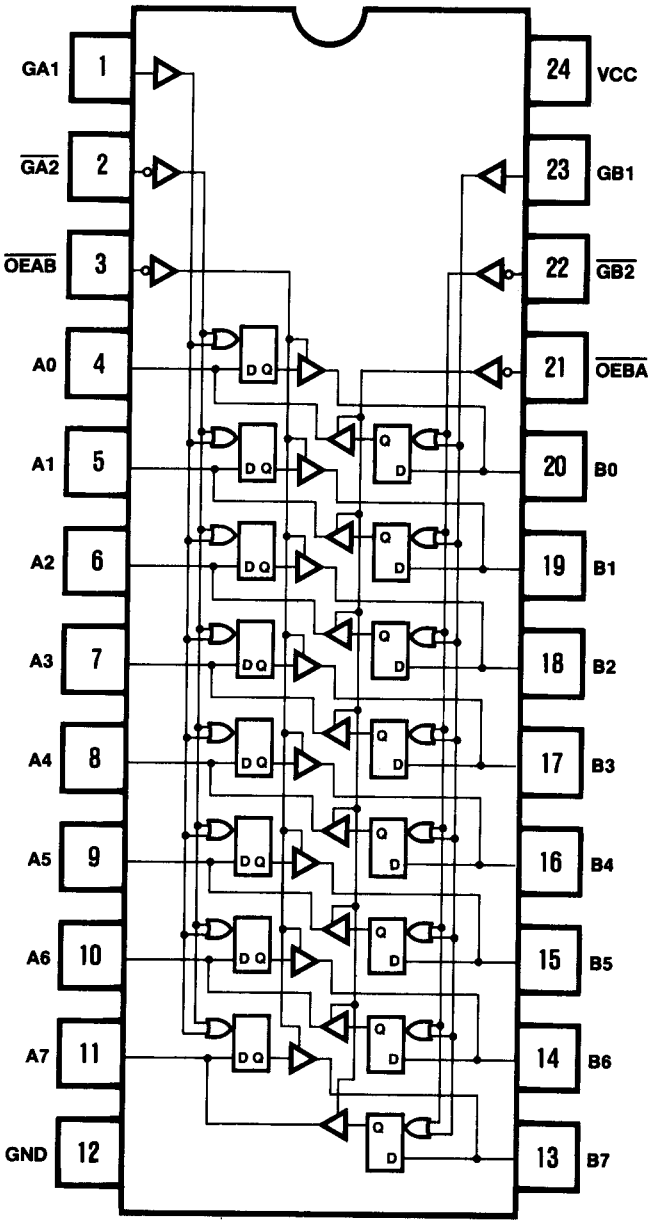
Logic Diagram

SN54/74LS546
REGISTER TRANSCEIVER
NON-INVERTING OUTPUTS



Logic Diagram

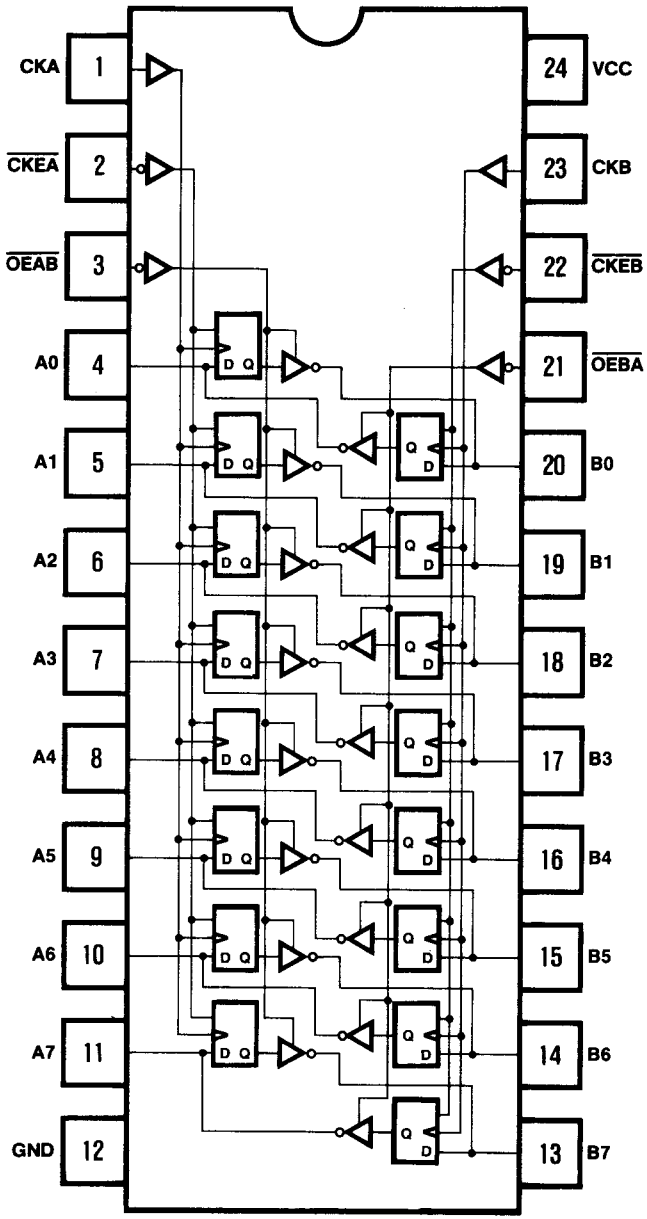
SN54/74LS547
LATCH TRANSCEIVER
NON-INVERTING OUTPUTS



13

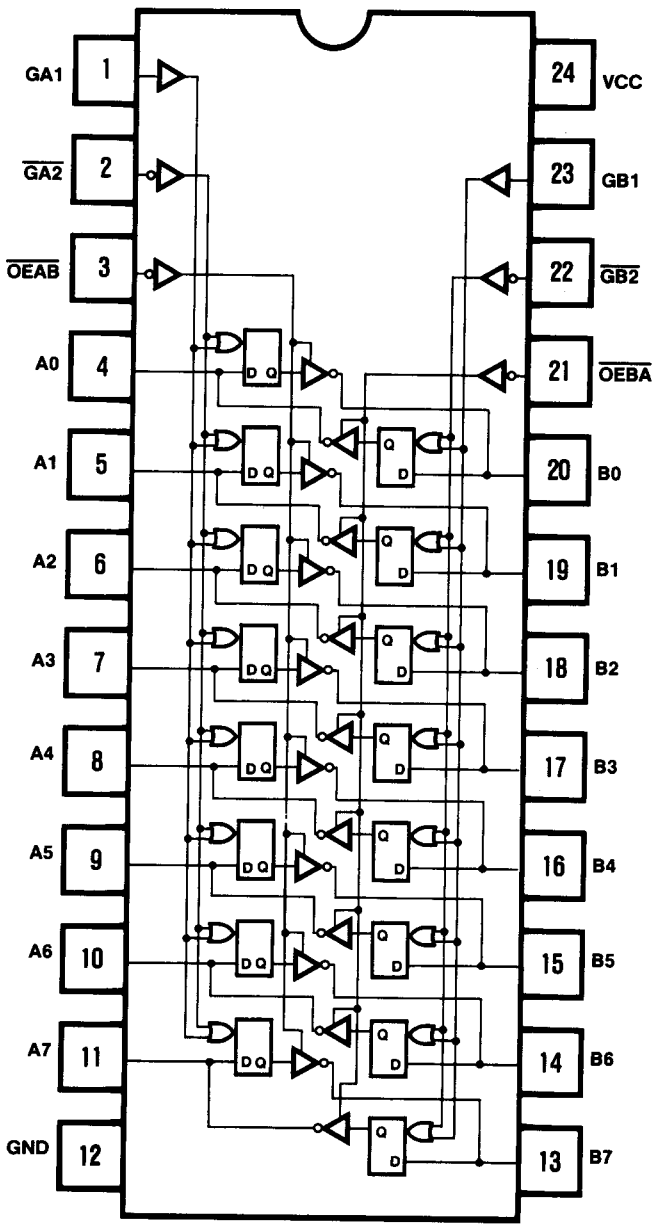
Logic Diagram

SN54/74LS566
REGISTER TRANSCEIVER
INVERTING OUTPUTS



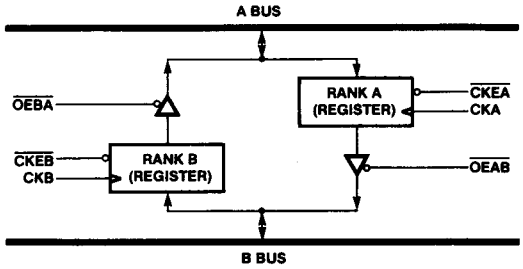
Logic Diagram

SN54/74LS567
LATCH TRANSCEIVER
INVERTING OUTPUTS

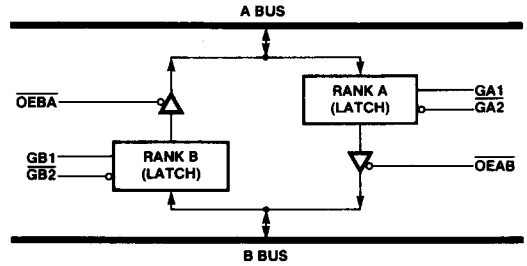


Block Diagrams

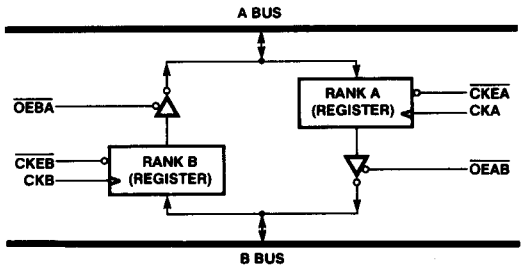
'LS546 (Non-inverting)



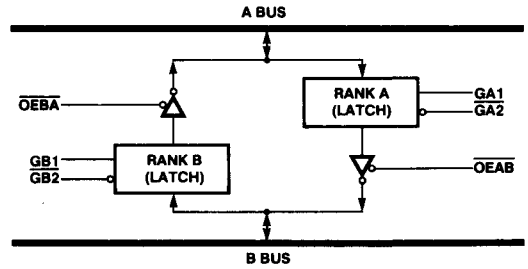
'LS547 (Non-inverting)



'LS566 (Inverting)

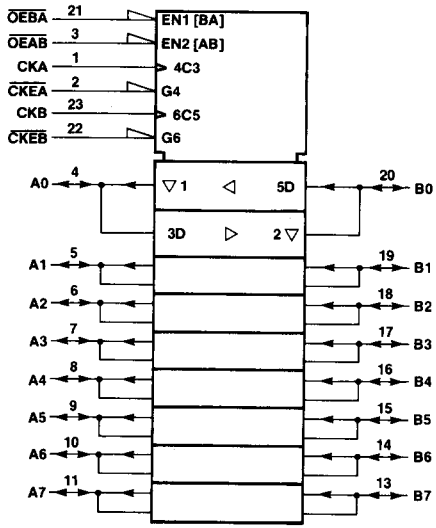


'LS567 (Inverting)

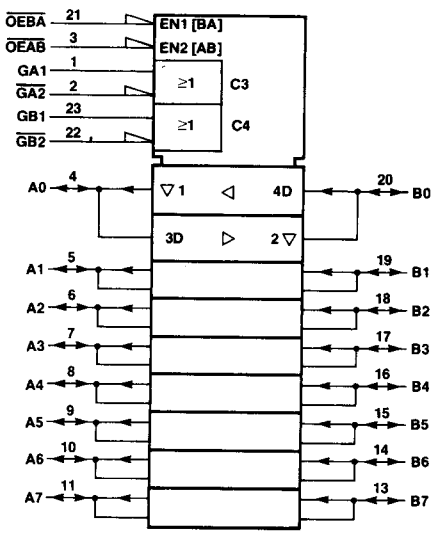


IEEE Symbols

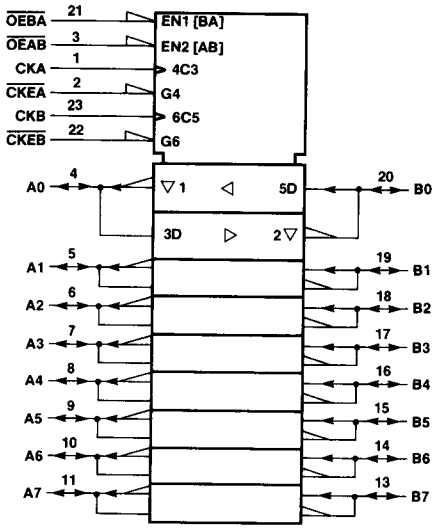
'LS546



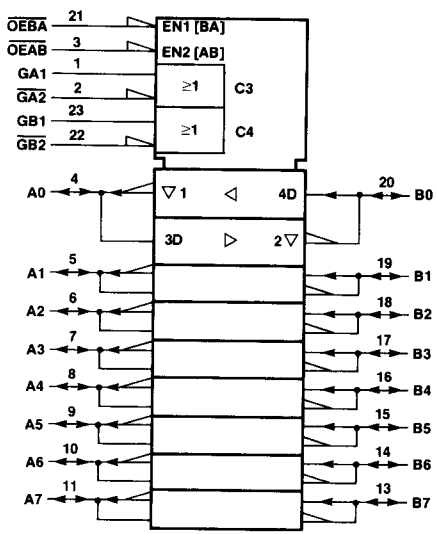
'LS547



'LS566



'LS567



13

Function Table Nomenclature Description

A0-A7: Eight input/output pins on the A side.

B0-B7: Eight input/output pins on the B side.

X: H or L state irrelevant ("Don't Care" conditions).

GA1/$\overline{GA2}$: Gate enables for rank A of 'LS547/'LS567.

GB1/$\overline{GB2}$: Gate enables for rank B of 'LS547/'LS567.

QoA/QoB: Previous data of the internal rank A/B.

GA1	$\overline{GA2}$	RANK A	GB1	$\overline{GB2}$	RANK B
X	L	Enabled (Flush)	X	L	Enabled (Flush)
X	L	Enabled (Flush)	L	H	Disabled (Freeze)
X	L	Enabled (Flush)	H	X	Enabled (Flush)
L	H	Disabled (Freeze)	H	X	Enabled (Flush)
L	H	Disabled (Freeze)	X	L	Enabled (Flush)
L	H	Disabled (Freeze)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	X	L	Enabled (Flush)
H	X	Enabled (Flush)	L	H	Disabled (Freeze)
H	X	Enabled (Flush)	H	X	Enabled (Flush)

$\overline{CKEA}$/$\overline{CKEB}$: Clock enable for rank A/B of 'LS546/'LS566.

CKA/CKB: Clock for rank A/B of 'LS546/'LS566.

UC: H or L or ↓ case (nonclocked operation).

↑: Positive edge of CK causes clocking, if clock enable is asserted.

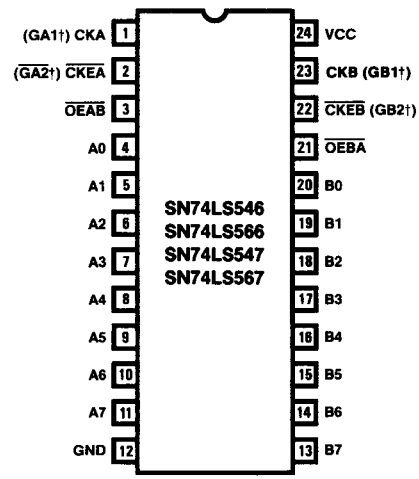
CKA	$\overline{CKEA}$	RANK A	CKB	$\overline{CKEB}$	RANK B
UC	X	Disabled	UC	X	Disabled
↑	L	Enabled	↑	L	Enabled
↑	L	Enabled	↑	H	Disabled
↑	H	Disabled	↑	L	Enabled
↑	H	Disabled	↑	H	Disabled

$\overline{OEAB}$: To enable the A-to-B operation.

$\overline{OEBA}$: To enable the B-to-A operation.

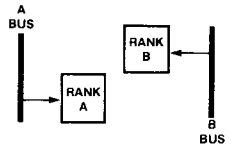
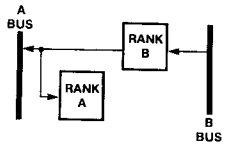
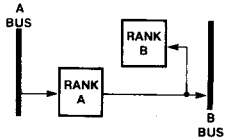
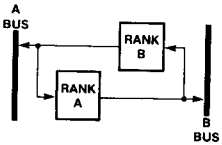
$\overline{OEAB}$	$\overline{OEBA}$	OPERATION DIRECTION
L	L	A, B buses both are outputs (Transfer stored data to bus stored)
L	H	A-to-B
H	L	B-to-A
H	H	A, B buses both are inputs (storage)

Pin Configuration



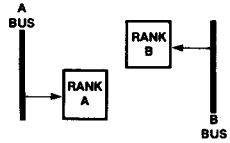
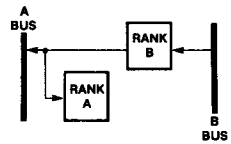
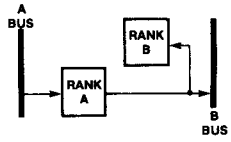
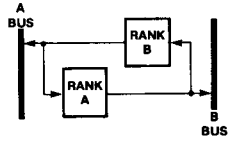
†For SN74LS547, SN74LS567

Bus Operation For 'LS546

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE (A)		RANK A	CLOCK ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		CKA	$\overline{CKEA}$		CKB	$\overline{CKEB}$	
Storage	H	H	Input	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	B bus
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
B-to-A Operation	H	L	Output of Rank B	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	Rank B	UC	X	QoB
						↑	L	Rank B	↑	L	B bus
						↑	L	Rank B	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
A-to-B Operation	L	H	Input	Output of Rank A		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	Rank A
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	Rank A
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	Rank A
						↑	H	QoA	↑	H	QoB
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	Rank A
						UC	X	QoA	↑	H	QoB
						↑	L	Rank B	UC	X	QoB
						↑	L	Rank B	↑	L	Rank A
						↑	L	Rank B	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	Rank A
						↑	H	QoA	↑	H	QoB

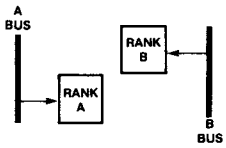
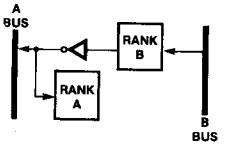
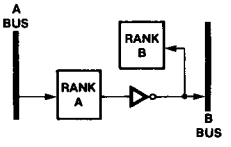
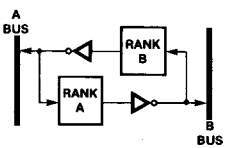
13

Bus Operation For 'LS547

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of Rank B	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	Rank B	L	H	QoB
						H	X	Rank B	H	X	B bus
						H	X	Rank B	X	L	B bus
						X	L	Rank B	L	H	QoB
						X	L	Rank B	H	X	B bus
						X	L	Rank B	X	L	B bus
A-to-B Operation	L	H	Input	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	Rank A
						H	X	A bus	X	L	Rank A
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	Rank A
						X	L	A bus	X	L	Rank A
Transfer Stored Data	L	L	Output of Rank B	Output of Rank A		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	Rank A
						L	H	QoA	X	L	Rank A
						H	X	Rank B	L	H	QoB
						H*	X	Rank B	H	X	Rank A
						H*	X	Rank B	X	L	Rank A
						X	L	Rank B	L	H	QoB
						X*	L	Rank B	H	X	Rank A
						X*	L	Rank B	X	L	Rank A

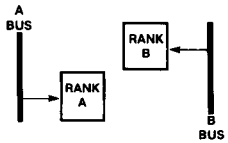
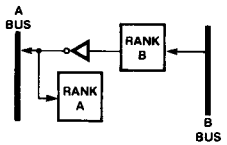
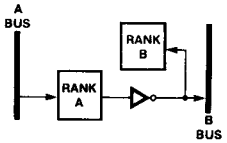
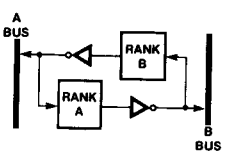
* NOTE: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can cause race conditions.

Bus Operation For 'LS566

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	CLOCK ENABLE (A)		RANK A	CLOCK ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		CKA	$\overline{CKEA}$		CKB	$\overline{CKEB}$	
Storage	H	H	Input	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	B bus
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
B-to-A Operation	H	L	Output of $\overline{\text{Rank B}}$	Input		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	B bus
						UC	X	QoA	↑	H	QoB
						↑	L	$\overline{\text{Rank B}}$	UC	X	QoB
						↑	L	$\overline{\text{Rank B}}$	↑	L	B bus
						↑	L	$\overline{\text{Rank B}}$	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	B bus
						↑	H	QoA	↑	H	QoB
A-to-B Operation	L	H	Input	Output of $\overline{\text{Rank A}}$		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	$\overline{\text{Rank A}}$
						UC	X	QoA	↑	H	QoB
						↑	L	A bus	UC	X	QoB
						↑	L	A bus	↑	L	$\overline{\text{Rank A}}$
						↑	L	A bus	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	$\overline{\text{Rank A}}$
						↑	H	QoA	↑	H	QoB
Transfer Stored Data	L	L	Output of $\overline{\text{Rank B}}$	Output of $\overline{\text{Rank A}}$		UC	X	QoA	UC	X	QoB
						UC	X	QoA	↑	L	$\overline{\text{Rank A}}$
						UC	X	QoA	↑	H	QoB
						↑	L	$\overline{\text{Rank B}}$	UC	X	QoB
						↑	L	$\overline{\text{Rank B}}$	↑	L	$\overline{\text{Rank A}}$
						↑	L	$\overline{\text{Rank B}}$	↑	H	QoB
						↑	H	QoA	UC	X	QoB
						↑	H	QoA	↑	L	$\overline{\text{Rank A}}$
						↑	H	QoA	↑	H	QoB

13

Bus Operation For 'LS567

OPERATION	DIRECTION CONTROL		DATA I/O		BLOCK DIAGRAM	GATE ENABLE (A)		RANK A	GATE ENABLE (B)		RANK B
	$\overline{OEAB}$	$\overline{OEBA}$	A0-A7	B0-B7		GA1	$\overline{GA2}$		GB1	$\overline{GB2}$	
Storage	H	H	Input	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	B bus
						H	X	A bus	X	L	B bus
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	B bus
						X	L	A bus	X	L	B bus
B-to-A Operation	H	L	Output of $\overline{\text{Rank B}}$	Input		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	B bus
						L	H	QoA	X	L	B bus
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H	X	$\overline{\text{Rank B}}$	H	X	B bus
						H	X	$\overline{\text{Rank B}}$	X	L	B bus
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X	L	$\overline{\text{Rank B}}$	H	X	B bus
						X	L	$\overline{\text{Rank B}}$	X	L	B bus
A-to-B Operation	L	H	Input	Output of $\overline{\text{Rank A}}$		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	A bus	L	H	QoB
						H	X	A bus	H	X	$\overline{\text{Rank A}}$
						H	X	A bus	X	L	$\overline{\text{Rank A}}$
						X	L	A bus	L	H	QoB
						X	L	A bus	H	X	$\overline{\text{Rank A}}$
						X	L	A bus	X	L	$\overline{\text{Rank A}}$
Transfer Stored Data	L	L	Output of $\overline{\text{Rank B}}$	Output of $\overline{\text{Rank A}}$		L	H	QoA	L	H	QoB
						L	H	QoA	H	X	$\overline{\text{Rank A}}$
						L	H	QoA	X	L	$\overline{\text{Rank A}}$
						H	X	$\overline{\text{Rank B}}$	L	H	QoB
						H*	X	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						H*	X	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$
						X	L	$\overline{\text{Rank B}}$	L	H	QoB
						X*	L	$\overline{\text{Rank B}}$	H	X	$\overline{\text{Rank A}}$
						X*	L	$\overline{\text{Rank B}}$	X	L	$\overline{\text{Rank A}}$

* NOTE: These controls for $\overline{OEAB}$, $\overline{OEBA}$, GA1, $\overline{GA2}$, GB1 and $\overline{GB2}$ can cause race conditions.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER				MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage				4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature				-55		125	0		75	°C
T_W	Width of clock/gate	'LS546, 'LS566	High	CK	11			8			ns
			Low		19			15			
		'LS547, 'LS567	High	GA1,GB1	10			8			
			Low	$\overline{GA2}$,$\overline{GB2}$	18			16			
T_{su}	Setup time	'LS546	CKA, CKB		14↑			11↑			ns
		'LS547	GA1, GB1		5↓			5↓			
			$\overline{GA2}$, $\overline{GB2}$		15↑			15↑			
		'LS566	CKA, CKB		14↑			11↑			
		'LS567	GA1, GB1		13↓			13↓			
			$\overline{GA2}$, $\overline{GB2}$		22↑			22↑			
T_h	Hold time	'LS546	CKA, CKB		0↑			0↑			ns
		'LS547	GA1, GB1		13↓			13↓			
			$\overline{GA2}$, $\overline{GB2}$		5↑			5↑			
		'LS566	CKA, CKB		0↑			0↑			
		'LS567	GA1, GB1		11↓			11↓			
			$\overline{GA2}$, $\overline{GB2}$		5↑			5↑			
T_{suce}	Setup time for $\overline{CKEA}$, $\overline{CKEB}$, ('LS546, 'LS566 only)				15↑			11↑			ns
T_{hce}	Hold time for $\overline{CKEA}$, $\overline{CKEB}$ ('LS546, 'LS566 only)				5↑			4↑			ns

↑ ↓ the arrow indicates the transition of the clock/gate input used for reference:
↑ for the low-to-high transitions.
↓ for the high-to-low transitions.

13

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IH}	High-level input voltage				2			2			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA			−1.5			−1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V	A or B			−250			−250	μA
				All others			−400			−400	
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V			20			20	μA
I_I	Maximum input current	A or B	V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
		All others		V_I = 7.0 V							
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OL} = 24 mA			0.5				V
				I_{OL} = 32 mA					0.35	0.5	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2V	I_{OH} = −1 mA	2.4	3.4					V
				I_{OH} = −2.6 mA				2.4	3.1		
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V			−250			−250	μA
I_{OZH}				V_O = 2.4 V			20			20	
I_{OS}	Output short-circuit current*		V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	'LS546			180			180	mA
				'LS547			180			180	
				'LS566			180			180	
				'LS567			180			180	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY		COMMERCIAL		UNIT
			'LS546 MIN MAX	'LS547 MIN MAX	'LS546 MIN MAX	'LS547 MIN MAX	
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	33		43		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS546 only)		26		21		ns
t_{PLH}/t_{PHL}	$\overline{GA1}$, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only)			27		24	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS547 only)			23		18	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	25	25	21	21	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	22	22	19	19	ns

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	'LS546 MIN MAX	'LS547 MIN MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	50		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS546 only)		19		ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS547 only)			23	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS547 only)			17	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	19	19	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	17	17	ns

13

Switching Characteristics Over Operating Conditions

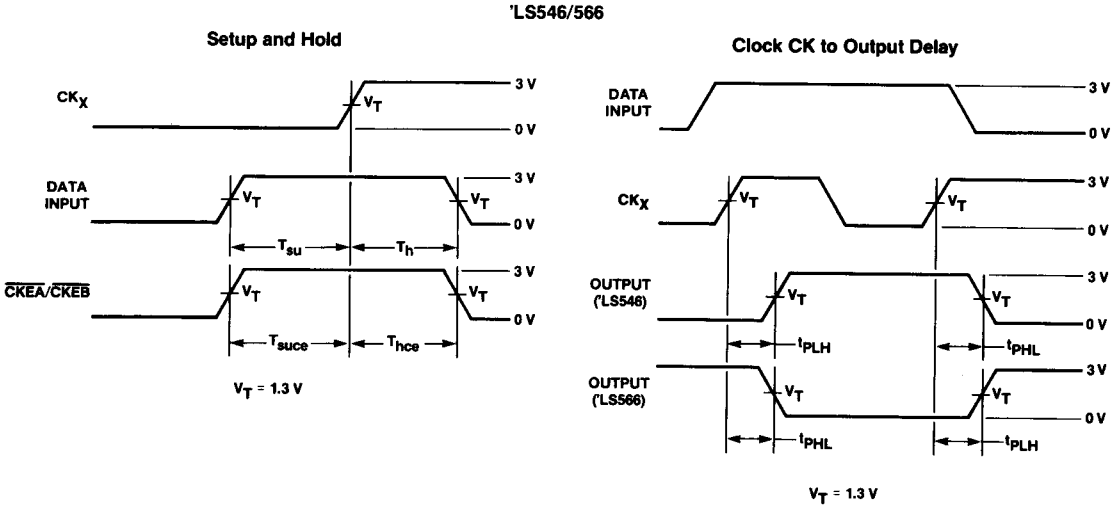
SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY		COMMERCIAL		UNIT
			'LS566 MIN MAX	'LS567 MIN MAX	'LS566 MIN MAX	'LS567 MIN MAX	
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	33		43		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS566 only)		26		21		ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS567 only)			26		24	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS567 only)			29		23	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	25	25	21	21	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	22	22	19	19	ns

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	'LS566 MIN MAX	'LS567 MIN MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 45 pF R_L = 280 Ω $\overline{OE}$ = L	50		MHz
t_{PLH}/t_{PHL}	CK to output delay ('LS566 only)		19		ns
t_{PLH}/t_{PHL}	GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to output delay ('LS567 only)			21	ns
t_{PLH}/t_{PHL}	Data D to output delay ('LS567 only)			19	ns
t_{PZL}/t_{PZH}	Output enable delay	C_L = 45 pF R_L = 280 Ω	19	19	ns
t_{PLZ}/t_{PHZ}	Output disable delay	C_L = 5 pF R_L = 280 Ω	17	17	ns

Definition of Waveforms

'LS546/566

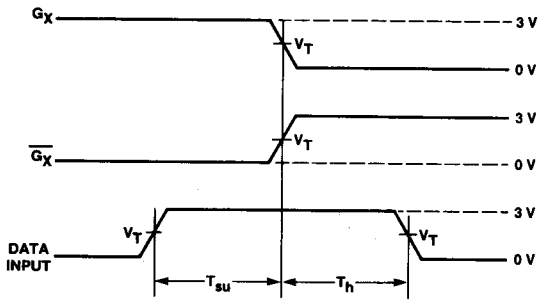


13

Definition of Waveforms

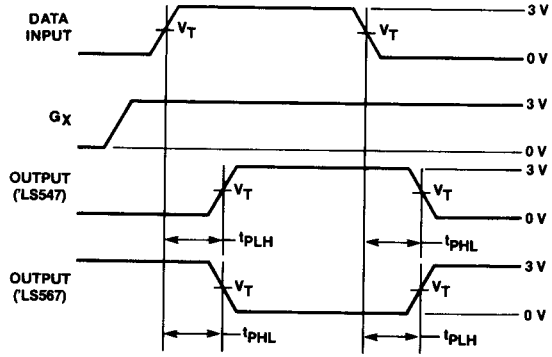
'LS547/567

Setup and Hold



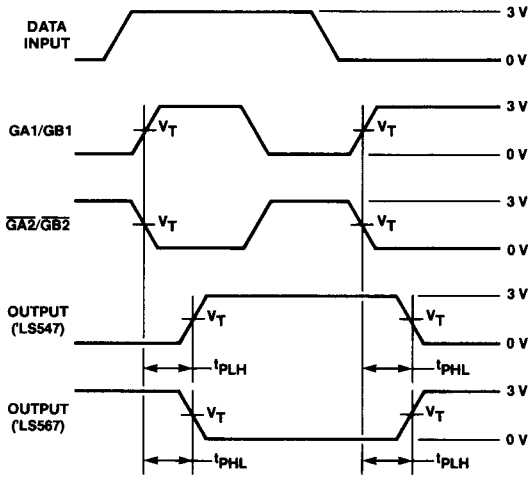
V_T = 1.3 V

Data D to Output Delay



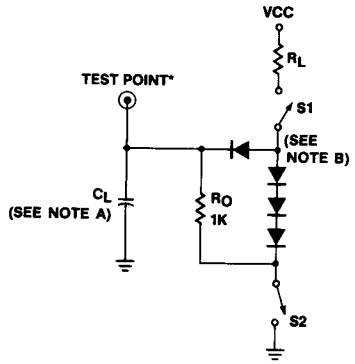
V_T = 1.3 V

GA1, $\overline{GA2}$, GB1 or $\overline{GB2}$ to Output Delay

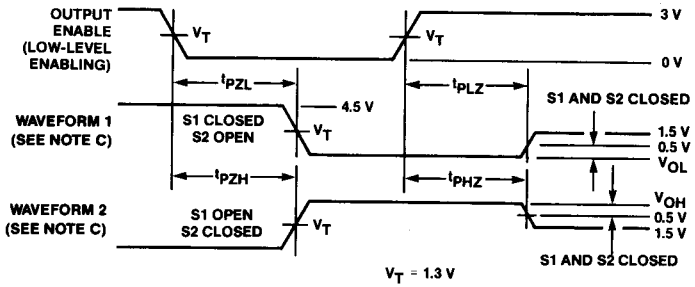


V_T = 1.3 V

Test Load



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



ENABLE AND DISABLE

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} = 50Ω and t_R ≤ 15 ns t_F ≤ 6 ns.
F. When measuring propagation delay times of 3-state outputs, switches S1 and S2 are closed.

13