HARRIS SEMICONDUCTOR

RFG70N06
RFP70N06

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1992

Features

- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- UIS Rating Curve (Single Pulse)
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- +175°C Operating Temperature
- Temperature Compensated SPICE Model Provided

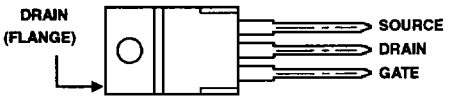
Description

The RFG70N06 and RFP70N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

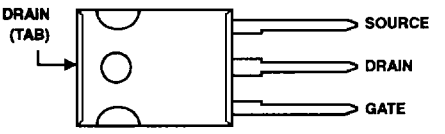
The RFG70N06 is supplied in the JEDEC TO-247 style plastic package and the RFP70N06 is supplied in the JEDEC TO-220AB plastic package.

Packages

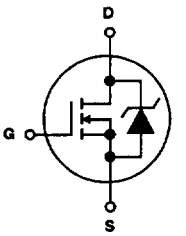
TO-220AB
TOP VIEW



TO-247
TOP VIEW



Terminal Diagram



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFG70N06, RFP70N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	180	A
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
T_C = +25°C	P_D	150	W
Derate above +25°C		1.0	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3206**

Electrical Characteristics At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 0.25mA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 0.25mA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V,	T_C = +25°C	-	-	1	µA
		V_{GS} = 0V	T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(on)}$	I_D = 70A, V_{GS} = 10V		-	-	14	mΩ
Turn-On Time	$t_{(on)}$	V_{DD} = 30V, I_D = 70A R_L = 0.43Ω, V_{GS} = +10V R_{GS} = 2.5Ω		-	-	125	ns
Turn-On Delay Time	$t_{d(on)}$			-	12	-	ns
Rise Time	t_r			-	50	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	40	-	ns
Fall Time	t_f			-	15	-	ns
Turn-Off Time	$t_{(off)}$			-	-	125	ns
Total Gate Charge	$Q_{g(tot)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 70A, R_L = 0.68Ω	-	185	215	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0V to 10V		-	100	115	nC
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0V to 2V		-	5.5	6.5	nC
Plateau Voltage	$V_{(plateau)}$	I_D = 70A, V_{DS} = 15V		-	-	7.5	V
Input Capacitance	C_{iss}	V_{DS} = 25V, V_{GS} = 0V f = 1MHz		-	3000	-	pF
Output Capacitance	C_{oss}			-	900	-	pF
Reverse Transfer Capacitance	C_{rss}			-	300	-	pF
Turn-Off Energy Loss per Cycle	E_{off}	V_{DD} = 30V, I_D = 70A, L = 0.21µH, R_L = 0.43Ω V_{GS} = 10V, R_{GS} = 2.5Ω		-	-	1.0	mJ
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 70A, dI_{SD}/dt = 100A/µs	-	-	125	ns

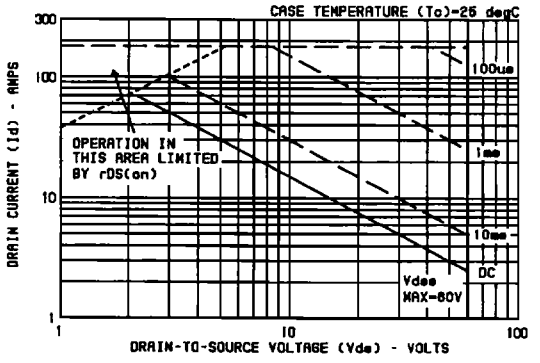


FIGURE 1. SAFE OPERATING AREA CURVE

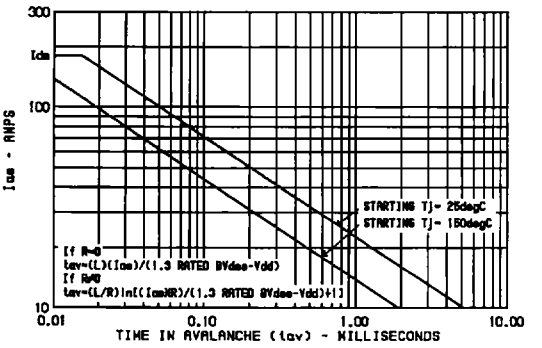


FIGURE 2. UNCLAMPED INDUCTIVE SWITCHING

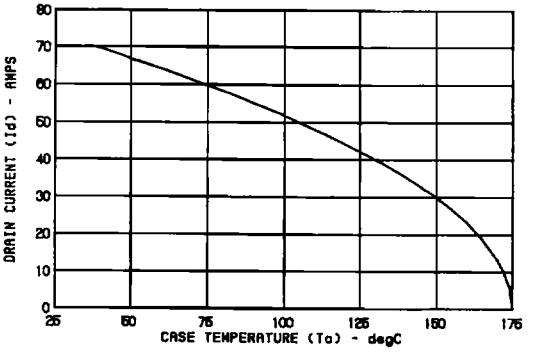


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs. TEMPERATURE

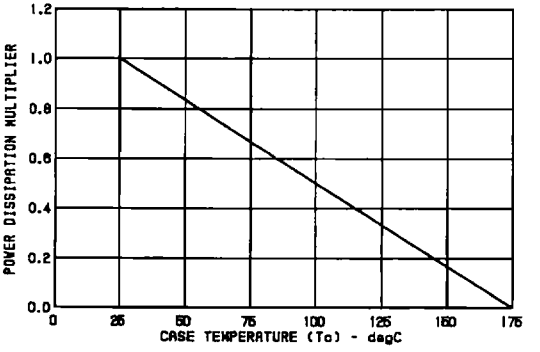


FIGURE 4. NORMALIZED POWER DISSIPATION vs. TEMPERATURE DERATING CURVE

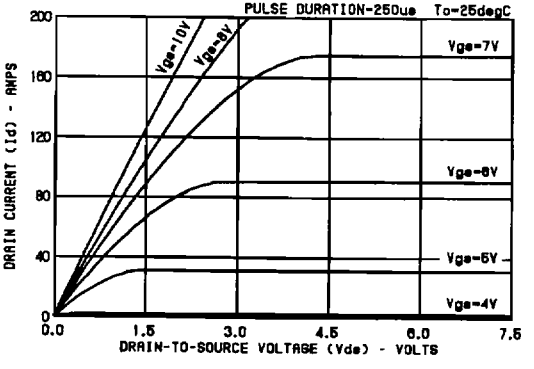


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

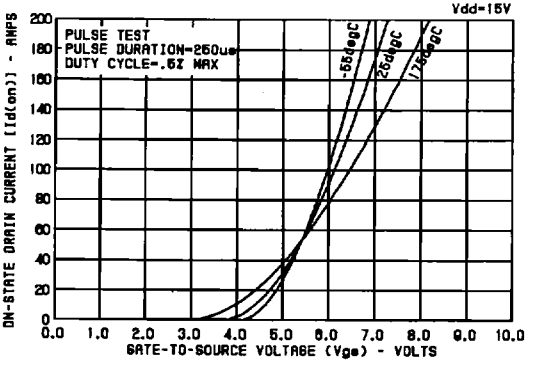


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

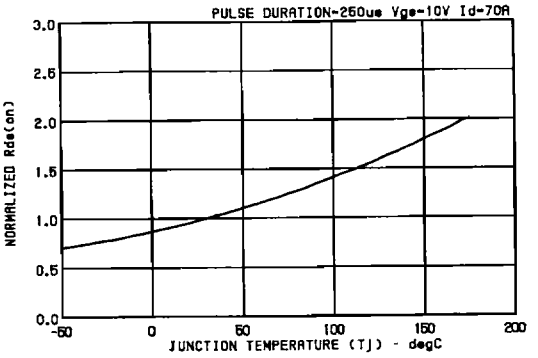


FIGURE 7. NORMALIZED $r_{DS(on)}$ vs. JUNCTION TEMPERATURE

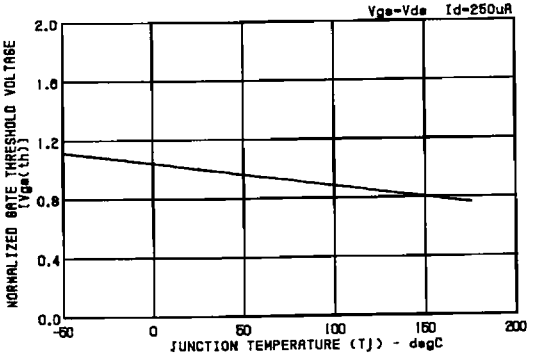


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs. TEMPERATURE

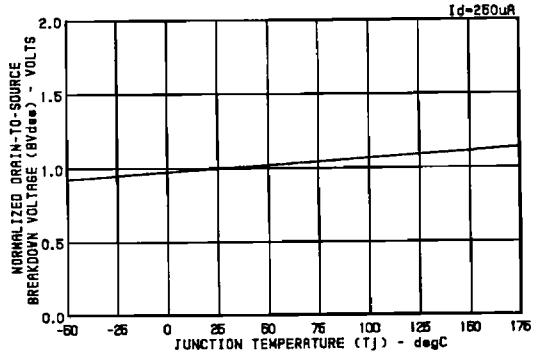


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs. TEMPERATURE

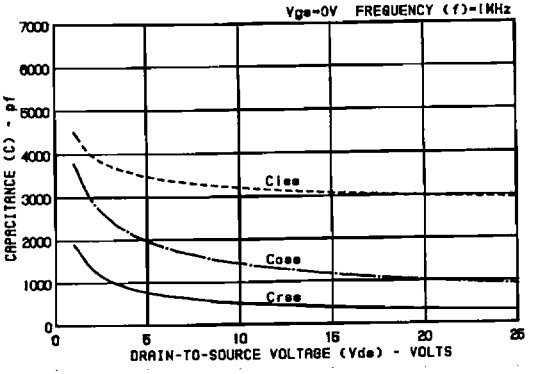


FIGURE 10. TYPICAL CAPACITANCE vs. VOLTAGE

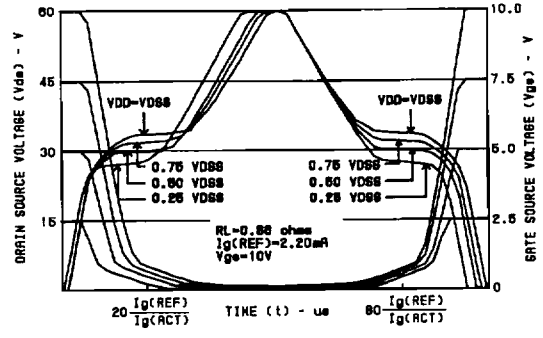


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

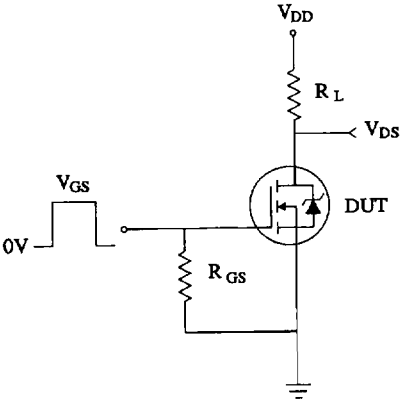


FIGURE 12. RESISTIVE SWITCHING TEST CIRCUIT

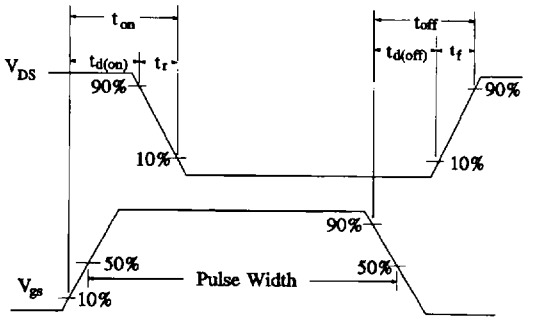


FIGURE 13. RESISTIVE SWITCHING WAVEFORMS

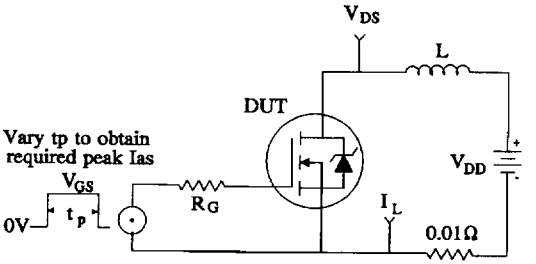


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

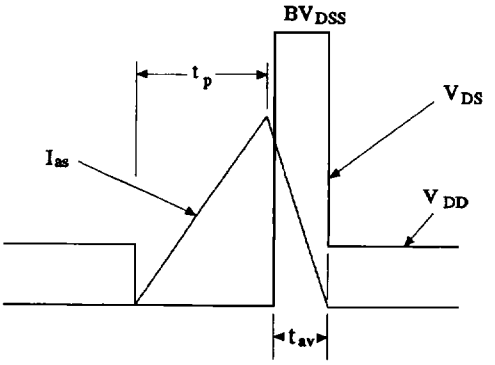
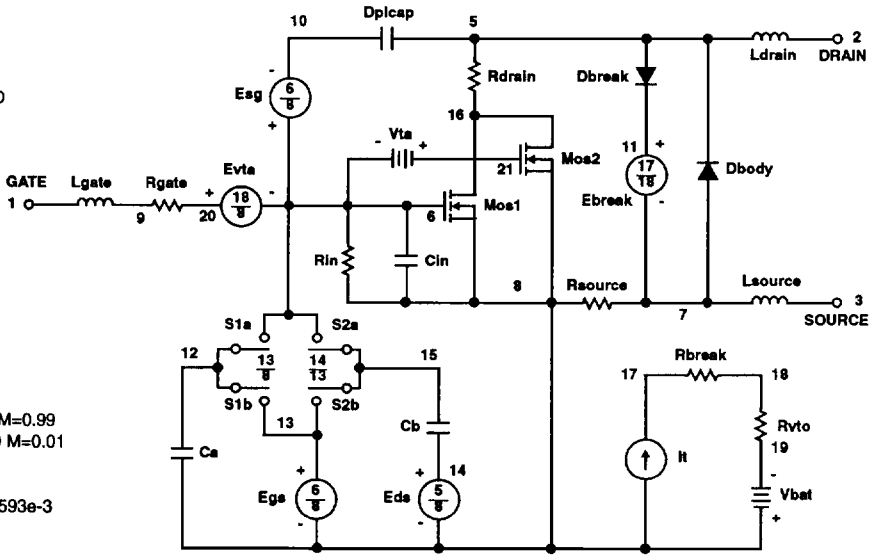


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

PSPICE Model For the RFG70N06, RFP70N06

```
SUBCKT TA49007 2 1 3 ;        rev 3/20/92
*Nom Temp=25 deg C

Ca 12 8 5.56e-9
Cb 15 14 5.303e-9
Cin 6 8 2.63e-9

Dbody 7 5 DBDMOD
Dplcap 10 5 DPLCAPMOD
Dbreak 5 11 DBKMOD

Ebreak 11 7 17 18 65.1
Eds 14 8 5 8 1
Egs 13 8 6 8 1
Esg 6 10 6 8 1
Evto 20 6 18 8 1

It 8 17 1

Lgate 1 9 3.10e-9
Ldrain 2 5 1e-9
Lsource 3 7 1.82e-9

Mos1 16 6 8 8 MOSMOD M=0.99
Mos2 16 21 8 8 MOSMOD M=0.01

Rbreak 17 18 RBKMOD 1
Rdrain 5 16 RDSMOD 4.6593e-3
Rgate 9 20 1.21
Rin 6 8 1e9
Rsource 8 7 RDSMOD 1.822e-3
Rvto 18 19 RVTOMOD 1

S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD

Vbat 8 19 DC 1
Vto 21 6 0.6977

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.90 VOFF=-2.90)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.90 VOFF=-4.90)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.20 VOFF=4.80)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.80 VOFF=-3.20)
.MODEL DBDMOD D (IS=1.11e-12 RS=2.91e-3 TRS1=3.26e-3 TRS2=-5.07e-6 CJO=3.12e-9 TT=6.18e-8)
.MODEL DBKMOD D (RS=9.46e-2 TRS1=8.47e-4 TRS2=-1.31e-6)
.MODEL DPLCAPMOD D (CJO=1.92e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.674 KP=38.507 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.55e-4 TC2=5.99e-8)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=2.37e-5)
.MODEL RVTOMOD RES (TC1=-3.71e-3 TC2=-6.01e-7)

.ENDS
```



Note: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFet Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.