TRUTH TABLE

Mode	$\overline{E1}$	$\overline{E2}$	$\overline{WE}$	$\overline{OE}$	DQ	Power
Standby	H	X	X	X	HIGH Z	Standby
Standby	X	H	X	X	HIGH Z	Standby
Read	L	L	H	L	DOUT	Active
Deselect	L	L	H	H	HIGH Z	Active
Write (1)	L	L	L	L	DIN	Active
Write (1)	L	L	L	H	HIGH Z	Active
Write (2)	L	L	L	X	HIGH Z	Active

X = H or L

1. For VT6285H/85HL only.
2. For VT6286H/86HL only.

TIMING CHARACTERISTICS TA=0°C to +70°C, VCC=5 V ±10%, Note 1

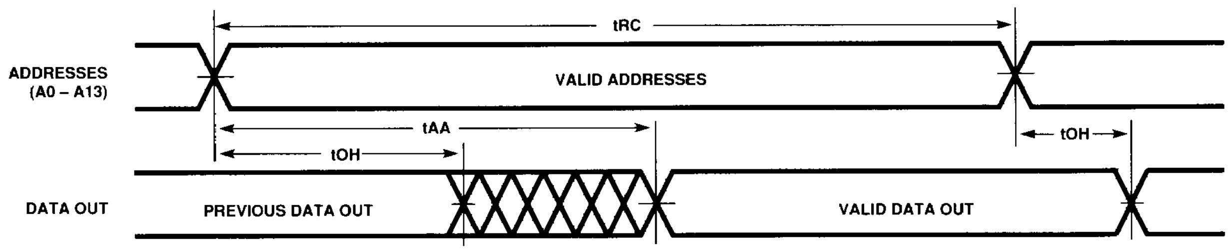
READ CYCLE

Symbol	Parameter	VT6285H(L)-15 VT6286H(L)-15		VT6285H(L)-20 VT6286H(L)-20		VT6285H(L)-25 VT6286H(L)-25		VT6285H(L)-35 VT6286H(L)-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
tRC	Read Cycle Time	15		20		25		35		ns
tAA	Address Access Time		15		20		25		35	ns
tEA	Chip Enable to Output Valid		15		20		25		35	ns
tOH	Output Hold from Address Change	3		4		5		5		ns
tGA	Output Enable LOW to Output Valid		8		10		15		20	ns
tLZG	Output Enable LOW to Output Low Z (Output Load Figure 1b), Note 2	0		0		0		0		ns
tHZG	Output Enable HIGH to Output High Z (Output Load Figure 1b), Note 2		7		10		15		20	ns
tLZE	Chip Enable to Output in Low Z (Output Load Figure 1b), Note 2	0		0		0		0		ns
tHZE	Chip Enable to Output High Z (Output Load Figure 1b), Note 2		8		10		15		20	ns
tPU	Chip Enable to Power- Up, Note 2	0		0		0		0		ns
tPD	Chip Enable to Power-Down, Note 2		15		20		25		35	ns

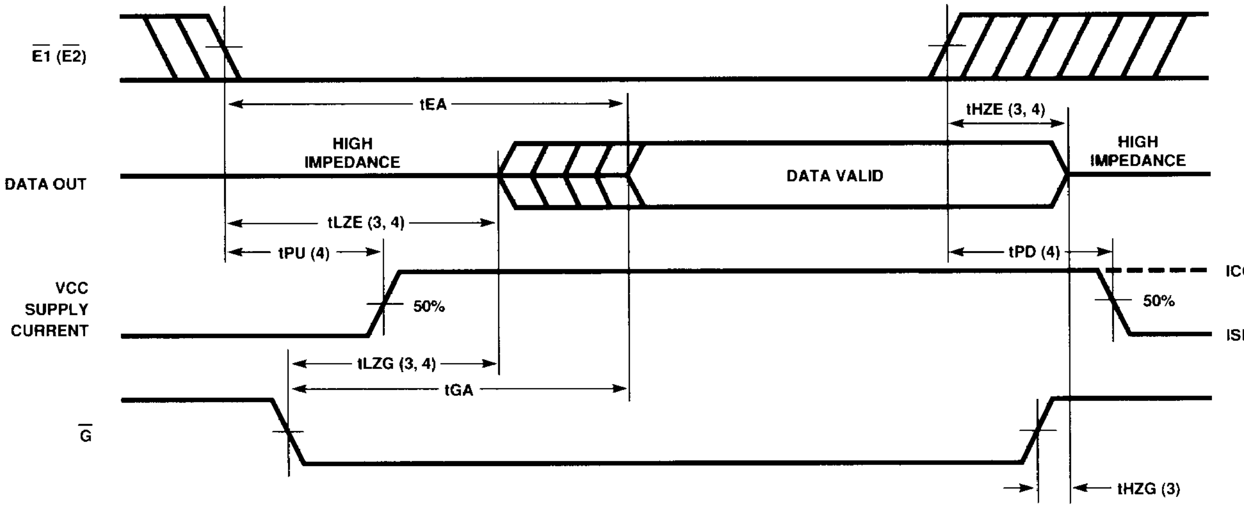
Notes:
1. All timing parameters are measured with output load Figure 1a unless otherwise noted.
2. This parameter is guaranteed by design and not 100% tested.

TIMING DIAGRAMS

READ CYCLE NO. 1 ($\overline{WE}$ = VIH; $\overline{E1}$/$\overline{E2}$ = VIL; $\overline{OE}$ = VIL)



READ CYCLE NO. 2 ($\overline{WE}$ = VIH), Notes 1 and 2



Notes:

1. Addresses valid prior to or coincident with $\overline{E1}$ and/or $\overline{E2}$ transition LOW, and must remain unchanged until $\overline{E1}$/$\overline{E2}$ transition HIGH.
2. $\overline{E2}$ timing is identical to $\overline{E1}$ timing.
3. Transition is measured ±200 mV from steady state voltage with loading specified in Figure 1b.
4. This parameter is guaranteed by design and not 100% tested.

TIMING CHARACTERISTICS TA=0°C to +70°C, VCC=5 V ±10%, Note 1

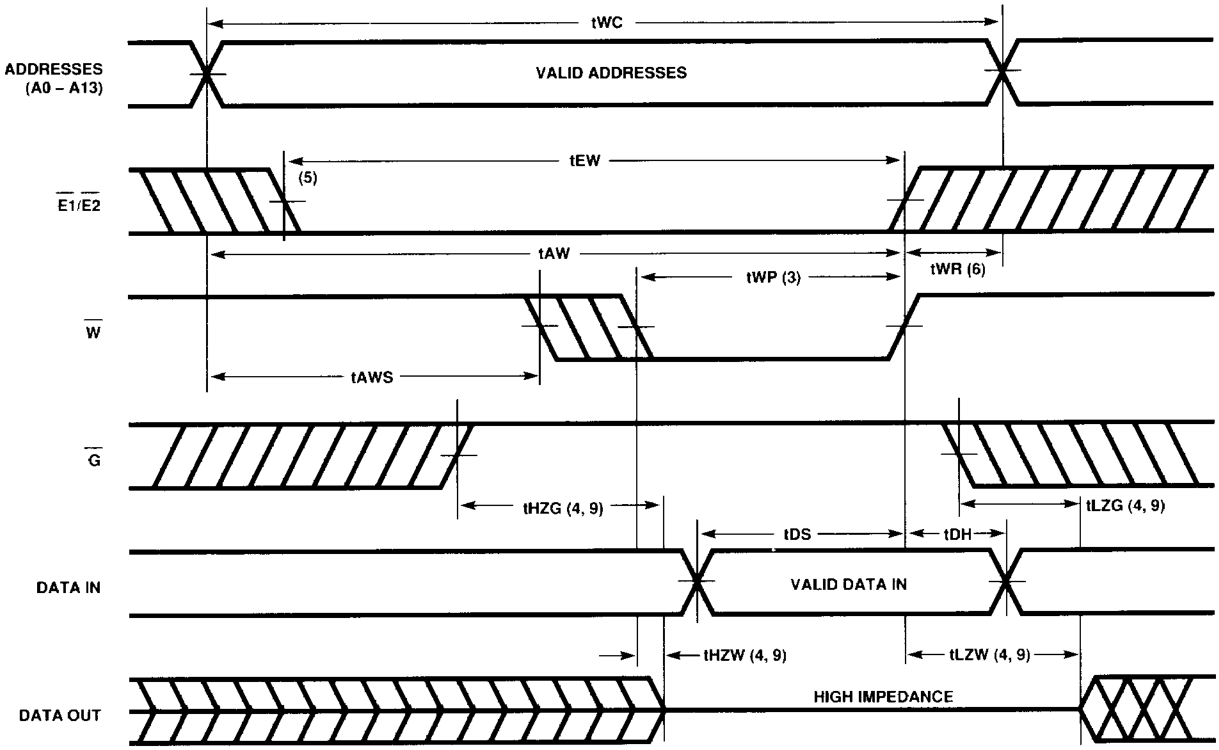
WRITE CYCLE

Symbol	Parameter	VT6285H(L)-15 VT6286H(L)-15 Min	Max	VT6285H(L)-20 VT6286H(L)-20 Min	Max	VT6285H(L)-25 VT6286H(L)-25 Min	Max	VT6285H(L)-35 VT6286H(L)-35 Min	Max	Unit
tWC	Write Cycle Time	15		20		25		35		ns
tEW	Chip Enable to Write End	12		15		20		25		ns
tAW	Address Set-Up Time to Write End	12		15		20		25		ns
tWR	Write Recovery Time	0		0		0		0		ns
tAWS	Address Set-Up Time to Write Start	0		0		0		0		ns
tWP	Write Pulse Width	12		15		20		25		ns
tDS	Data In Set-Up Time to Write End	9		12		15		20		ns
tDH	Data In Hold Time after Write End	0		0		0		0		ns
tHZW	Write Enable LOW to Output High Z (Output Load Figure 1b), Notes 3 and 4	0	8	0	10	0	15	0	15	ns
tLZW	Output Active from End of Write, Notes 3 and 4	3		3		3		3		ns
tAWE	Write Enable to Output Valid, Notes 2 and 4		12		15		20		30	ns
tADV	Data Valid to Output Valid, Notes 2 and 4		12		15		20		30	ns

Notes:
1. All timing parameters were measured with output load Figure 1a unless otherwise noted.
2. For VT6285H/85HL only.
3. For VT6286H/86HL only.
4. This parameter is guaranteed by design and not 100% tested.

TIMING DIAGRAMS

WRITE CYCLE NO. 1 ($\overline{W}$ Controlled), Notes 1 and 2

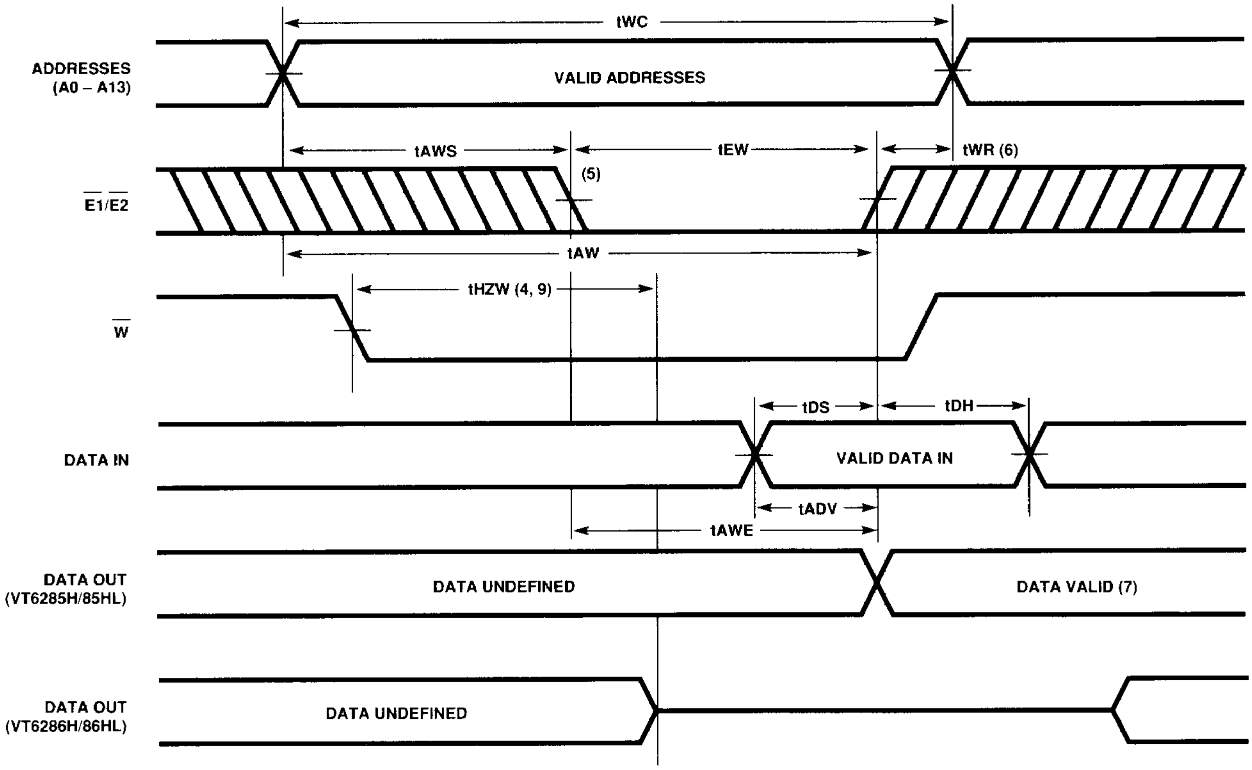


Notes:

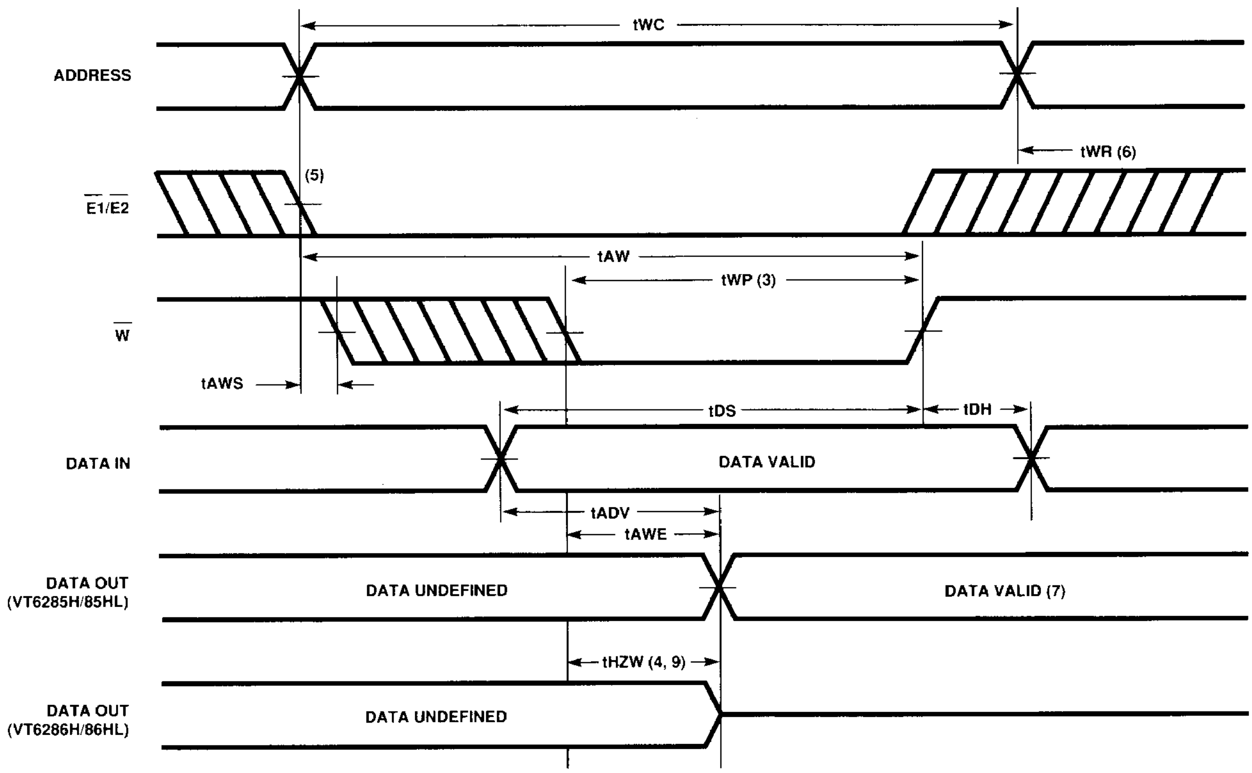
1. All timing parameters were measured with output load Figure 1a unless otherwise noted.
2. $\overline{E1}$, $\overline{E2}$ and $\overline{W}$ must be LOW to initiate a write. Either $\overline{E1}$, $\overline{E2}$ or $\overline{W}$ can terminate a write by going HIGH; thus, data set-up and hold are referenced to the trailing edge of $\overline{E1}$, $\overline{E2}$ or $\overline{W}$, whichever occurs first.
3. A write occurs during the overlap (tWP or tEW) of a LOW $\overline{W}$, a LOW $\overline{E1}$ and a LOW $\overline{E2}$.
4. Transition is measured ±200 mV from steady voltage with loading specified in Figure 1b.
5. If the $\overline{E1}$ LOW transition and/or $\overline{E2}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. tWR is measured from the earlier of $\overline{E1}$/$\overline{E2}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
7. Data Out=Data In.
8. $\overline{OE}$ is continuously low ($\overline{OE}$=VIL).
9. This parameter is guaranteed by design and not 100% tested.

TIMING DIAGRAMS (Cont.)

WRITE CYCLE NO. 2 ($\overline{E1}$ AND $\overline{E2}$ Controlled), Notes 1, 2, and 8; Page 6



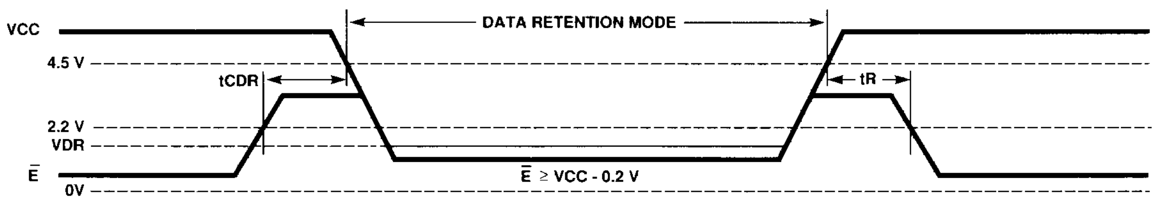
WRITE CYCLE NO. 3 ($\overline{W}$ Controlled; $\overline{OE}$ = LOW), Notes 1 and 2; Page 6



LOW VCC DATA RETENTION CHARACTERISTICS (VT6285HL and VT6286HL only) TA=0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
VDR	VCC for Data Retention	2.0			V	$\overline{E}$≥VCC −0.2 V, VIN≥VCC −0.2 V or 0 V≤VIN≤0.2 V
ICCDR	Data Retention Current (VCC=3.0 V)		1	50	μA	
tCDR	Chip Disable to Data Retention Time	0			ns	
tR	Operation Recovery Time	tRC			ns	

LOW VCC DATA RETENTION WAVEFORM (VT6285HL and VT6286HL only)



PACKAGE OUTLINES

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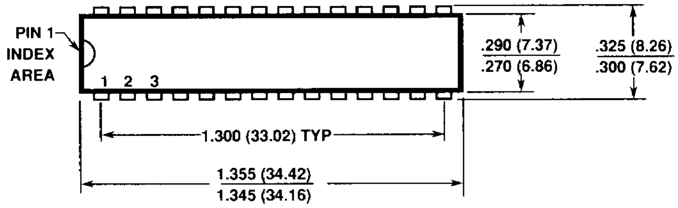
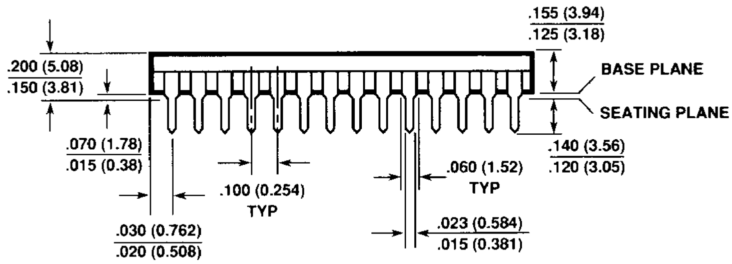
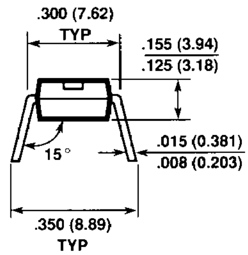


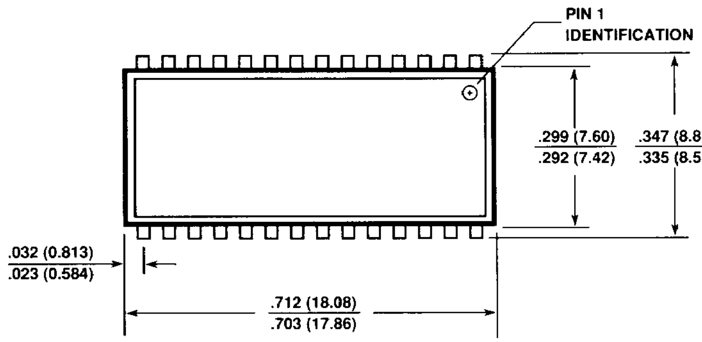


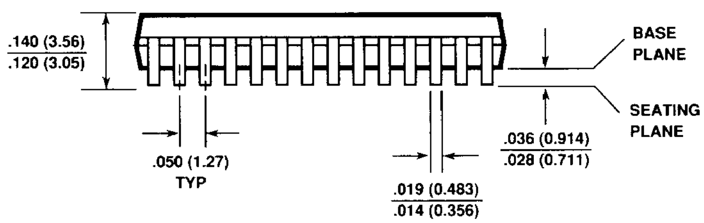


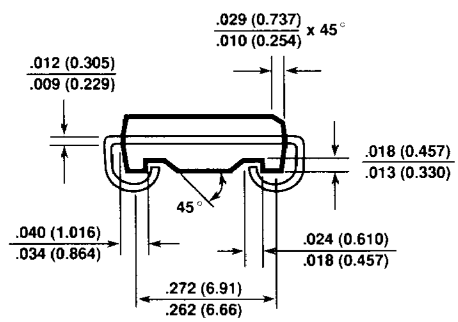
00-00000 4/88

NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: ALLOY 42 OR COPPER.
3. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.
4. PACKAGE LENGTH DOES NOT INCLUDE END FLASH BURR, WHICH IS .010 (0.254) MAX. AT EACH END.
5. TOLERANCE TO BE ± .005 (0.127).

28-LEAD 300 MIL SMALL OUTLINE "J-LEAD" (SOJ)







00-00000 4/88

NOTES: UNLESS OTHERWISE SPECIFIED.
1. LEAD FINISH: MATTE TIN PLATE OR LEAD/TIN SOLDER.
2. LEAD MATERIAL: COPPER.
3. CONTROLLING DIMENSIONS ARE METRIC, ALL METRIC DIMENSIONS ARE IN PARENTHESES.
4. DIMENSIONS DO NOT INCLUDE MOLD FLASH, WHICH IS .006 (0.152) MAX.
5. TOLERANCE TO BE ± .005 (0.127).

ORDER INFORMATION

Part Number	Access Time	Package
VT6285H-15PC	15 ns	Plastic DIP
VT6285H-15JC		SOJ
VT6286H-15PC		Plastic DIP
VT6286H-15JC		SOJ
VT6285HL-15PC	15 ns	Plastic DIP
VT6285HL-15JC		SOJ
VT6286HL-15PC		Plastic DIP
VT6286HL-15JC		SOJ
VT6285H-20PC	20 ns	Plastic DIP
VT6285H-20JC		SOJ
VT6286H-20PC		Plastic DIP
VT6286H-20JC		SOJ
VT6285HL-20PC	20 ns	Plastic DIP
VT6285HL-20JC		SOJ
VT6286HL-20PC		Plastic DIP
VT6286HL-20JC		SOJ
VT6285H-25PC	25 ns	Plastic DIP
VT6285H-25JC		SOJ
VT6286H-25PC		Plastic DIP
VT6286H-25JC		SOJ
VT6285HL-25PC	25 ns	Plastic DIP
VT6285HL-25JC		SOJ
VT6286HL-25PC		Plastic DIP
VT6286HL-25JC		SOJ
VT6285H-35PC	35 ns	Plastic DIP
VT6285H-35JC		SOJ
VT6286H-35PC		Plastic DIP
VT6286H-35JC		SOJ
VT6285HL-35PC	35 ns	Plastic DIP
VT6285HL-35JC		SOJ
VT6286HL-35PC		Plastic DIP
VT6286HL-35JC		SOJ

Note:
Operating temperature range is from 0°C to +70°C.

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AN-138
SPICE-COMPATIBLE OP AMP MACRO-MODELS

APPLICATION NOTE 138

BY MARK ALEXANDER AND DEREK F. BOWERS

There is a definite trend towards a comprehensive circuit-simulation approach. We believe that 75 percent of all installed circuit simulators are being used for system, rather than IC, design. Almost all of these simulators are variants of SPICE. With the growth of the electronics industry, system engineers have come to need increasingly accurate models for an ever larger number of integrated circuits, especially the ubiquitous operational amplifier. However, the increasing speed and complexity of these IC devices has caused problems that were never anticipated by the original developers of SPICE.

Because of the large number of active devices in a typical op amp, circuit simulations that use only transistor-level models can take an unacceptable amount of time, particularly when the circuit contains several op amps. Even simple models of semiconductor devices consume a large amount of computing time because of the multiplicity of nonlinear equations involved. In some cases, the time needed for a complete simulation might exceed the time necessary to build an engineering prototype. Obviously, such a situation would completely defeat the whole purpose of using SPICE.

Fortunately, you can reduce simulation time by using a macro-model that represents the op amp as accurately as possible without using large numbers of transistors or other nonlinear devices. However, it is quite a challenge to design a macro-model that, for all intents and purposes, exactly mimics the real device. For an op amp model to be of real use to the circuit designer, it must not only accommodate all important DC parameters, but also provide a reasonbly close approximation of the AC characteristics over a region that extends well beyond the unity-gain crossover frequency.

EXISTING MACRO-MODELS ARE INADEQUATE

Macro-models for many op amps already exist in the device libraries of several available software simulators. Most of these models are based on the original work done by Graeme Boyle and his colleagues (see Reference 1), who developed their macro-model during the mid-1970s to ease the CPU-time crunch on the already overloaded mainframe computers of the day. Boyle eliminated all but two transistors from his macro-model. The two remaining devices formed the differential-input stage of the op amp; all subsequent stages were implemented with linear controlled sources, passive components, and diodes. The transistors in the input stage were retained because they facilitated the simulation of real-world effects such as bias currents and variation of output dV/dt with the differential input voltage.

Because Boyle's method greatly reduces the number of overall nonlinear elements, the simulation time required per amplifier also decreases substantially. The Boyle structure is certainly an improvement over a full transistor-level simulation, but the structure still has several deficiencies, which prompted the development of the new macro-model. The deficiencies are as follows:

- The Boyle model provides only two poles (and no zeroes) for shaping the frequency response of the complete amplifier – a configuration that is barely adequate for slower op amps, and completely insufficient for today's faster devices.
- All internally generated node voltages are referenced to ground, even if the amplifier is "floated" with respect to ground. This configuration is not representative of the true operation of an op amp – almost none of the available devices provide a ground reference.
- The output-terminal current flows out of a controlled source connected to ground, instead of from the power-supply rails as it would in a real amplifier. This feature completely precludes the simulation of circuits that depend on the amp's output current splitting correctly between the supply rails.

IDEAL ELEMENTS CAN REDUCE COMPLEXITY

The circuit topology of the original Boyle model (Figure 1) was developed using two basic macro-modeling techniques (called simplification and build-up) that proved very useful in the development of the new macro-model as well.

The simplification technique successively reduces the complexity of major internal stages of the op amp by using simple ideal elements to replace real portions of the circuit. Therefore, you can expect a functional block that uses this approach to

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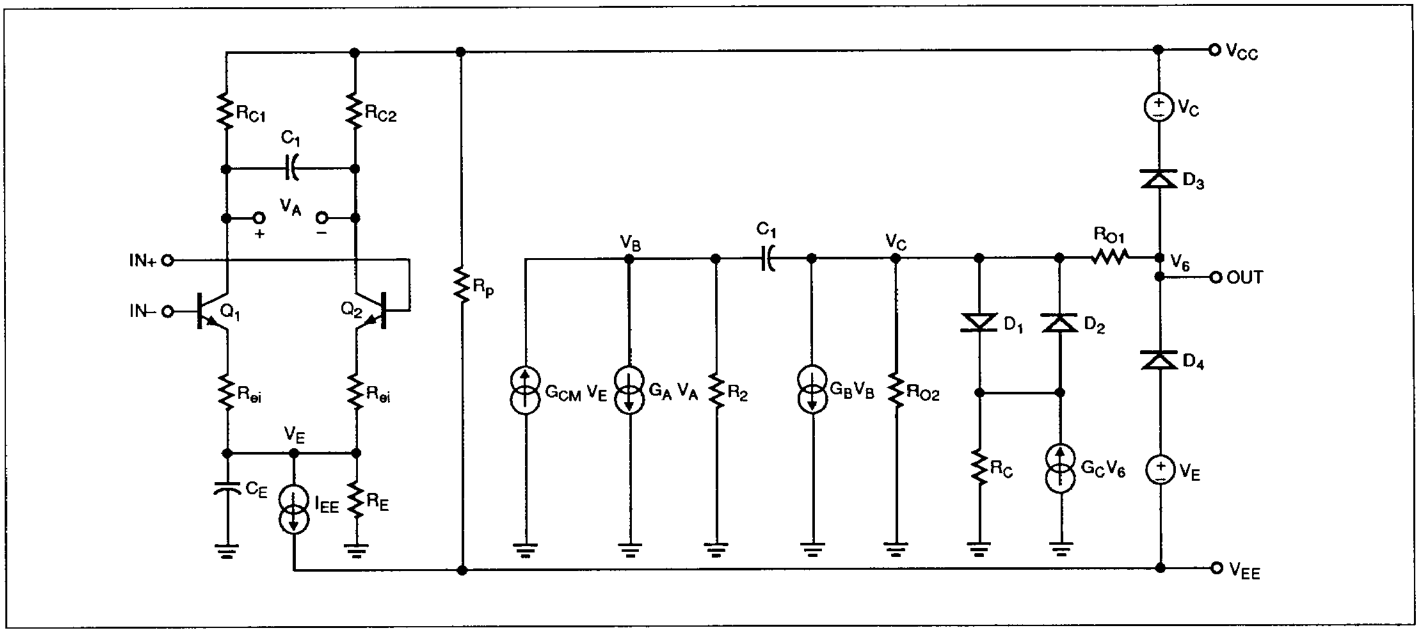

FIGURE 1: *A serious disadvantage to the Boyle op amp macro-model is that all voltages are referenced to ground.*

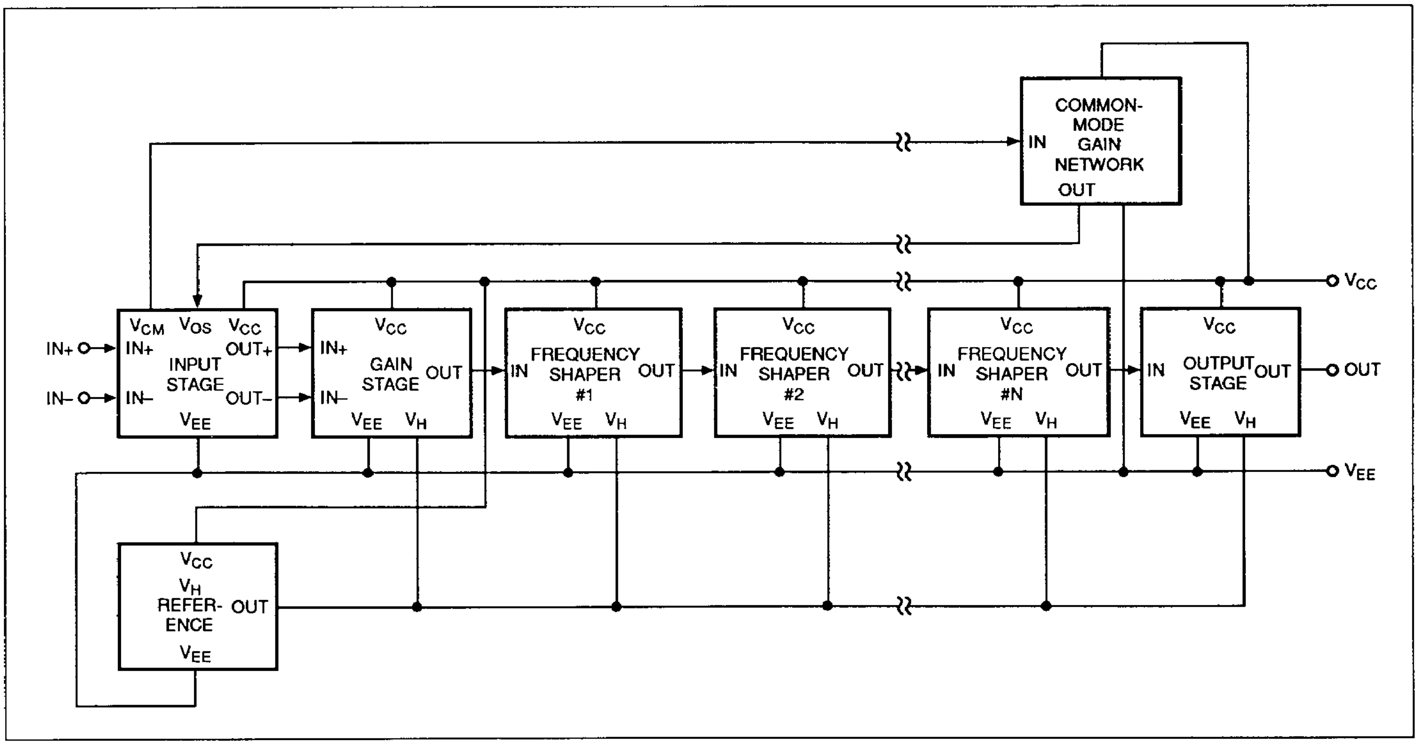

FIGURE 2: *The new op amp macro-model is inherently modular. You can cascade any of the building blocks to obtain any number of poles and zeroes in your op amp design.*

closely resemble the actual circuit. In Figure 1, the model of the input stage is a good example of simplification. The model retains the differential-input characteristics of an emitter-coupled pair, but eliminates any active loads; it replaces the tail-current source with an ideal element; and it assumes the task of generating the second amplifier pole. Adding a single capacitor (C_E) allows the model to provide a pole in this stage, and the reduction in overall component count makes the simulation run faster.