MICROCHIP TC4426A/TC4427A/TC4428A

1.5A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current – 1.5A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability – 1000 pF in 25 nsec (typ.)
- Short Delay Times – 30 nsec (typ.)
- Matched Rise, Fall and Delay Times
- Low Supply Current:
  - With Logic '1' Input – 1 mA
  - With Logic '0' Input – 100 µA
- Low Output Impedance – 7Ω
- Latch-Up Protected: Will Withstand 0.5A Reverse Current
- Input Will Withstand Negative Inputs Up to 5V
- ESD Protected – 4 kV
- Pinouts Same as TC426/TC427/TC428

Applications

- Switch Mode Power Supplies
- Line Drivers
- Pulse Transformer Drive

General Description

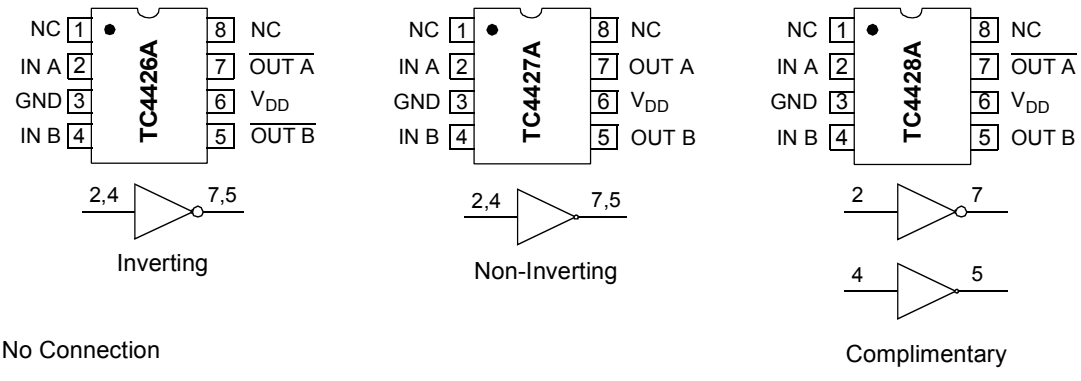
The TC4426A/TC4427A/TC4428A are improved versions of the earlier TC426/TC427/TC428 family of MOSFET drivers. In addition to matched rise and fall times, the TC4426A/TC4427A/TC4428A devices have matched leading and falling edge delay times.

These devices are highly latch-up resistant under any conditions within their power and voltage ratings. They are not subject to damage when up to 5V of noise spiking (of either polarity) occurs on the ground pin. They can accept, without damage or logic upset, up to 500 mA of reverse current (of either polarity) being forced back into their outputs. All terminals are fully protected against electrostatic discharge up to 4 kV.

The TC4426A/TC4427A/TC4428A MOSFET drivers can easily charge/discharge 1000 pF gate capacitances in under 30 nsec and provide low enough impedances in both the 'ON' and 'OFF' states to ensure the MOSFET's intended state will not be affected, even by large transients.

Package Types

8-Pin PDIP/SOIC/CERDIP



NC = No Connection

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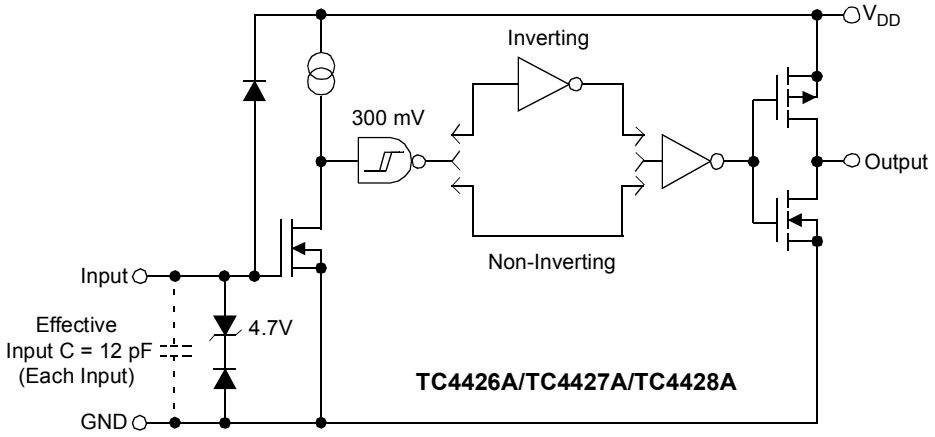
Functional Block Diagram



Note 1: TC4426A has two inverting drivers; TC4427A has two non-inverting drivers; TC4428A has one inverting and one non-inverting driver.

2: Ground any unused driver input.

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage ..... +22V
Input Voltage, IN A or IN B
.....(V_{DD} + 0.3V) to (GND – 5V)
Package Power Dissipation ($T_A \leq 70°C$)
PDIP ..... 730 mW
CERDIP ..... 800 mW
SOIC ..... 470 mW
Package Thermal Resistance
CERDIP $R_{\theta J-A}$ ..... 150°C/W
CERDIP $R_{\theta J-C}$ ..... 50°C/W
PDIP $R_{\theta J-A}$ ..... 125°C/W
PDIP $R_{\theta J-C}$ ..... 42°C/W
SOIC $R_{\theta J-A}$ ..... 155°C/W
SOIC $R_{\theta J-C}$ ..... 45°C/W
Operating Temperature Range
C Version .....0°C to +70°C
E Version ..... -40°C to +85°C
M Version..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Maximum Junction Temperature .....150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, Over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic '1', High Input Voltage	V_{IH}	2.4	—	—	V	
Logic '0', Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1.0 -10	— —	+1.0 +10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	DC Test
Low Output Voltage	V_{OL}	—	—	0.025	V	DC Test
Output Resistance	R_O	— — —	7 7 8	9 10 11	Ω	I_{OUT} = 10 mA, V_{DD} = 18V, T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C
Peak Output Current	I_{PK}	—	1.5	—	A	V_{DD} = 18V
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	0.5	—	A	Duty cycle $\leq$ 2%, t $\leq$ 300 µsec V_{DD} = 18V
Switching Time (Note 1)						
Rise Time	t_R	— — —	25 27 29	35 40 40	nsec.	T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C, **Figure 4-1**.
Fall Time	t_F	— — —	25 27 29	35 40 40	nsec.	T_A = +25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C, **Figure 4-1**.

Note 1: Switching times ensured by design.

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DC CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise noted, Over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Delay Time	t_{D1}	— — —	30 33 35	35 40 45	nsec.	T_A = +25°C 0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C, **Figure 4-1**.
Delay Time	t_{D2}	— — —	30 33 35	35 40 45	nsec.	T_A = +25°C 0°C ≤ T_A ≤ +70°C -40°C ≤ T_A ≤ +85°C, **Figure 4-1**.
Power Supply						
Power Supply Current	I_S	— —	1.0 0.1	2.0 0.2	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs), V_{DD} = 18V

Note 1: Switching times ensured by design.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

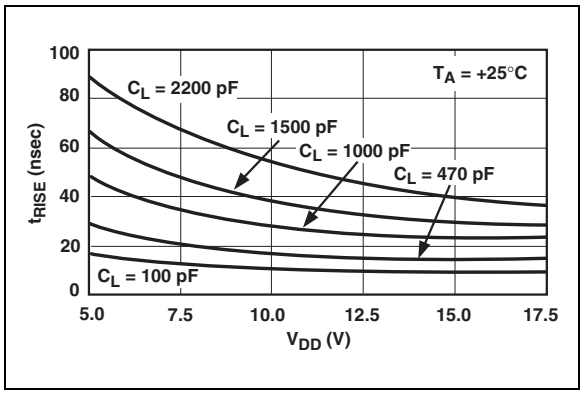

FIGURE 2-1: *Rise Time vs. Supply Voltage.*

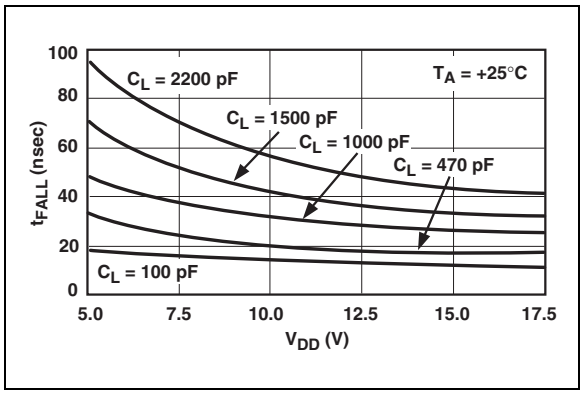

FIGURE 2-4: *Fall Time vs. Supply Voltage.*

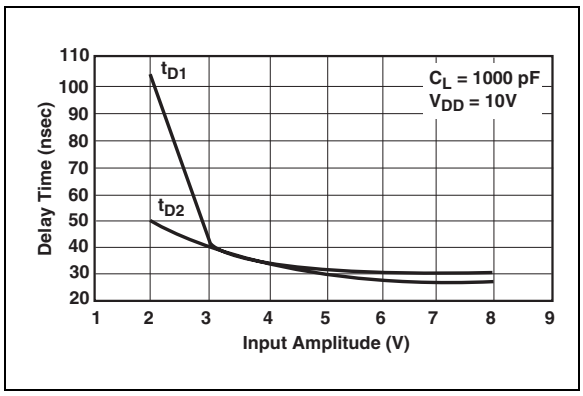

FIGURE 2-2: *Delay Time vs. Input Amplitude.*

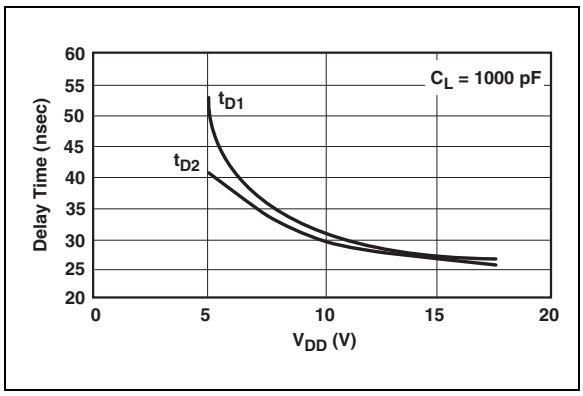

FIGURE 2-5: *Propagation Delay Time vs. Supply Voltage.*

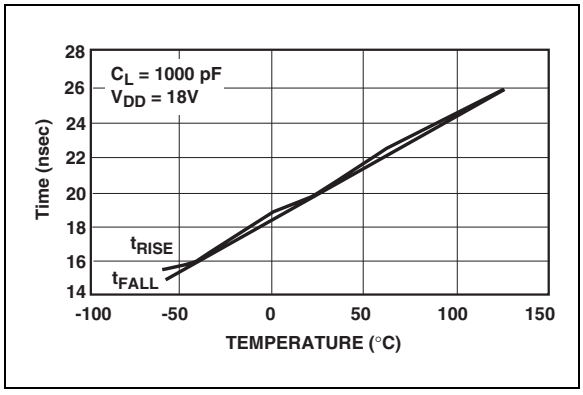

FIGURE 2-3: *Rise and Fall Times vs. Temperature.*

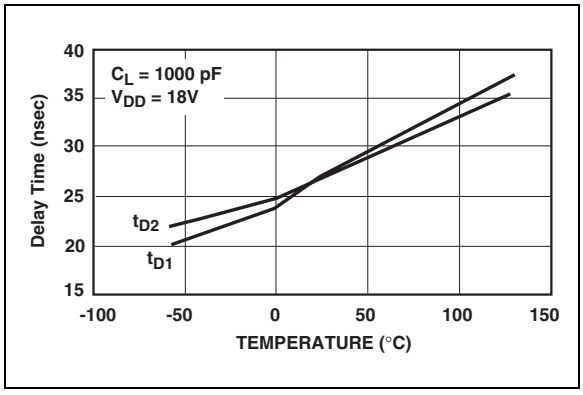

FIGURE 2-6: *Propagation Delay Time vs. Temperature.*

Note: Unless otherwise indicated, over operating temperature range with 4.5V ≤ V_{DD} ≤ 18V.

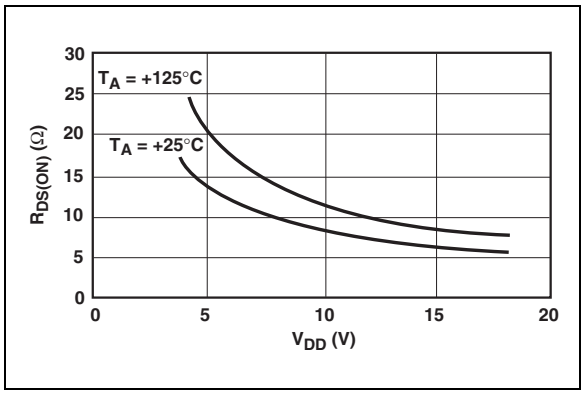

FIGURE 2-7: *High-State Output Resistance.*

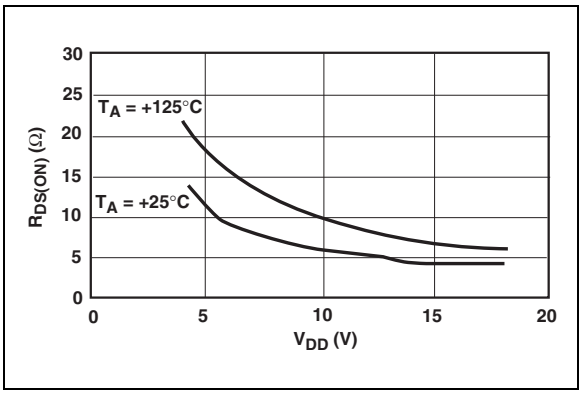

FIGURE 2-10: *Low State Output Resistance.*

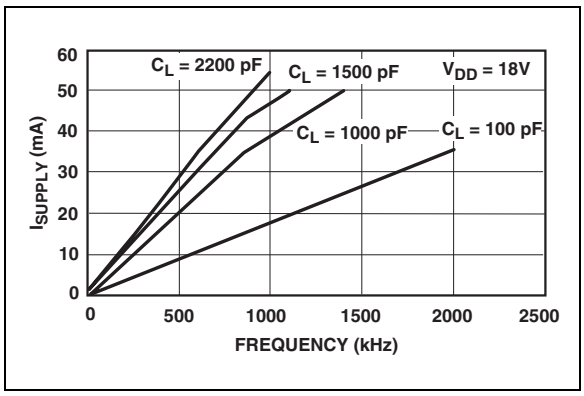

FIGURE 2-8: *Supply Current vs. Frequency.*

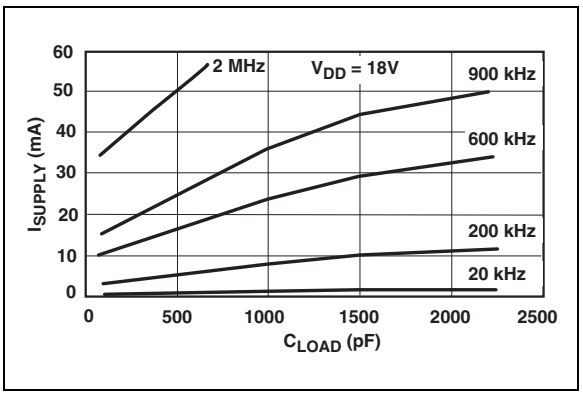

FIGURE 2-11: *Supply Current vs. Capacitive Load.*

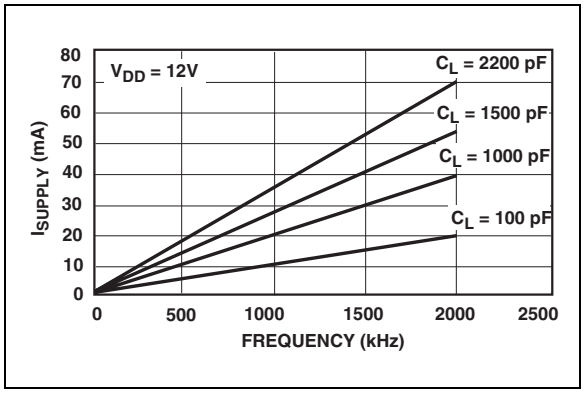

FIGURE 2-9: *Supply Current vs. Frequency.*

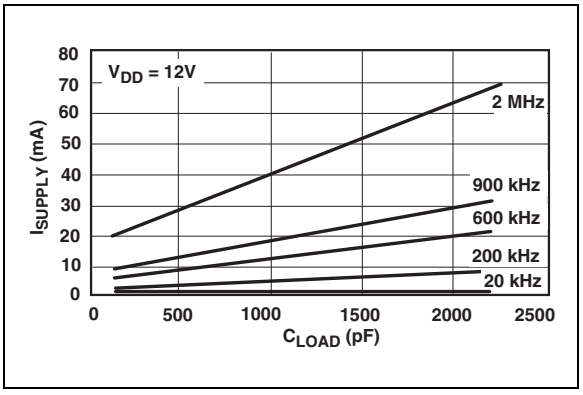

FIGURE 2-12: *Supply Current vs. Capacitive Load.*

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Note: Unless otherwise indicated, over operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.

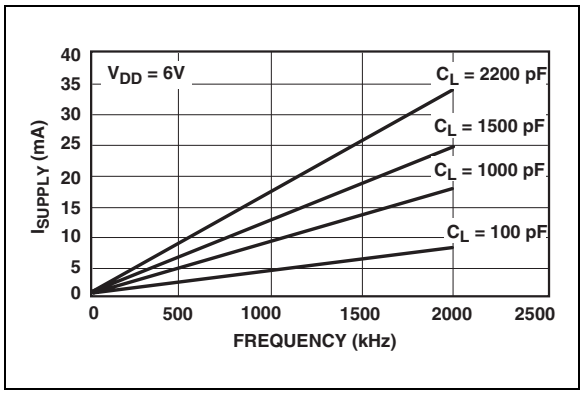

FIGURE 2-13: *Supply Current vs. Frequency.*

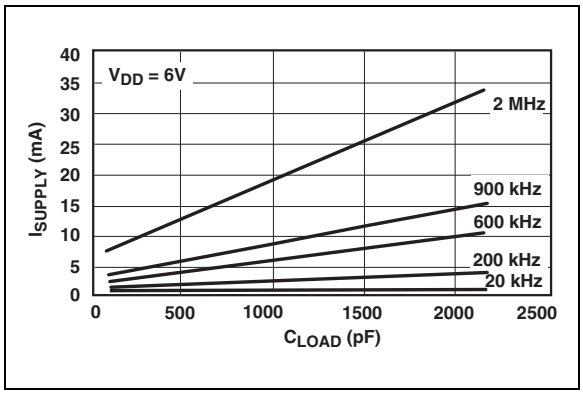

FIGURE 2-15: *Supply Current vs. Capacitive Load.*

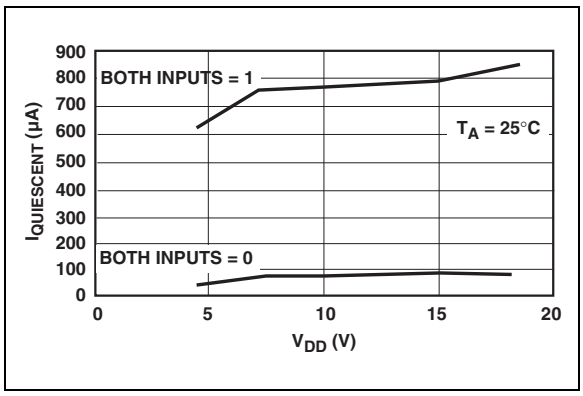

FIGURE 2-14: *Quiescent Supply Current vs. Voltage.*

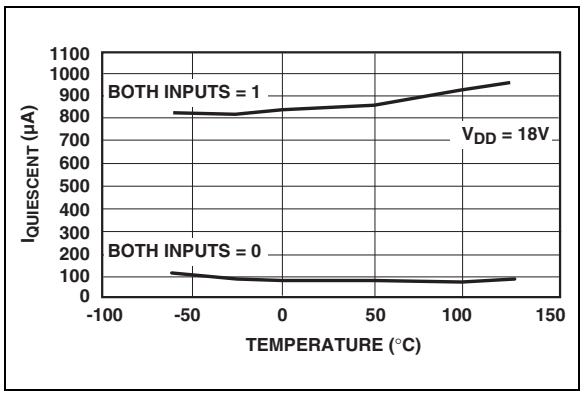

FIGURE 2-16: *Quiescent Supply Current vs. Temperature.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, SOIC, CERDIP)	Symbol	Description
1	NC	No connection
2	IN A	Input A
3	GND	Ground
4	IN B	Input B
5	OUT B	Output B
6	V_{DD}	Supply Input
7	OUT A	Output A
8	NC	No connection

3.1 Inputs A & B

MOSFET driver inputs A & B are high-impedance, TTL/CMOS compatible inputs. These inputs also have 300 mV of hysteresis between the high and low thresholds which prevents output glitching even when the rise and fall time of the input signal is very slow.

3.2 Ground (GND)

Ground terminal.

3.3 Output A & B

MOSFET driver outputs A & B are low-impedance, CMOS push-pull style outputs. The pull down and pull up devices are equal strength, making the rise and fall times equivalent.

3.4 Supply Input (V_{DD})

The V_{DD} input is the bias supply for the MOSFET driver and is rated for 4.5V to 18V with respect to the ground pin. The V_{DD} input should be bypassed with local ceramic capacitors. The value of these capacitors should be chosen based on the capacitive load that is being driven. A value of 1.0 µF is suggested.

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4.0 APPLICATIONS INFORMATION

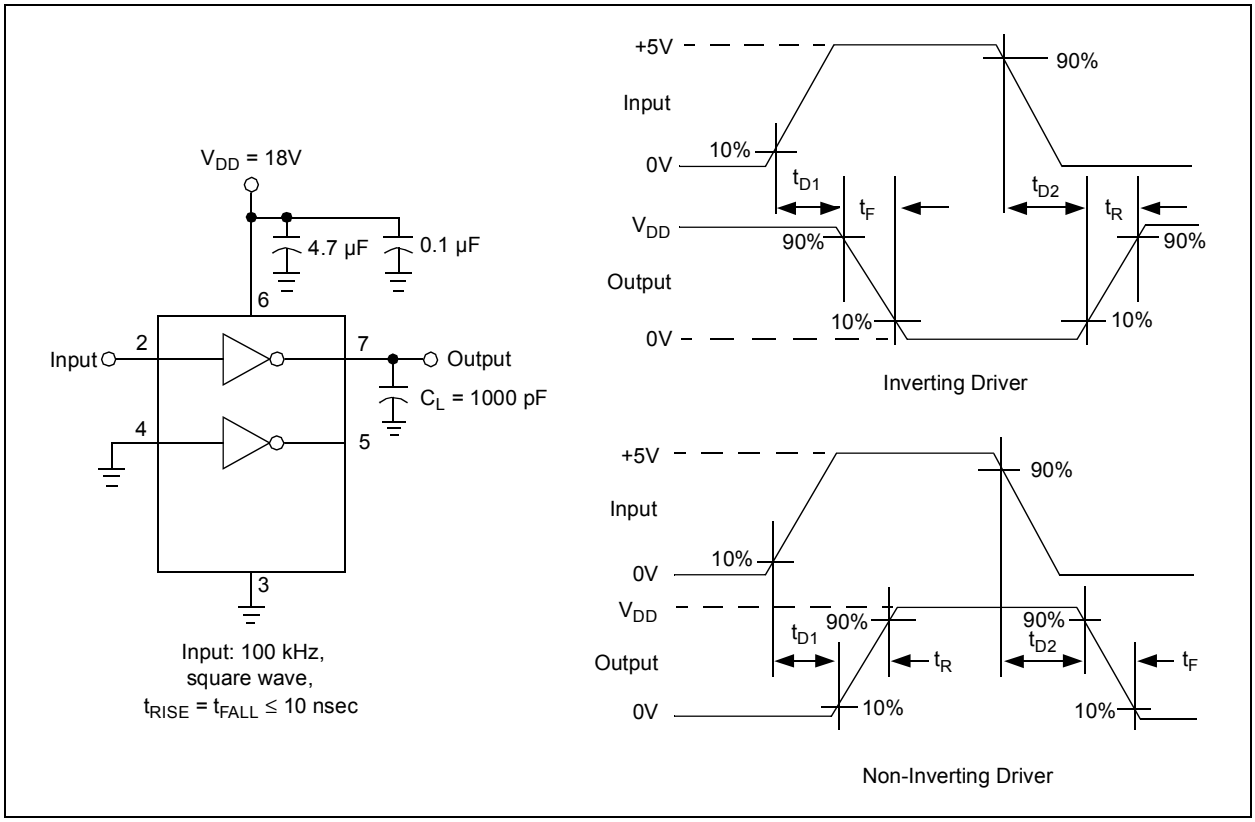
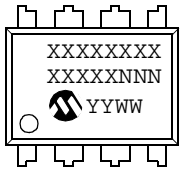


FIGURE 4-1: *Switching Time Test Circuit.*

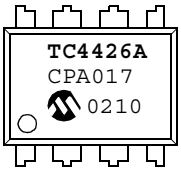
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

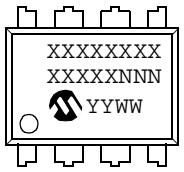
8-Lead PDIP (300 mil)



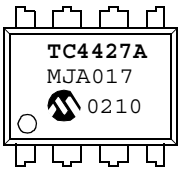
Example:



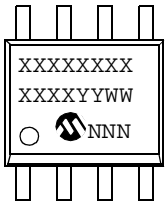
8-Lead CERDIP (300 mil)



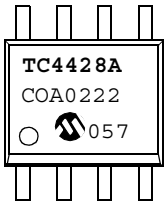
Example:



8-Lead SOIC (150 mil)



Example:



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

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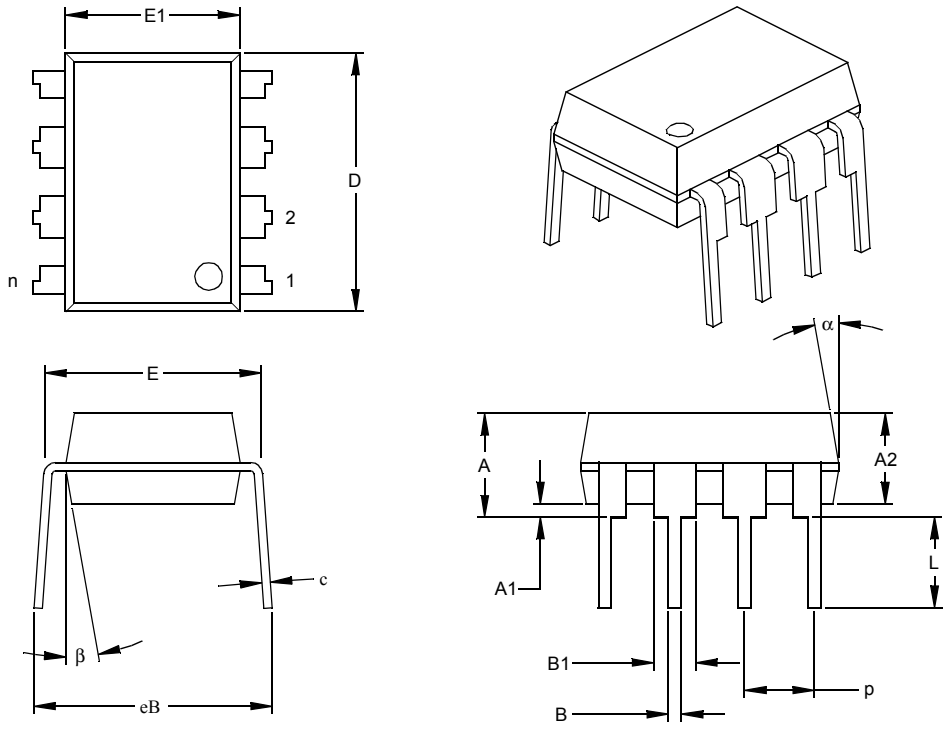
8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

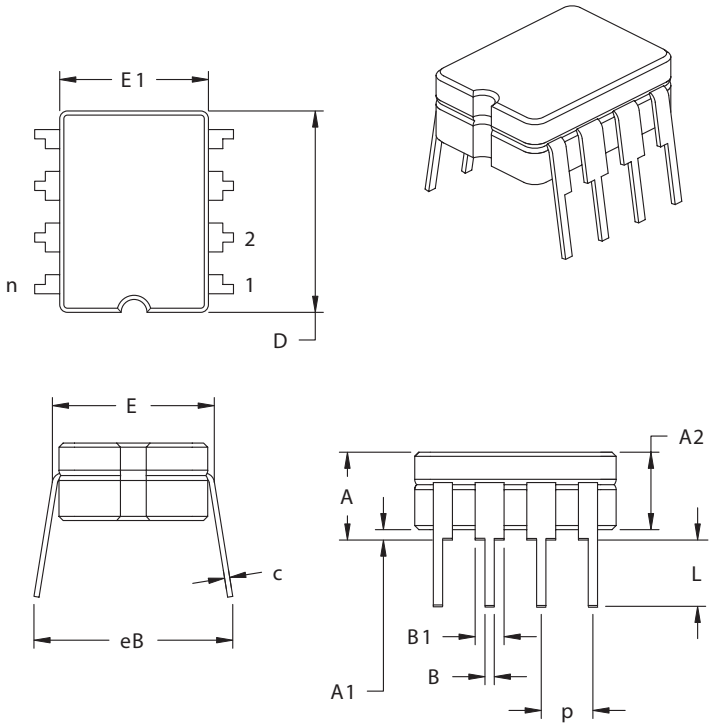


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-018

8-Lead Ceramic Dual In-line – 300 mil (CERDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

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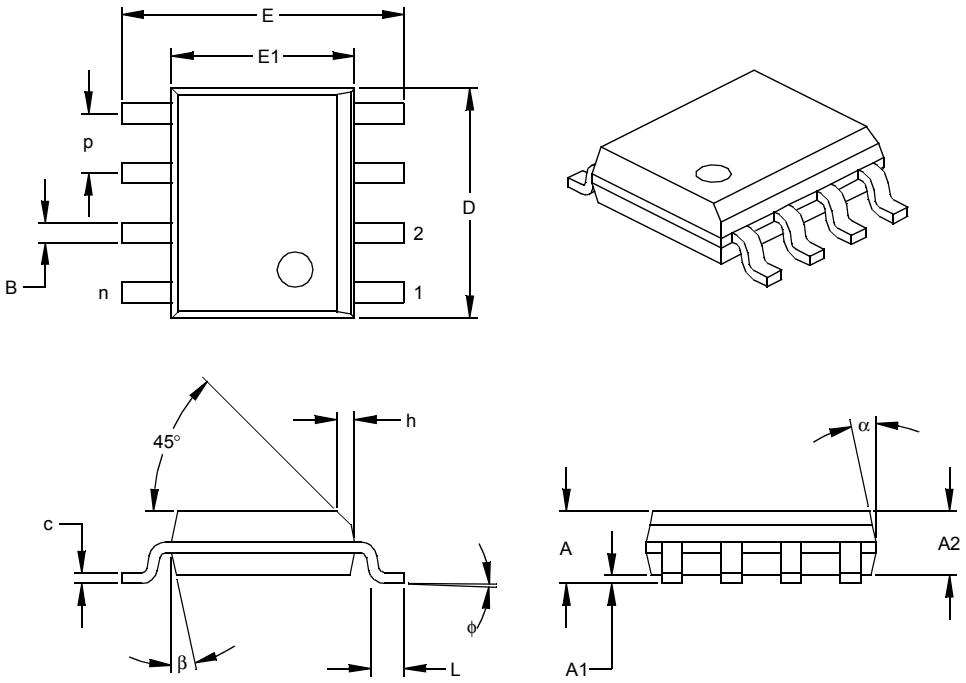
8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-057

NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:	TC4426A: 1.5A Dual MOSFET Driver, Inverting TC4427A: 1.5A Dual MOSFET Driver, Non-Inverting TC4428A: 1.5A Dual MOSFET Driver, Complimentary
Temperature Range:	C = 0°C to +70°C E = -40°C to +85°C M = -55°C to +125°C
Package:	JA = Ceramic Dual In-line (300 mil Body), 8-lead OA = Plastic SOIC, (150 mil Body), 8-lead OA713 = Plastic SOIC, (150 mil Body), 8-lead (Tape and Reel) PA = Plastic DIP (300 mil Body), 8-lead

Examples:

a) TC4426ACOA: 1.5A Dual MOSFET driver, SOIC package, 0°C to +70°C.

b) TC4426AEOA: 1.5A Dual MOSFET driver, SOIC package, -40°C to +85°C.

a) TC4427ACPA: 1.5A Dual MOSFET driver, PDIP package, 0°C to +70°C.

b) TC4427AEPA: 1.5A Dual MOSFET driver, PDIP package, -40°C to +85°C.

a) TC4428AMJA: 1.5A Dual MOSFET driver, CDIP package, -55°C to +125°C.

b) TC4428ACOA713: 1.5A Dual MOSFET driver, Tape and Reel, SOIC package, 0°C to +70°C.

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WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: http://www.microchip.com

Rocky Mountain
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-4338

Atlanta
3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034 Fax: 770-640-0307

Boston
2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago
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Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas
4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit
Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo
2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles
18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

San Jose
Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto
6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia
Microchip Technology Australia Pty Ltd
Marketing Support Division
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing
Microchip Technology Consulting (Shanghai) Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu
Microchip Technology Consulting (Shanghai) Co., Ltd., Chengdu Liaison Office
Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou
Microchip Technology Consulting (Shanghai) Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Hong Kong SAR
Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

China - Shanghai
Microchip Technology Consulting (Shanghai) Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen
Microchip Technology Consulting (Shanghai) Co., Ltd., Shenzhen Liaison Office
Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380 Fax: 86-755-82966626

China - Qingdao
Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India
Microchip Technology Inc.
India Liaison Office
Marketing Support Division
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan
Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471- 6166 Fax: 81-45-471-6122

Korea
Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore
Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan
Microchip Technology (Barbados) Inc., Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria
Microchip Technology Austria GmbH
Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark
Microchip Technology Nordic ApS
Regus Business Centre
Lautrup hoj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France
Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - ler Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany
Microchip Technology GmbH
Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-089-627-144-100
Fax: 49-089-627-144-44

Italy
Microchip Technology SRL
Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611 Fax: 39-0331-466781

United Kingdom
Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

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