

ZN527/ZN528

DUAL 8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

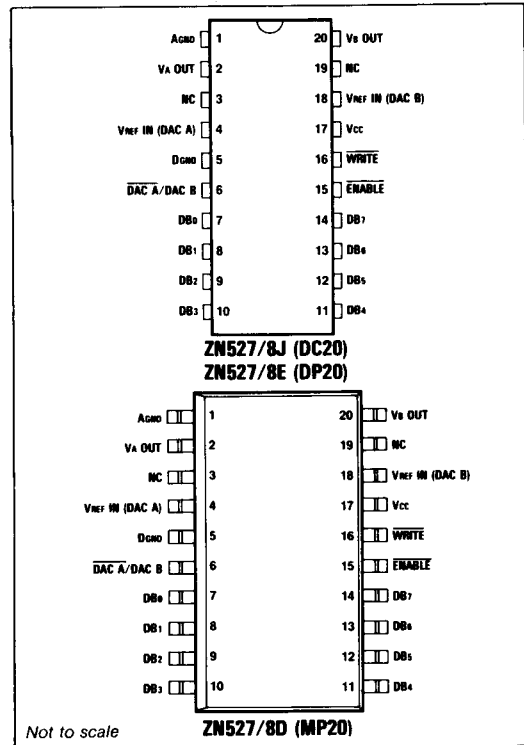
The ZN527 and ZN528 are monolithic dual 8-bit DACs designed to be easily interfaced to microprocessors. Integrated on-chip are two 8-bit DAC's, separate V_{REF} inputs and data latches for each DAC. A consequence of the two DAC's being fabricated on the same chip is excellent, inherent, DAC to DAC matching.

FEATURES

- 800ns Voltage Settling Time
- Monotonic over Full Temperature Range
- Single +5V Supply
- Excellent DAC to DAC Matching
- Separate V_{REF} IN for each DAC
- Commercial and Military Temperature Ranges

ORDERING INFORMATION

Device type	Linearity error (LSB)	Operating temperature	Package
ZN527E	± 1	-40°C to +85°C	DP20
ZN528E	$\pm \frac{1}{2}$	-40°C to +85°C	DP20
ZN527D	± 1	-40°C to +85°C	MP20
ZN528D	$\pm \frac{1}{2}$	-40°C to +85°C	MP20
ZN527J	± 1	-55°C to +125°C	DC20
ZN528J	$\pm \frac{1}{2}$	-55°C to +125°C	DC20



Not to scale

Pin connections - top view

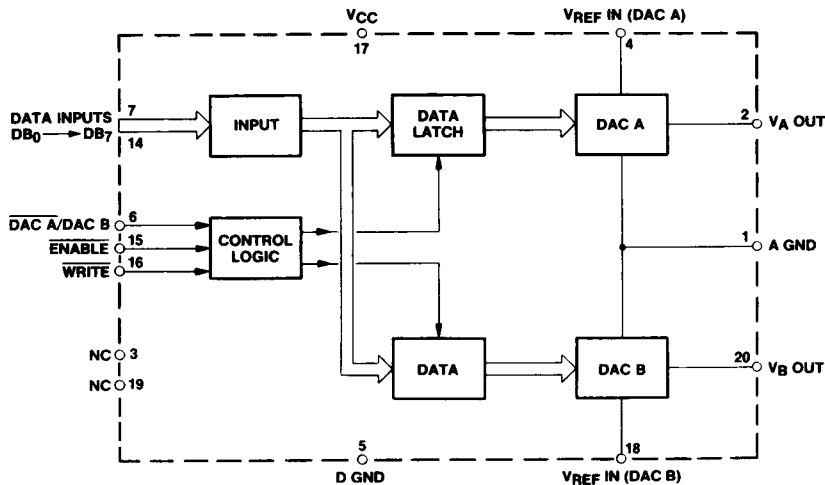


Fig.1 System diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage V _{CC}	+7V	ZN527/8J	-55°C to 125°C
Max. voltage, logic and V _{REF} input	+V _{CC}	Storage temperature range	-55°C to 125°C
Operating temperature range		Analog ground to digital ground	±200mV
ZN527/8E and ZN527/8D	-40°C to +85°C		

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
ZN528					
Linearity error			±0.5	LSB	
Differential linearity error			±0.75	LSB	
ZN527					
Linearity error			±1.0	LSB	
Differential linearity error			±0.75	LSB	
All types					
Linearity error TC		±3		ppm/°C	
Differential non-linearity TC		±6		ppm/°C	
Offset voltage		2	5	mV	All bits OFF
Offset voltage TC		±3		ppm/°C	
Full scale output	2.545	2.550	2.555	V	External reference V _{REF IN} = 2.560V, all bits ON
Full scale output TC		2		ppm/°C	
Analog output resistance		4		kΩ	
External reference voltage	0		3.0	V	
Settling time to 0.5 LSB		800		ns	1 LSB major transition (Note 1)
		1.25		μs	All bits ON to OFF or OFF to ON (Note 1)
Operating temperature range:					
ZN508E and ZN508D	-40		85	°C	
ZN508J	-55		125	°C	
Supply voltage (V _{CC})	4.5	5.0	5.5	V	
Supply current		36		mA	
Power consumption		180		mW	
DC supply rejection		-57		dB	ΔV _{CC} = 250μV p-p f ≤ 50kHz
Digital to analog glitch impulse				nV-s	00000000 11111111
Channel to channel isolation					
V _{REF A} to Out B		-82		dB	} f ≤ 50kHz
V _{REF B} to Out A		-82		dB	
Internal voltage reference					
Output voltage		2.5		V	
Slope impedance		1		Ω	
V _{REF OUT} TC		50		ppm/°C	
Reference current	1		15	mA	
Logic					
(over specified operating temperature range)					
High level input voltage V _{IH}	2.0			V	
Low level input voltage V _{IL}			0.8	V	
High level input current I _{IH}			20	μA	V _{IN} = 2.4, V _{CC} = 5.5V
			320	μA	V _{IN} = 5.5, V _{CC} = 5.5V
Low level input current I _{IL}			-310	μA	V _{IN} = 0.4V, V _{CC} = 5.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Switching characteristics					
Chip select to write set up time t_{CS}	150			ns	
Chip select to write hold time, T_{CH}	10			ns	
DAC select to write set up time t_{AS}	150			ns	
DAC select to write hold time t_{AH}	10			ns	
Data valid to write set up time t_{DS}	100			ns	
Data valid to write hold time t_{DH}	50			ns	
Write pulse width t_{WR}	150			ns	

NOTE

1. $R_L = 10$ Megohms $C_L = 10\mu F$.

D-A CONVERTER

The converters are of the voltage switching type and use an R-2R ladder network as shown in Fig.2. Each 2R element is connected to 0V or $V_{REF IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

where n is the digital input to the D-A from the data latch. V_{OS} is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of V_{OS} is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low ($\pm 6\mu V/^\circ C$) the effect on accuracy is negligible.

$$\text{Analog output} = \frac{n}{256} (V_{REF IN} - V_{OS}) + V_{OS}$$

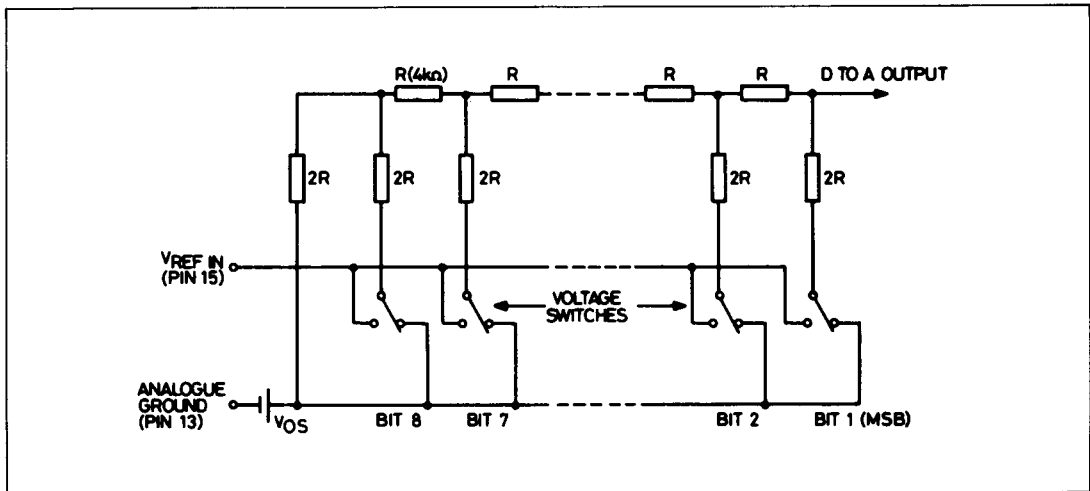


Fig.2 The R-2R ladder network

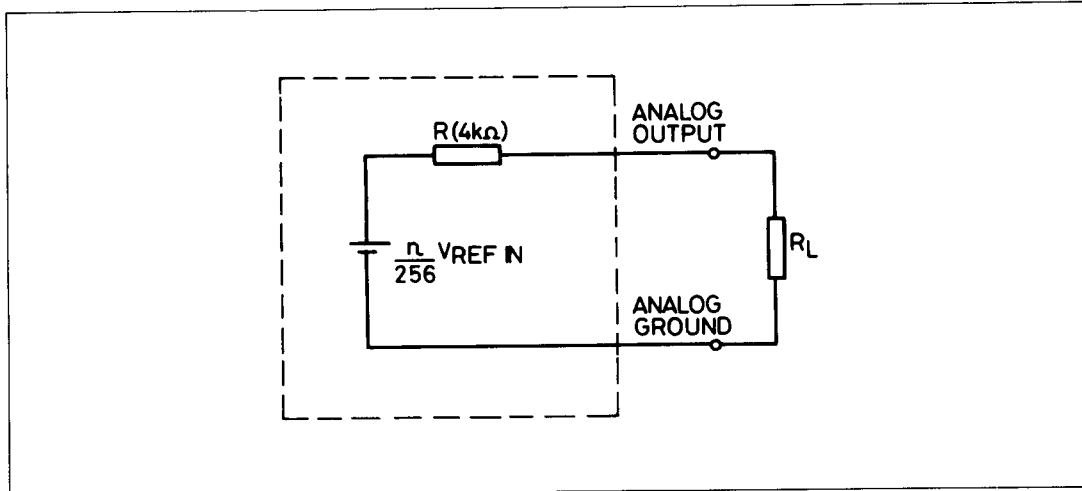


Fig.3 Analog output equivalent circuit

Fig.3 shows an equivalent circuit of the outputs (ignoring V_{OS}). The output resistance R has a temperature coefficient of $+0.2\%$ per $^{\circ}C$.

The gain drift due to this is $\frac{0.2R}{R + R_L}$ % per $^{\circ}C$

R_L should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400k\Omega$ then the gain drift due to the TC of R for a $100^{\circ}C$ change in ambient temperature will be less than 0.2% . Alternatively the ZN527/8 outputs can be buffered by amplifiers (see Operating Notes).

REFERENCE

External Reference

Should an external reference voltage be connected to $V_{REF IN}$, the slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF IN}$ can be varied from 0 to $+3V$ for ratiometric operation. The ZN527/8 is guaranteed monotonic for $V_{REF IN}$ above $2V$.

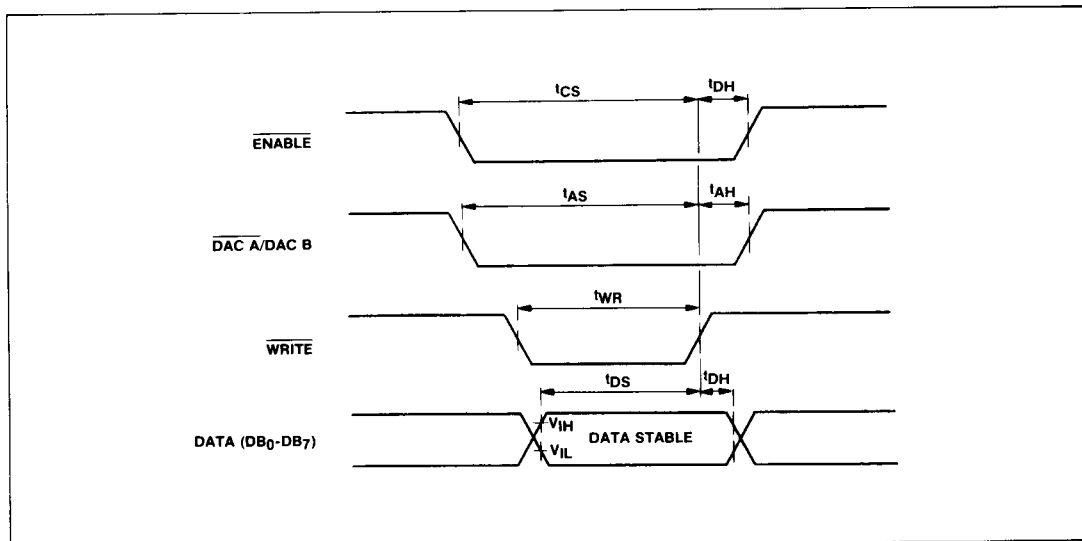


Fig.4 Logic timing diagram

LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. Both DAC A and DAC B share an internal data bus and an 8-bit input port. The DAC to be loaded with new data is chosen by DAC A/DAC B select pin; DAC A when the input is low and DAC B when the input is high. When $\overline{\text{ENABLE}}$ and $\overline{\text{WRITE}}$ are both low the DAC selected is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data presented to the input port. The data is then latched when either $\overline{\text{ENABLE}}$ or $\overline{\text{WRITE}}$ are taken high.

DAC A/DAC B	CS	WR	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

Table 1 Logic truth table

OPERATING NOTES

In some applications the standard 0 to $V_{\text{REF IN}}$ output voltage range and drive capability are not suitable, and other output ranges, both unipolar and bipolar are required.

To maintain flexibility two types of operational amplifier are illustrated; the industry standard 741 and a low cost pin-compatible alternative with a JFET input, the LF351. The LF351 features a high slew rate of $13\text{V}/\mu\text{s}$, which gives a faster potential settling time than the 741. To keep drift to a minimum when using the 741, the external range setting resistors are calculated to match them to the $4\text{k}\Omega$ ladder output impedance. This is not a consideration with the LF351, as the input offset current change with temperature is negligible for the impedances concerned. The resistor values for the LF351 were chosen to keep the output ringing to a minimum; a problem sometimes encountered with high slew rate op-amps. It is only the relative and not the absolute values of these resistors which set the range, and therefore can be changed as long as their ratios remain the same.

Unipolar Operation

The general scheme for unipolar operation is shown in Fig.4 and is suitable for amplifiers with input bias currents less than $1.5\mu\text{A}$.

The resulting full scale range is given by

$$V_{\text{OUT FS}} = 1 + \frac{R1}{R2} (V_{\text{REF IN}} - 1 \text{ LSB})$$

$$= G (V_{\text{REF IN}} - 1 \text{ LSB})$$

The impedance at the inverting input is $R1/R2$ and for low drift with temperature (741 only), this parallel combination should be equal to the ladder resistance ($4\text{k}\Omega$).

The required nominal values of $R1$ and $R2$ are therefore given by $R1 = 4\text{Gk}\Omega$ and $R2 = 4\text{G}/(\text{G}-1)\text{k}\Omega$.

Using these relationships a table of nominal resistance values for $R1$ and $R2$ can be constructed for $V_{\text{REF IN}} = 2.5\text{V}$ (Table 2). For gain setting $R1$ is adjusted about its nominal value. Practical circuit realisations for $+5\text{V}$ and $+10\text{V}$ output ranges are given in Figs. 6 and 7.

Output range	G	R1	R2
+5V	2	8kΩ	8kΩ
+10V	4	16kΩ	5.33kΩ

Table 2 Nominal values for R1 and R2

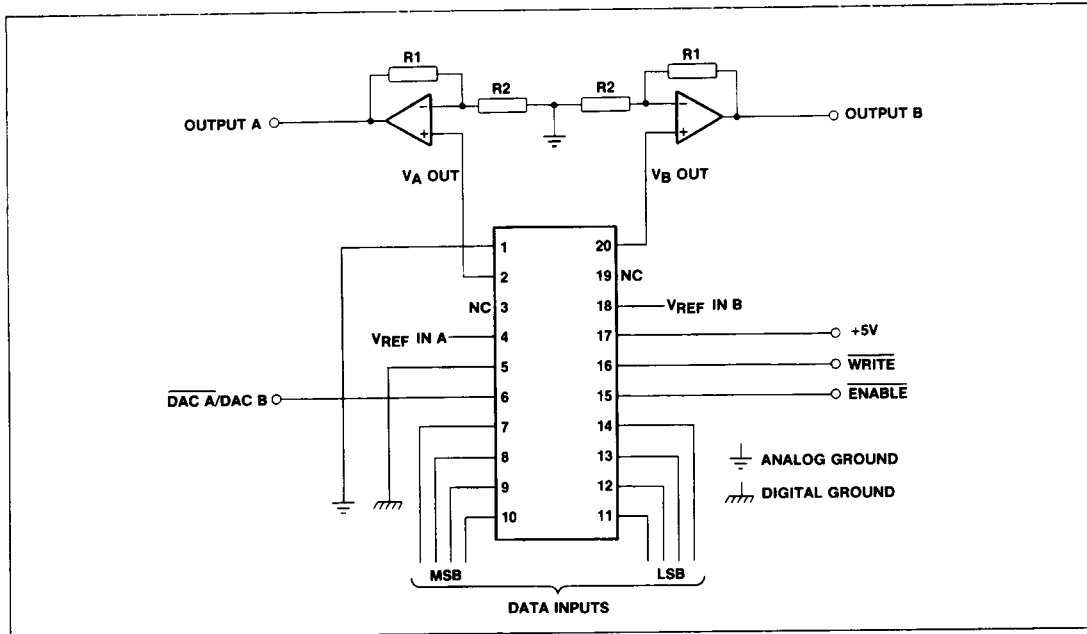


Fig.5 Unipolar operation - basic circuit

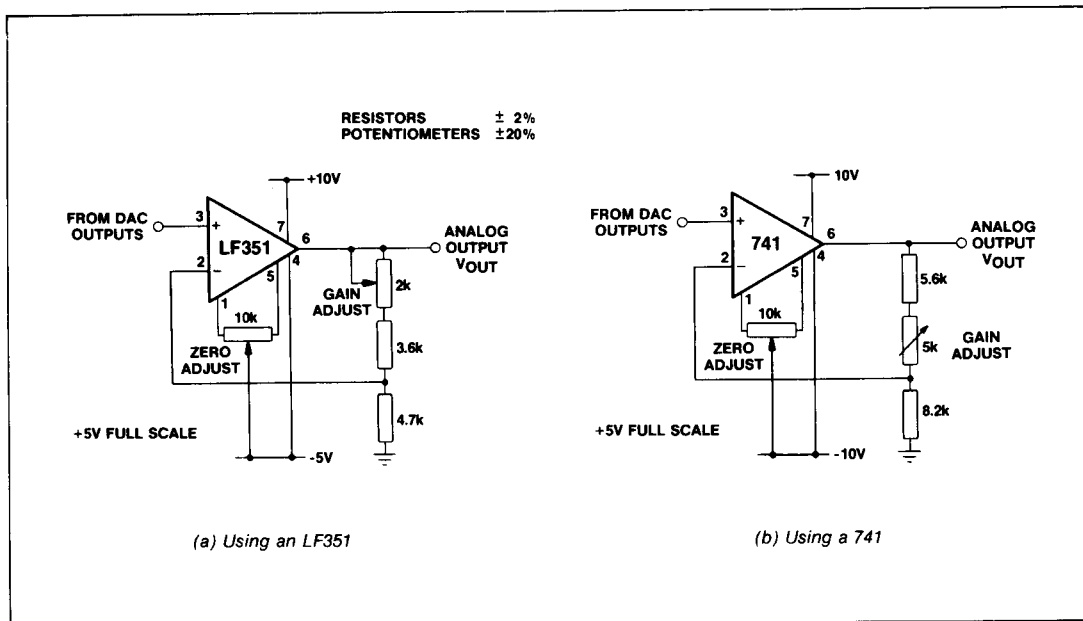


Fig.6 +5V full scale unipolar operation - component values

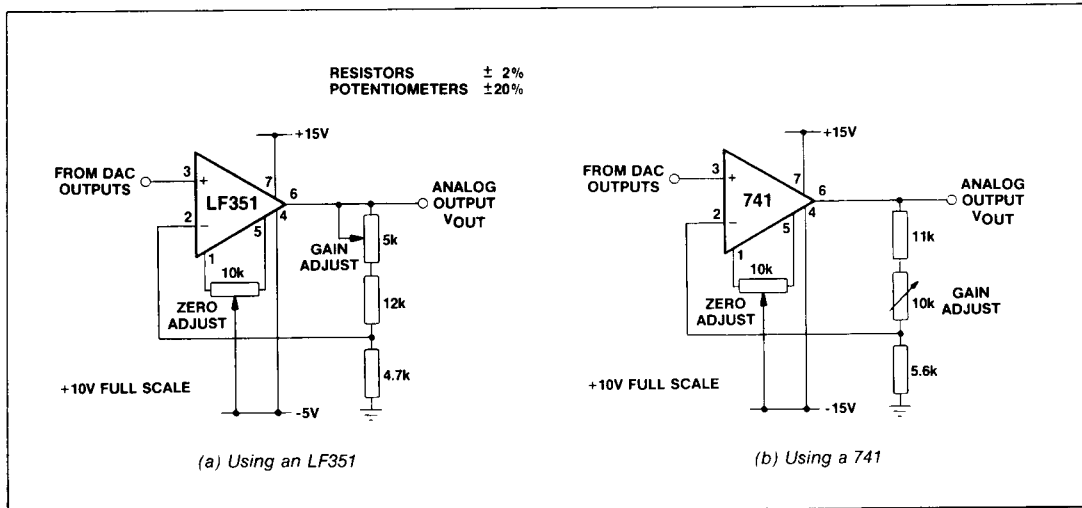


Fig.7 +10V full scale unipolar operation - component values

Unipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until $V_{\text{OUT}} = 0.0000V$.
2. Set all bit ON (high) and adjust gain until $V_{\text{OUT}} = FS - 1 \text{ LSB}$.

Output range, +FS	LSB	FS - 1 LSB
+ 5V	19.5mV	4.9805V
+10V	39.1mV	9.9609V

$$1 \text{ LSB} = \frac{FS}{256}$$

Table 3 Unipolar setting up points

Input code (Binary)	Analog output (nominal value)
11111111	FS - 1 LSB
11111110	FS - 2 LSB
11000000	$\frac{3}{4}$ FS
10000001	$\frac{1}{2}$ FS + 1 LSB
10000000	$\frac{1}{2}$ FS
01111111	$\frac{1}{2}$ FS - 1 LSB
01000000	$\frac{1}{4}$ FS
00000001	1 LSB
00000000	0

Table 4 Unipolar logic coding

Bipolar Operation

For bipolar operation the output from the ZN527/8 is offset by half full scale by connecting a resistor R3 between $V_{\text{REF IN}}$ and the inverting input of the buffer amplifier (Fig.8).

When the digital input to the ZN527/8 is zero and the analog output is zero and the amplifier output should be - full scale. An input of all ones to the D-A will give a ZN527/8 output of $V_{\text{REF IN}} - 1 \text{ LSB}$ and an amplifier output of + full scale. When using the 741, the parallel combination of R1, R2 and R3 should match the 4kΩ ladder resistance.

The nominal values of R1, R2 and R3 which meet these conditions are given by

$$R1 = 8Gk\Omega, R2 = 8G/(G-1)k\Omega \text{ and } R3 = 8k\Omega,$$

where the resultant output range is $\pm G V_{\text{REF IN}}$.

A binary output range of $\pm V_{\text{REF IN}}$ (which corresponds to the basic unipolar range 0 to $V_{\text{REF IN}}$) is obtained if $R1 = R3 = 8k\Omega$ and $R2 = \infty$.

Assuming that $V_{\text{REF IN}} = 2.5V$ the nominal values of resistors for $\pm 5V$ and $\pm 10V$ output ranges are given in Table 5.

Output range	G	R1	R2	R3
+ 5V	2	16kΩ	16kΩ	8kΩ
$\pm 10V$	4	32kΩ	10.66kΩ	8kΩ

Table 5

Minus full scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full scale (gain) is set by adjusting R2 relative to R1.

Practical circuit realisations are given in Figs. 9 and 10. Note that in the $\pm 5V$ case (741 only), R3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to give a more symmetrical range of adjustment using standard potentiometers.

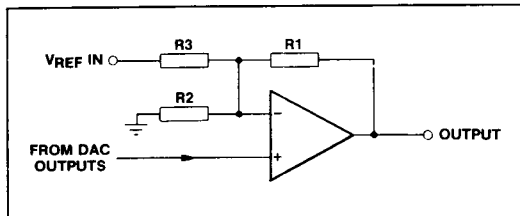


Fig.8 Bipolar operation

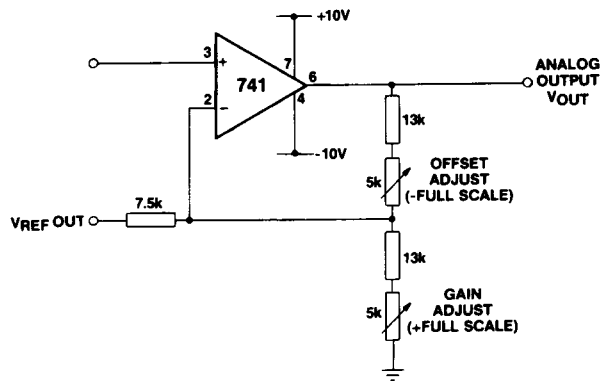
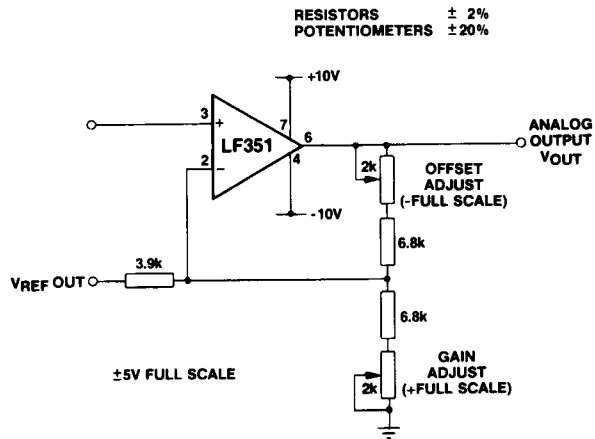


Fig.9 $\pm 5V$ full scale bipolar operation - component values

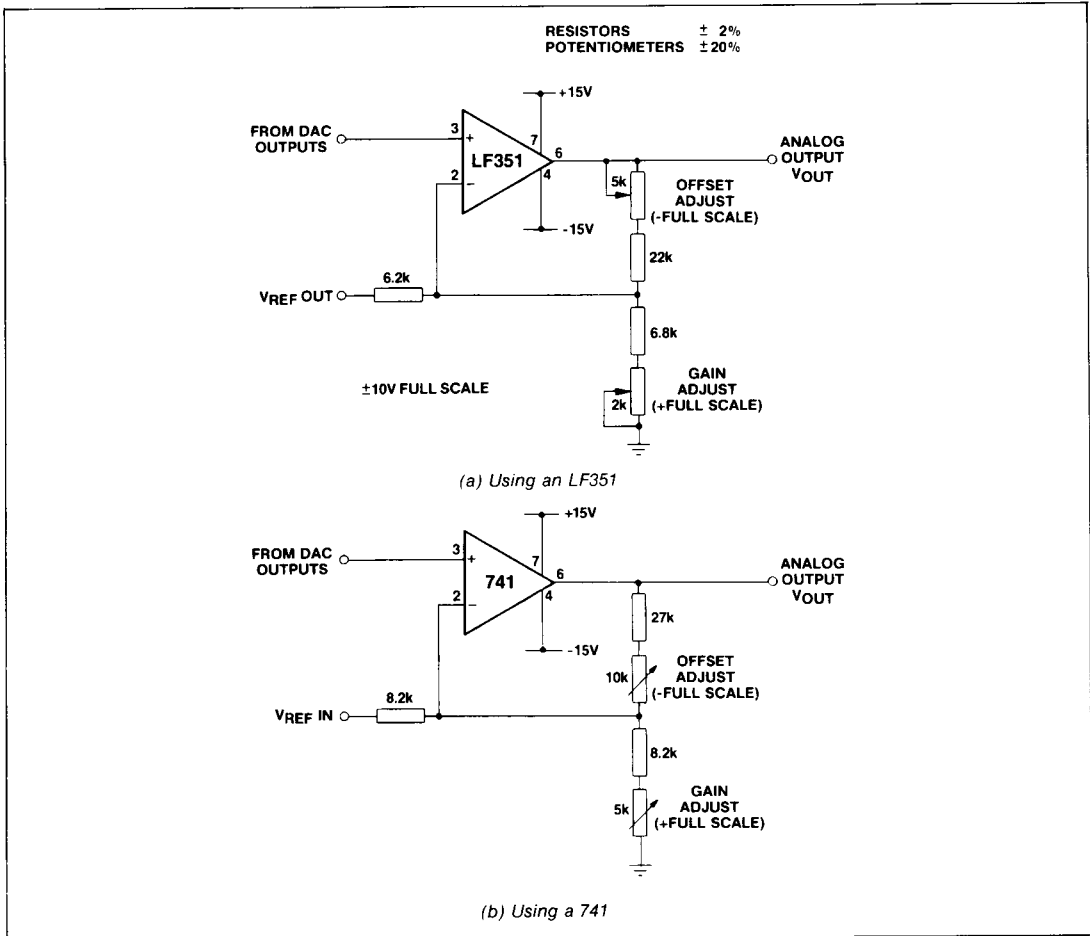


Fig.10 $\pm 10V$ full scale bipolar operation - component values

Bipolar Adjustment Procedure

1. Set all bits to OFF (low) with ENABLE low and adjust offset until the amplifier output reads - full scale.
2. Set all bits ON (high) and adjust gain until the amplifier output reads + (full scale - 1 LSB).

Input range, $\pm FS$	LSB	-FS	$+(FS - 1 LSB)$
$\pm 5V$	39.1mV	-5.0000V	+4.9609V
$\pm 10V$	78.1mV	-10.0000V	+9.9219V

1 LSB = $\frac{2FS}{256}$

Table 6 Bipolar setting up points

Input code (offset binary)	Analog output (nominal value)
11111111	$+(FS - 1 LSB)$
11111110	$+(FS - 2 LSB)$
11000000	$+\frac{1}{2} FS$
10000001	+1 LSB
10000000	0
01111111	-1 LSB
01000000	$-\frac{1}{2} FS$
00000001	$-(FS - 1 LSB)$
00000000	-FS

Table 7 Bipolar logic coding