TC74HCT245AP/AF/AFW
TC74HCT640AP/AF
TC74HCT643AP/AF/AFW

OCTAL BUS BUFFER

TC74HCT245AP/AF/AFW	3-STATE, NON-INVERTING
TC74HCT640AP/AF	3-STATE, INVERTING
TC74HCT643AP/AF/AFW	3-STATE, INVERTING AND NON-INVERTING

The TC74HCT245A, HCT640A and HCT643A are high speed CMOS OCTAL BUS TRANSCEIVERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

Their inputs are compatible with TTL, NMOS, and CMOS output voltage levels.

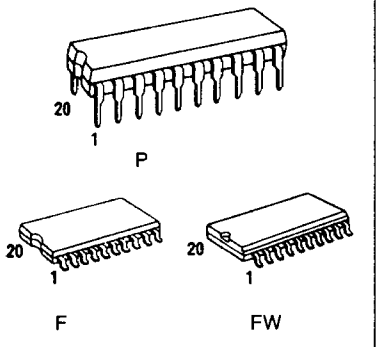
They are intended for two-way asynchronous communication between data busses. The direction of date transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed ····· t_{pd}=10ns(typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at TA=25℃
- Combatible with TTL outputs ····· V_{IL}=0.8V(Max.), V_{IH}=2.0(Min.)
- Wide Interfacing ability ····· LSTTL, NMOS, CMOS
- Output Drive Capability ····· 15 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=6mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \fallingdotseq t_{pHL}$
- Pin and Function Compatible with 74LS245,640,643

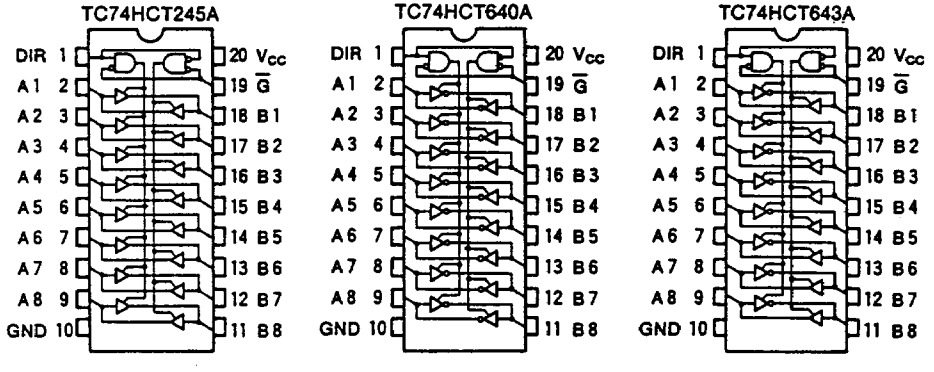


APPLICATION NOTES

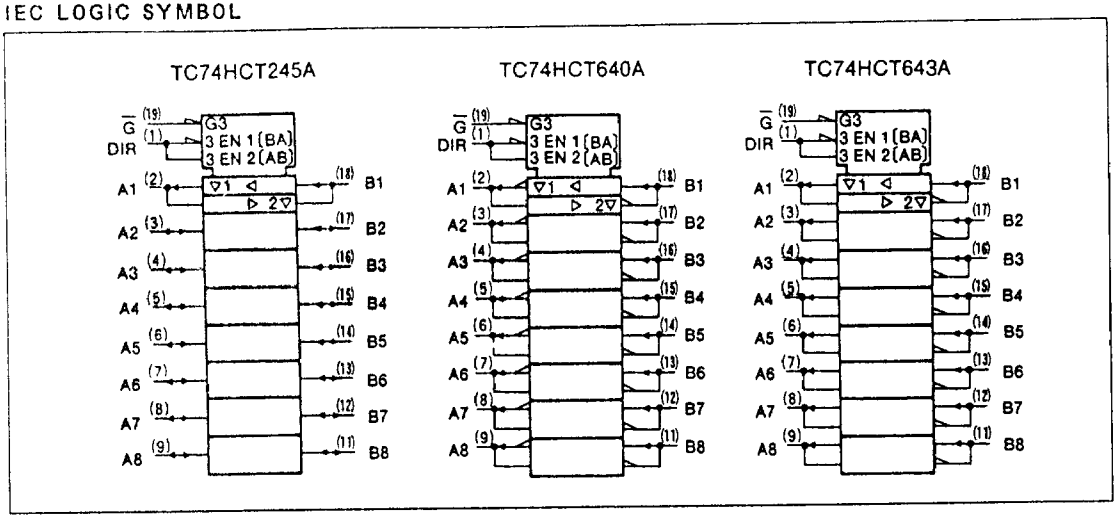
1) Do not apply a signal to any bus terminal when it is the output mode. Damage may result.

2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or down resistors or bus terminator IC's such as the TOSHIBA TC40117BP.

PIN ASSIGNMENT(TOP VIEW)



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		FUNCTION		OUTPUTS		
$\overline{G}$	DIR	A BUS	B BUS	HCT245A	HCT640A	HCT643A
L	L	OUTPUT	INPUT	A=B	A=$\overline{B}$	A=B
L	H	INPUT	OUTPUT	B=A	B=$\overline{A}$	B=$\overline{A}$
H	X	High Impedance		Z	Z	Z

X : "H" or "L"
Z : High Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	−65 ~150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	Topr	−40~85	℃
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High−Level Input Voltage	V_{IH}			4.5 ~ 5.5	2.0	−	−	2.0	−	V
Low−Level Input Voltage	V_{IL}			4.5 ~ 5.5	−	−	0.8	−	0.8	V
High−Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} =−6 mA	4.5	4.18	4.31	−	4.13	−	
Low−Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} =6 mA	4.5	−	0.17	0.26	−	0.33	
3−State Output Off−State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL}; V_{OUT} = V_{CC} or GND		5.5	−	−	±0.5	−	±5.0	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		5.5	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	−	−	4.0	−	40.0	μA
	ΔI_{CC}	Per input: V_{IN} = 0.5V or 2.4V; Other input: V_{CC} or GND		5.5	−	−	2.0	−	2.9	mA

AC ELECTRICAL CHARACTERISTICS(Input $t_r=t_f=6ns$)

PARAMETER	SYMBOL	TEST CONDITION	CL	V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
Output Transition Time	t_{TLH}		50	4.5	−	7	12	−	15	ns
	t_{THL}			5.5	−	6	11	−	14	
Propagation Delay Time	t_{pLH}		50	4.5	−	13	22	−	28	
				5.5	−	11	20	−	25	
	t_{pHL}		150	4.5	−	18	30	−	38	
				5.5	−	16	27	−	34	
3-State Output Enable Time	t_{pZL}	$R_L=1k\Omega$	50	4.5	−	19	30	−	38	
				5.5	−	16	27	−	34	
	t_{pZH}		150	4.5	−	24	38	−	48	
				5.5	−	22	34	−	43	
3-State Output Disable Time	t_{pLZ} t_{pHZ}	$R_L=1k\Omega$	50	4.5	−	17	30	−	38	
				5.5	−	16	27	−	34	
Input Capacitance	C_{IN}	DIR, $\overline{G}$			−	5	10	−	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			−	13	−	−	−	
Power Dissipation Capacitance	C_{PD}(1)	TC74HCT245A			−	41	−	−	−	
		TC74HCT640A/T643A			−	39	−	−	−	

Note(1): C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)}=C_{PD} \cdot V_{CC} \cdot f_{IN}+I_{CC}/8(\text{per bit})$$