Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and Plastic DIP, and 20-pin SOJ
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high reliability CMOS technology.

Access times as fast as 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, Plastic 20-pin SOJ, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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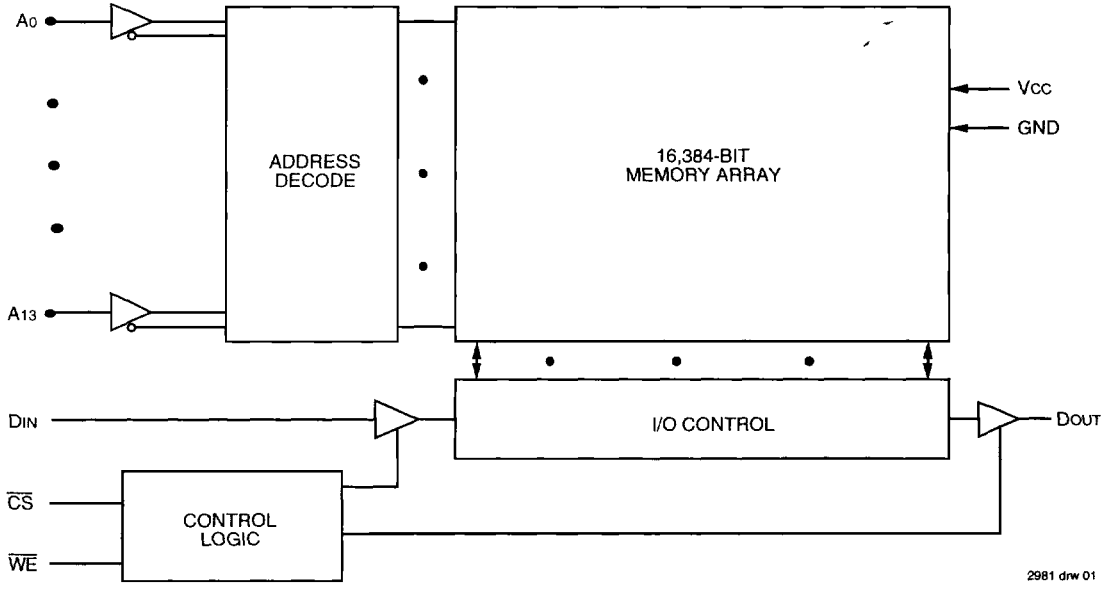
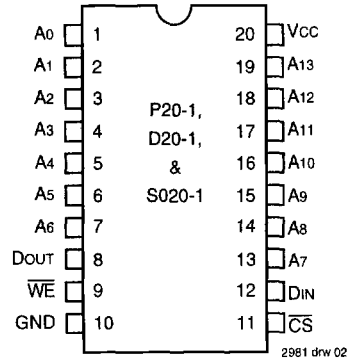
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW

PIN DESCRIPTIONS

A_0–A_{13}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power
D_{IN}	$DATA_{IN}$
D_{OUT}	$DATA_{OUT}$
GND	Ground

2981 tbl 01

TRUTH TABLE (1)

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	$DATA_{OUT}$	Active
Write	L	L	High-Z	Active

NOTE: 2981 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2981 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2981 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2981 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2981 tbl 05
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	6167SA/LA15 Com'l.	6167SA/LA15 Mil.	6167SA/LA20 Com'l.	6167SA/LA20 Mil.	6167SA/LA25 Com'l.	6167SA/LA25 Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	90	90	90	90	90	mA
		LA	55	60	55	60	55	60	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	120	130	100	110	100	100	mA
		LA	100	110	80	85	70	75	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	50	50	35	35	35	35	mA
		LA	35	35	30	30	25	25	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max. $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	5	10	5	10	5	10	mA
		LA	0.9	2	0.05	2	0.05	0.9	

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DC ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	Power	6167SA/LA35 Com'l.	6167SA/LA35 Mil.	6167SA/LA45[2] Com'l.	6167SA/LA45[2] Mil.	6167SA/LA55[2] Com'l.	6167SA/LA55[2] Mil.	6167SA/LA70[2] Com'l.	6167SA/LA70[2] Mil.	Unit
I_{CC1}	Operating Power Supply Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	90	—	90	—	90	—	90	mA
		LA	55	60	—	60	—	60	—	60	
I_{CC2}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	100	100	—	100	—	100	—	100	mA
		LA	65	70	—	65	—	60	—	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	35	35	—	35	—	35	—	35	mA
		LA	20	20	—	20	—	20	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max. $V_{IN} \ge V_{HC}$ or $V_{IN} \le V_{LC}$, f = 0[3]	SA	5	10	—	10	—	10	—	10	mA
		LA	0.05	0.9	—	0.9	—	0.9	—	0.9	

NOTES:

2981 tbl 07

1. All values are maximum guaranteed values.
2. –55°C to +125°C temperature range only. Also available; 85ns and 100ns Military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs cycling at f_{MAX}. f = 0 means no Address inputs change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6167SA Min.	IDT6167SA Max.	IDT6167LA Min.	IDT6167LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.,	MIL	—	10	—	5	µA
		V_{IN} = GND to V_{CC}	COM'L	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH},	MIL	—	10	—	5	µA
		V_{OUT} = GND to V_{CC}	COM'L	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2981 tbl 08

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

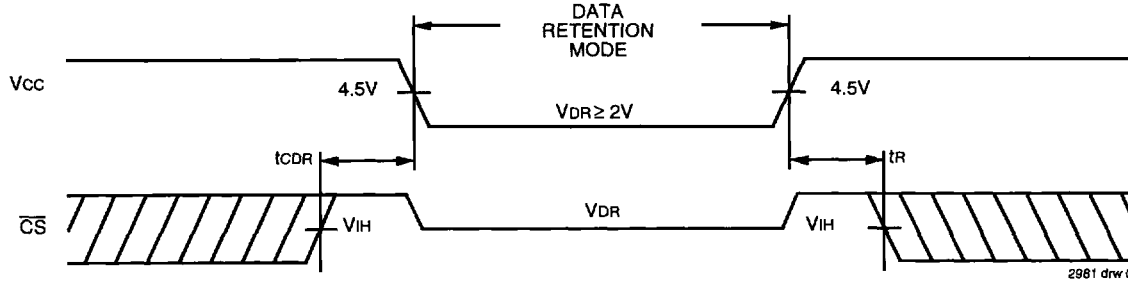
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) V_{CC} @ 2.0v	Typ.(1) V_{CC} @ 3.0V	Max. V_{CC} @ 2.0V	Max. V_{CC} @ 3.0V	Unit
V_{DR}	V_{CC} for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ VIN ≥ V_{HC} or ≤ V_{LC}	MIL.	—	0.5	1.0	200	300	µA
			COM'L.	—	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current	—		—	—	—	2	2	µA

2981 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM



2981 drw 03

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2981 tbl 10

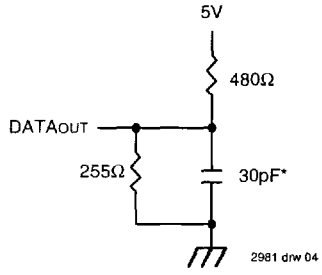


Figure 1. AC Test Load

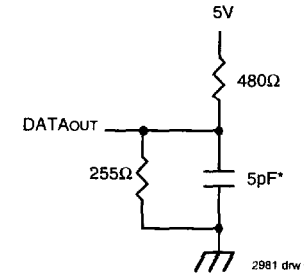


Figure 2. AC Test Load (for t_{CLZ}, t_{CHZ}, t_{WHZ} and t_{OW})

*Includes scope and jig.

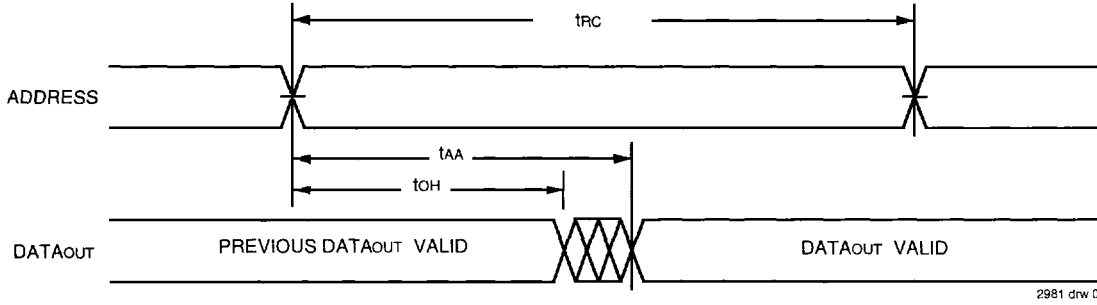
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6167SA15 6167LA15		6167SA20/25 6167LA20/25		6167SA35/45[1] 6167LA35/45[1]		6167SA55[1]/70[1] 6167LA55[1]/70[1]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	15	—	20/25	—	35/45	—	55/70	—	ns
t_{AA}	Address Access Time	—	15	—	20/25	—	35/45	—	55/70	ns
t_{ACS}	Chip Select Access Time	—	15	—	20/25	—	35/45	—	55/70	ns
t_{CLZ}[2]	Chip Deselect to Output in Low-Z	3	—	5/5	—	5/5	—	5/5	—	ns
t_{CHZ}[2]	Chip Select to Output in High-Z	—	10	—	10/10	—	15/30	—	40/40	ns
t_{OH}	Output Hold from Address Change	3	—	5/5	—	5/5	—	5/5	—	ns
t_{PU}[2]	Chip Select to Power-Up Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{PD}[2]	Chip Deselect to Power-Down Time	—	15	—	20/25	—	35/45	—	55/70	ns
Write Cycle										
t_{WC}	Write Cycle Time	15	—	20/20	—	30/45	—	55/70	—	ns
t_{CW}	Chip Select to End-of-Write	15	—	15/20	—	30/40	—	45/55	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	15/20	—	30/40	—	45/55	—	ns
t_{AS}	Address Set-up Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{WP}	Write Pulse Width	13	—	15/20	—	30/30	—	35/40	—	ns
t_{WR}	Write Recovery Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	12/15	—	17/20	—	25/30	—	ns
t_{DH}	Data Hold Time	0	—	0/0	—	0/0	—	0/0	—	ns
t_{WHZ}[2]	Write Enable to Output in High-Z	—	7	—	8/8	—	15/30	—	40/40	ns
t_{OW}[2]	Output Active from End-of-Write	0	—	0/0	—	0/0	—	0/0	—	ns

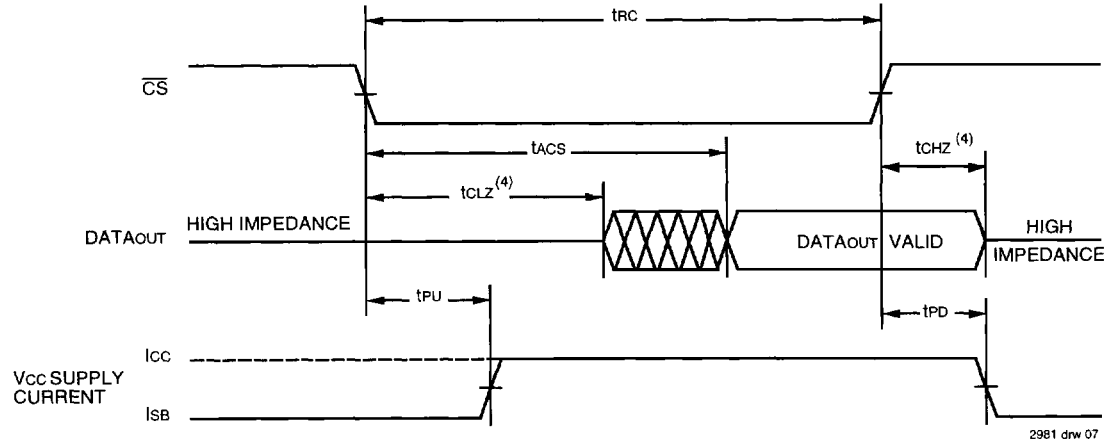
2981 tbl 11

NOTES:
1. –55°C to +125°C temperature range only. Also available: 85ns and 100ns Military devices.
2. This parameter is guaranteed with AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)

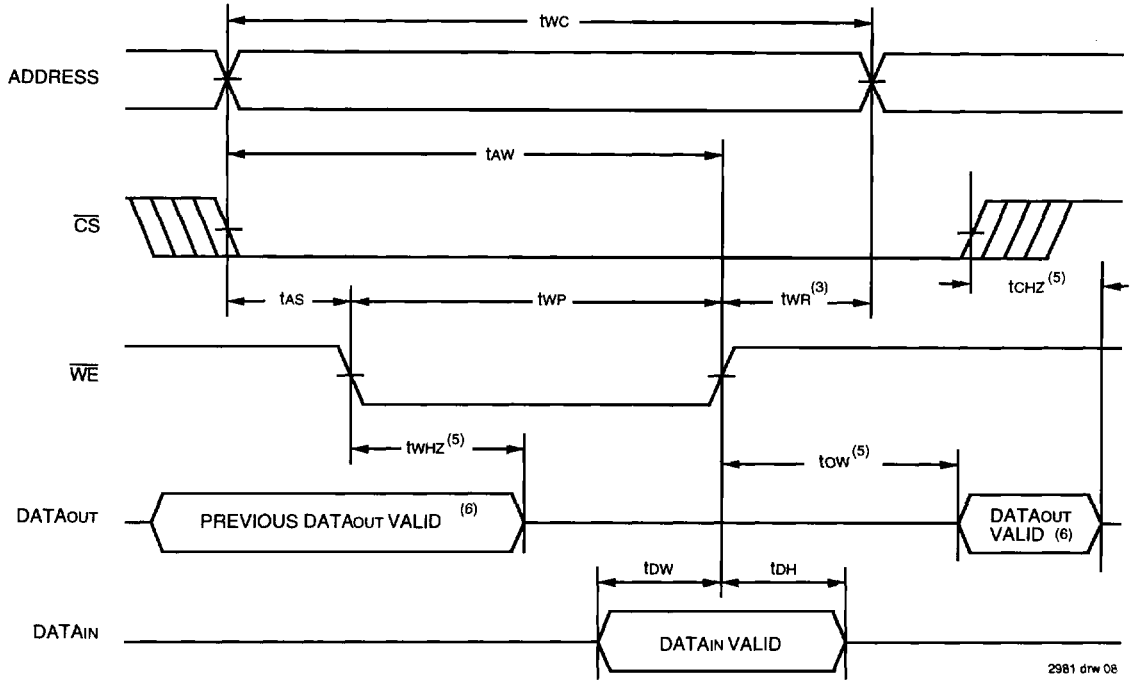


TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)

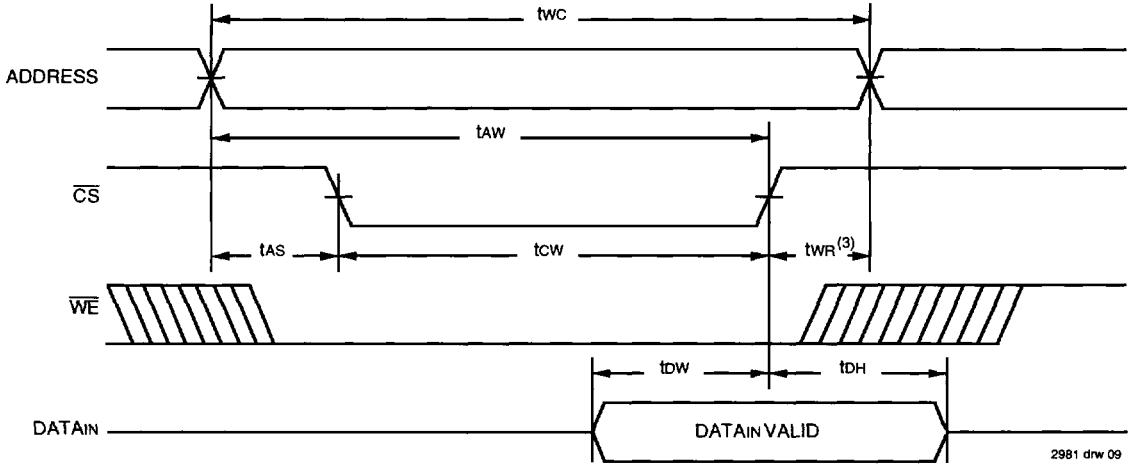


NOTES:
1. $\overline{WE}$ is HIGH for Read cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address valid prior to or coincedent with $\overline{CS}$ transition LOW.
4. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 4)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 4)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
5. Transition is measured ±200mV from steady state.
6. During this period, the I/O pins are in the output state and the input signals must not be applied.

ORDERING INFORMATION