SPEED/PACKAGE AVAILABILITY

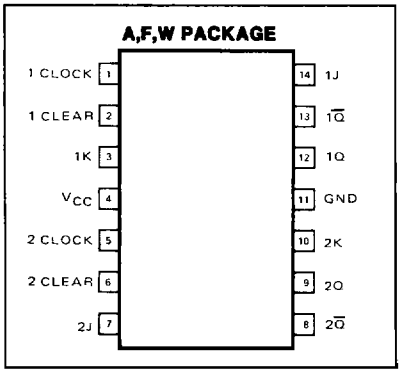
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F

DESCRIPTION

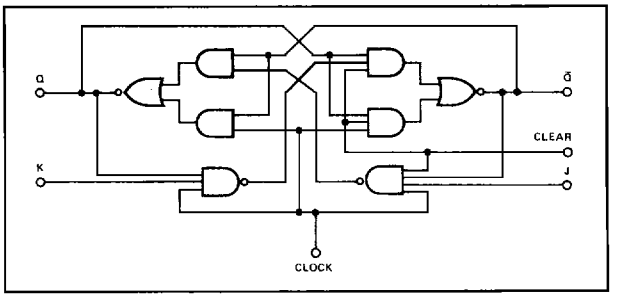
This monolithic edge-triggered dual J-K flip-flop features individual J, K, clock, and clear inputs to each flip-flop. A low logic level at the clear input resets the Q output to a low level regardless of the levels at the other inputs. With clear inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table, as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION

A,F,W PACKAGE



LOGIC DIAGRAM



FUNCTION TABLE (Each Flip-Flop)

54/74, 54/74H

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

54/74LS73

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	Q̄
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			15	20		25	30		30	45		MHz
$t_{w(Clock)}$	Width of clock input pulse									20			ns
	Clock high			20			12						
	Clock low			47			28						
$t_{w(Clear)}$	Width of clear input pulse			25			16			25			ns
t_{Setup}	Input setup time			0↑			0↑			20			ns
t_{Hold}	Input hold time			0↓			0↓			0			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clear			16	25		6	13		11	20	ns
t_{PHL}	High-to-low				25	40		12	24		15	30	ns
t_{PLH}	Low-to-high	Clock		10	16	25		16	21		11	20	ns
t_{PHL}	High-to-low			10	25	40		22	27		15	30	ns

Load circuit and typical waveforms are shown at the front of section.