BURR-BROWN®

033970

OPA100

Low Bias Current JFET Monolithic OPERATIONAL AMPLIFIER

FEATURES

- LOW INITIAL BIAS CURRENT
  1pA max at +25°C
- LOW BIAS CURRENT vs TEMPERATURE
  20pA max at +85°C
- HIGH INPUT IMPEDANCE, $10^{12}\Omega$
- LOW OFFSET VOLTAGE, 250μV max
- LOW OFFSET VOLTAGE DRIFT, 5μV/°C max

APPLICATIONS

- CURRENT-TO-VOLTAGE CONVERSION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  pH electrodes
  Biological probes/transducers
- PHOTO DETECTOR CIRCUITS
- LONG-TERM PRECISION INTEGRATION
- HIGH IMPEDANCE BUFFER
- PRECISION SAMPLE/HOLD

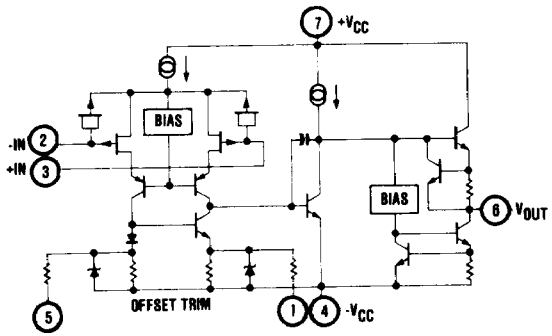
DESCRIPTION

The OPA100 is a precision monolithic low bias current operational amplifier. An enhanced bipolar FET process with JFET input transistors and dielectric isolation is used to achieve low input bias current. Additionally, bias current compensation circuitry is used to reduce the bias current even further. In addition to lowering the bias current at +25°C, this compensation significantly reduces the bias current at higher temperatures.

Low offset voltage (250μV max) and low voltage drift (5μV/°C) are also guaranteed. This performance is achieved by active laser-trimming the amplifiers thin-film resistors.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidentally shorted to supply terminals without damage.

The standard pin configuration (741-type) of the OPA100 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



International Airport Industrial Park • P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = 15VDC unless otherwise noted.

PARAMETER	CONDITIONS	OPA100AM			OPA100BM			OPA100CM			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN, DC	V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	T_A = +25°C	94	100		100	106		106	110		dB
	$T_A = T_{MIN}$ to T_{MAX}	88	100		94	106		100	110		dB
RATED OUTPUT											
Voltage at R_L = 2kΩ	$T_A = T_{MIN}$ to T_{MAX}	±10	±12		"	"		"	"		V
Current	$T_A = T_{MIN}$ to T_{MAX}	±5	±10		"	"		"	"		mA
Output Impedance			100			"			"		Ω
Load Capacitance[1]		500	1000		"	"		"	"		pF
Short Circuit Current		10	40		"	"		"	"		mA
FREQUENCY RESPONSE											
Unity Gain, Small Signal			1			"			"		MHz
Full Power Response		10	32		"	"		"	"		kHz
Slew Rate		0.6	2		"	"		"	"		V/µsec
Settling Time 0.1%	10V step		6			"			"		µsec
Settling Time 0.01%	10V step		10			"			"		µsec
Overload Recovery, 50% overdrive[2]			5			"			"		µsec
INPUT OFFSET VOLTAGE[3]											
Initial Offset	T_A = 25°C		±200	±1000		±100	±500		±50	±250	µV
Average Drift	$T_A = T_{MIN}$ to T_{MAX}		±3	±15		"	±10		±1	±5	µV/°C
Over Temperature	$T_A = T_{MIN}$ to T_{MAX}			±2			±1/±1.5			±0.5	mV
vs Supply	$T_A = T_{MIN}$ to T_{MAX}		±10	±100		"	±25		"	±25	µV/V
INPUT BIAS CURRENT[3]											
Initial Bias Current	T_A = +25°C		±1	±3		±0.6	±2		±0.3	±1	pA
Over Temperature	T_A = +85°C		±10	±100		"	±40		±5	±20	pA
INPUT OFFSET CURRENT											
Initial Difference Current	T_A = +25°C		±0.5			"			"		pA
Over Temperature	T_A = +85°C		±10			"			±5		pA
INPUT IMPEDANCE											
Differential			10^{12} || 6			"			"		Ω || pF
Common-Mode			10^{13} || 6			"			"		Ω || pF
INPUT NOISE											
Voltage, f_O = 10Hz			60			"			"		$nV/\sqrt{Hz}$
f_O = 100Hz			35			"			"		$nV/\sqrt{Hz}$
f_O = 1kHz			20			"			"		$nV/\sqrt{Hz}$
f_O = 10kHz			20			"			"		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			1			"			"		µV, p-p
Current, f_B = 0.1Hz to 10Hz			0.01			"			"		pA, p-p
f_B = 10Hz to 10kHz			0.03			"			"		pA, rms
f_O = 1kHz			0.6			"			"		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE											
Differential		±18			"			"			V
Common-Mode	$T_A = T_{MIN}$ to T_{MAX}	±10	±12		"	"		"	"		V
Common-Mode Rejection, V_{IN} = ±10V	$T_A = T_{MIN}$ to T_{MAX}	76	82		88	94		94	100		dB
Maximum Safe Input Voltage			±V_{CC}			"			"		V
POWER SUPPLY											
Rated Voltage			±15			"			"		VDC
Voltage Range, Derated Performance		±5		±18	"		"	"		"	VDC
Current, Quiescent	$T_A = T_{MIN}$ to T_{MAX}		1.0	3		"	2		"	1.5	mA
TEMPERATURE RANGE	Ambient										
Specification		−25		+85	"		"	"		"	°C
Operating		−55		+125	"		"	"		"	°C
Storage		65		+150	"		"	"		"	°C
θ Junction-Ambient			300			"			"		°C/W

"Specification same as for OPA100AM

NOTES (1) Stability guaranteed with load capacitance ≤500pF. (2) Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive. (3) Offset voltage and bias current are guaranteed after 1 minute of operation at T_A = +25°C. They are 100% tested.

ORDERING INFORMATION

OPA100 X X

Basic model number

Performance grade
A, B, C -25°C to +85°C

Package code
TO-99 metal can, M

ABSOLUTE MAXIMUM RATINGS

Supply	±18VDC
Internal power Dissipation(1)	500mW
Differential Input Voltage(2)	±36VDC
Input Voltage Range(2)	±18VDC
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
Lead Temperature (soldering, 10 seconds)	+300°C
Output Short Circuit Duration(3)	Continuous
Junction Temperature	+175°C

NOTES:
1. Package must be derated based on: θ_{JC} = 150°C/W or θ_{JA} = 300°C/W.
2. For supply voltages less than ±18VDC the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to power supply common only. Rating applies to +25°C ambient.

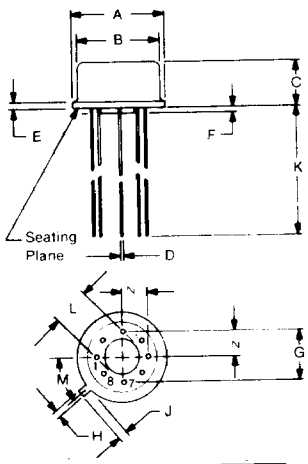
MECHANICAL

TO-99 PACKAGE

NOTE:
Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

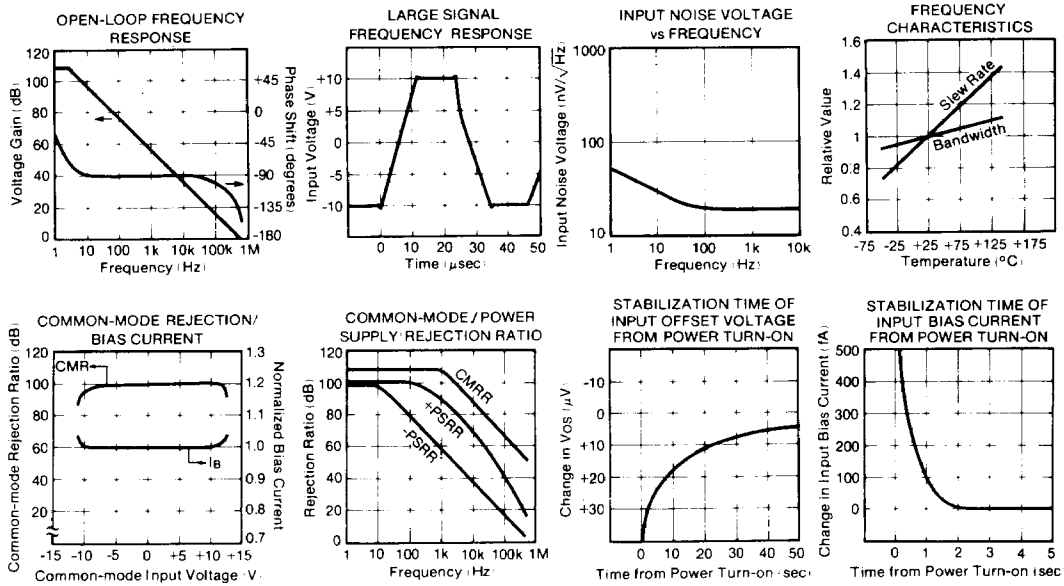
Pin material and plating composition conform to Method 2003 solderability of MIL-STD-883 except paragraph 3.2.



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	335	370	8.51	9.40
B	305	335	7.75	8.51
C	165	185	4.19	4.70
D	016	021	0.41	0.53
E	010	040	0.25	1.02
F	010	040	0.25	1.02
G	200 BASIC		5.08 BASIC	
H	028	034	0.71	0.86
J	029	045	0.74	1.14
K	500		12.7	
L	110	160	2.79	4.06
M	45° BASIC		45° BASIC	
N	095	105	2.41	2.67

TYPICAL PERFORMANCE CURVES

At T_A = +25°C and ±V_{CC} = 15VDC unless otherwise noted.



APPLICATIONS INFORMATION

INPUT BIAS CURRENT

The OPA100 uses FET input transistors with dielectric isolation to achieve low input bias currents. Additionally, bias current compensation circuitry is used to reduce the bias current even further. In addition to lowering the bias current at +25°C, this compensation makes significant reduction in the bias current at higher temperatures. Figure 1 shows an improvement of over a decade for temperatures above +75°C.

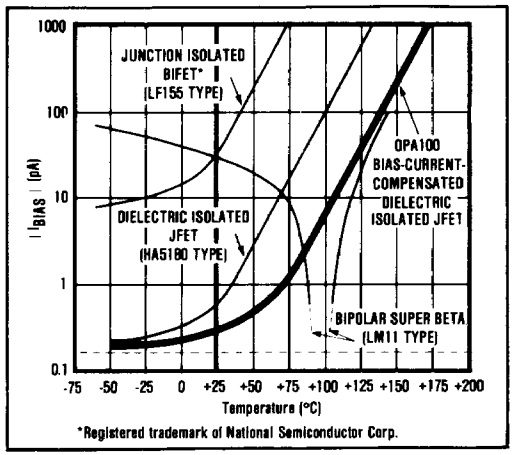


FIGURE 1. Absolute Value of Bias Current vs Temperature.

The compensation causes the polarity of the bias current to be indeterminate (note the "±" signs for I_B in the electrical specifications). This means that the bias current may flow into or out of the amplifier inputs.

VOLTAGE NOISE

In many FET amplifier applications the voltage noise is a critical parameter. The bias current cancellation design of the OPA100 allows low noise without sacrificing low bias current. Figure 2 shows the noise of various types of

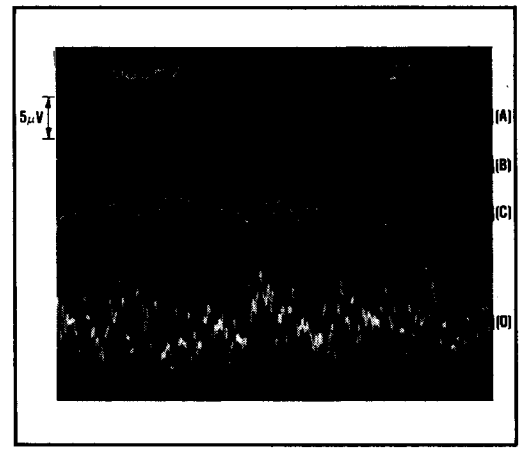


FIGURE 2. Noise of Various Low Bias Current Op Amps. (A) OPA100, (B) LF155 type, (C) LM11 type, (D) HA 5180 type.

low bias current operational amplifiers. The noise test circuit used has a gain of 100kV/V with a 1-pole filter at 0.1Hz and a 5-pole filter at 10Hz.

GUARDING AND SHIELDING

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA100. To avoid leakage problems, it is recommended that the signal input lead of the OPA100 be wired to a Teflon standoff. If the OPA100 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the high impedance input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup (see Figure 3).

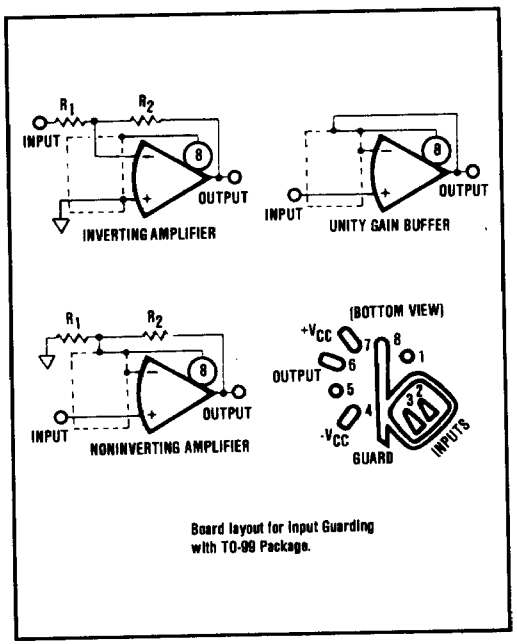


FIGURE 3. Connection of Input Guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA100 has a low initial offset voltage (250μV), some applications may require external nulling of this small offset. External offset voltage adjustment changes the drift by approximately 0.3μV/°C, for every 100μV of offset adjusted. See Figure 4.

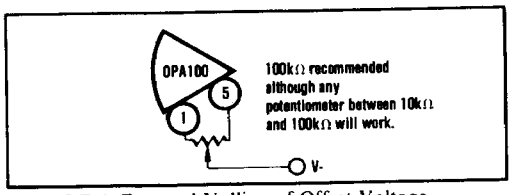


FIGURE 4. External Nulling of Offset Voltage.

APPLICATION CIRCUITS

The OPA100 is ideally suited for low bias current, high input impedance applications. Also because the noise and offset drift errors are low, total high performance can be achieved. Figures 5 through 8 show a photodiode, pH probe, isolation, and integrator amplifier.

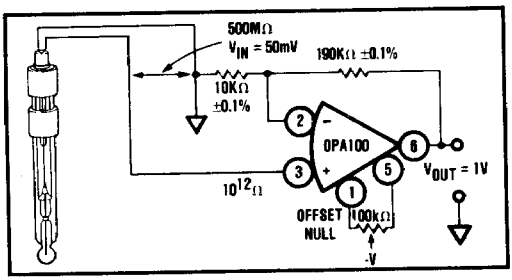


FIGURE 5. pH Probe Amplifier.

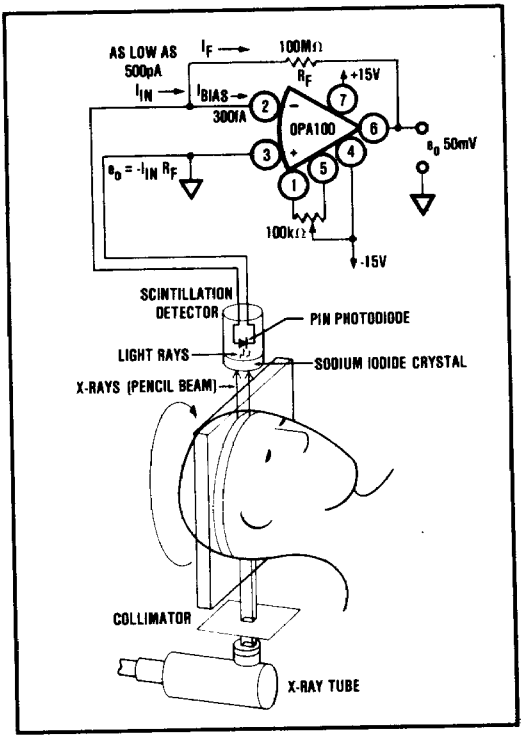


FIGURE 6. Computerized Axial Tomography (CAT) Scanner Channel Amplifier.

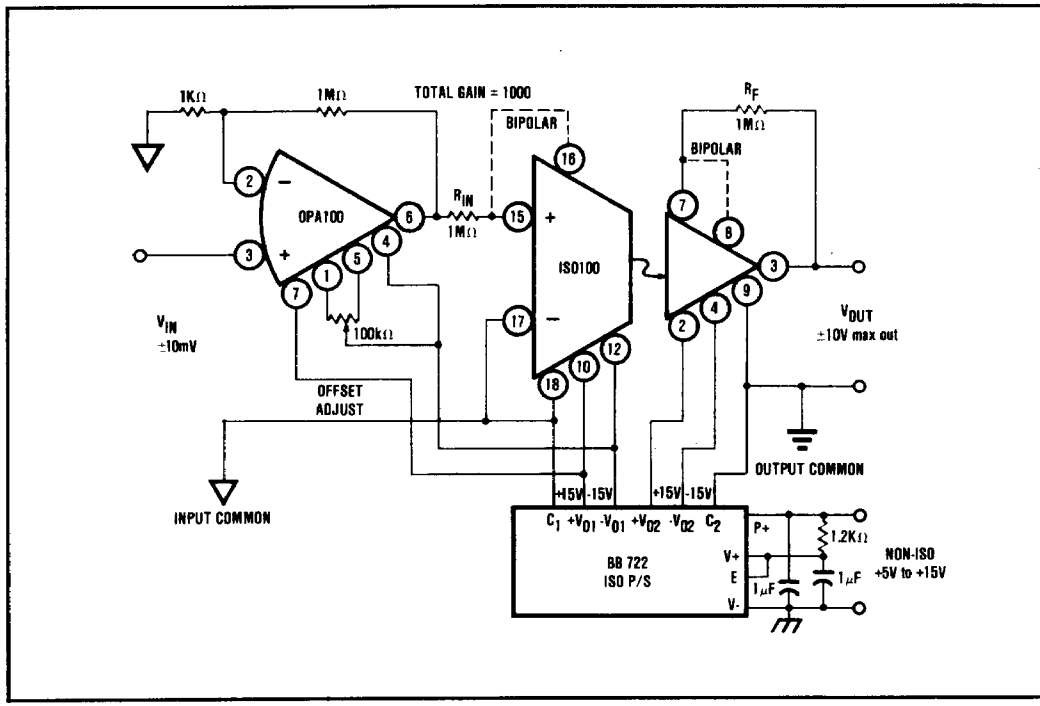


FIGURE 7. Low Level High Impedance Isolation Amplifier.

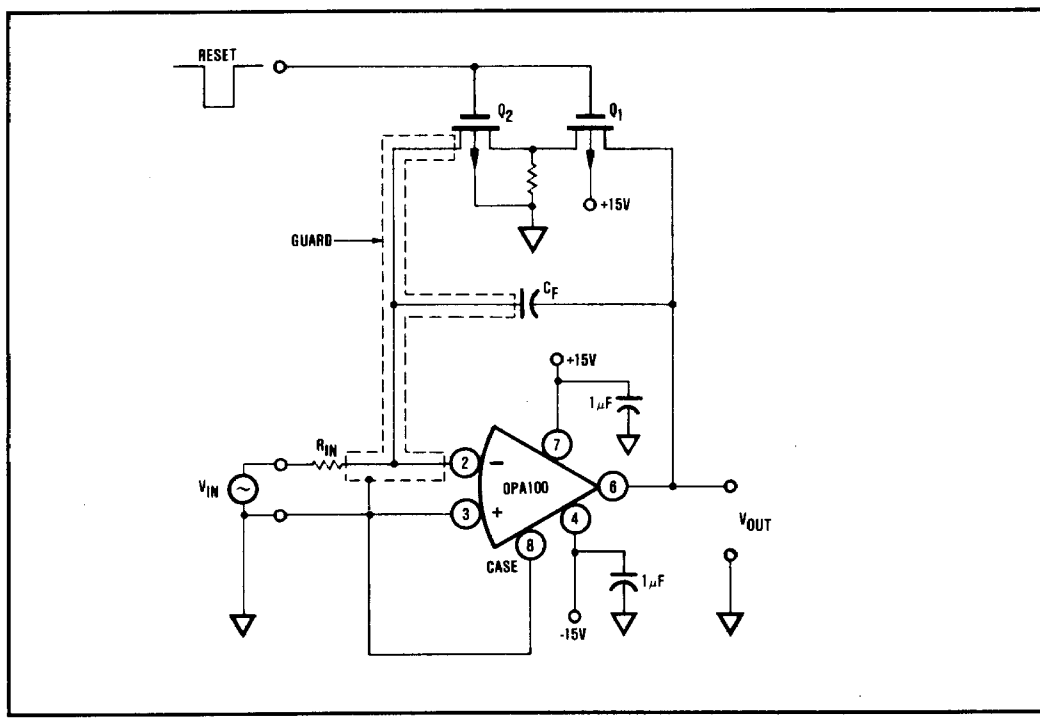


FIGURE 8. High Accuracy Integrator with Reset.