

**Features**

- Low Voltage and Standard Voltage Operation
  - 5.0 (V<sub>CC</sub> = 4.5V to 5.5V)
  - 2.7 (V<sub>CC</sub> = 2.7V to 5.5V)
  - 2.5 (V<sub>CC</sub> = 2.5V to 5.5V)
  - 1.8 (V<sub>CC</sub> = 1.8V to 5.5V)
- User Selectable Internal Organization
  - 1K: 128 x 8 or 64 x 16
  - 2K: 256 x 8 or 128 x 16
  - 4K: 512 x 8 or 256 x 16
- 3-Wire Serial Interface
- 2 MHz Clock Rate (5V) Compatibility
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin PDIP, JEDEC SOIC, and EIAJ SOIC Packages

**Description**

The AT93C46/56/57/66 provides 1024/2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V<sub>CC</sub> and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT93C46/56/57/66 is available in space saving 8-pin PDIP and 8-pin JEDEC and EIAJ SOIC packages.

(continued)

**3-Wire  
Serial CMOS  
E<sup>2</sup>PROMs**

1K (128 x 8 or 64 x 16)

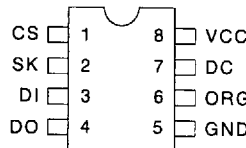
2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

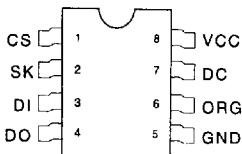
**Pin Configurations**

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V <sub>CC</sub>	Power Supply
ORG	Internal Organization
DC	Don't Connect

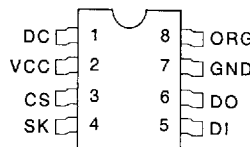
8-Pin PDIP



8-Pin SOIC



8-Pin SOIC



Rotated (R)  
(1K JEDEC Only)





## Description (Continued)

The AT93C46/56/57/66 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate ERASE cycle is required be-

fore WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. When CS is brought "high" following the initiation of a WRITE cycle, the DO pin outputs the READY/BUSY status of the part.

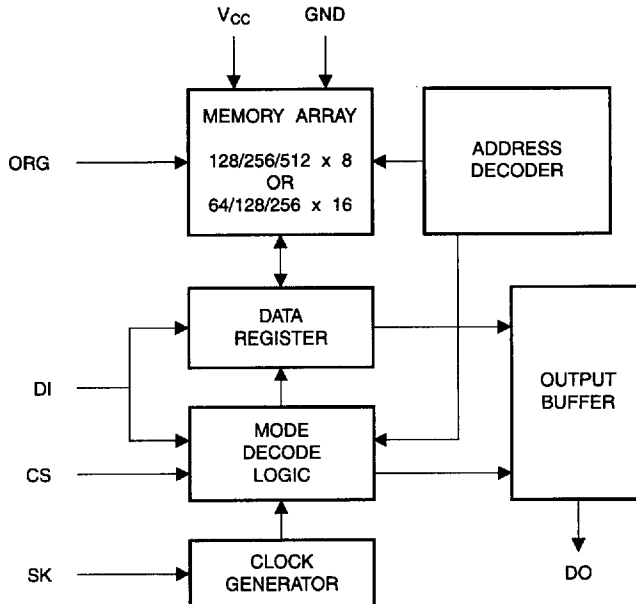
The AT93C46/56/57/66 is available in 4.5V to 5.5V, 2.7V to 5.5V, 2.5V to 5.5V, and 1.8V to 5.5V versions.

## Absolute Maximum Ratings\*

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground .....	-1.0V to +7.0V
Maximum Operating Voltage .....	6.25V
DC Output Current.....	5.0 mA

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Block Diagram <sup>(1)</sup>



Note: 1. When the ORG pin is connected to Vcc, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device (of approximately 1 MΩ) will select the x 16 organization. This feature is not available on 1.8V devices.

**Pin Capacitance** <sup>(1)</sup>

Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +5.0\text{V}$  (unless otherwise noted).

Test Conditions		Max	Units	Conditions
$C_{OUT}$	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
$C_{IN}$	Input Capacitance (CS, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

**DC Characteristics**

Applicable over recommended operating range from:  $T_{AI} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$ ,  $T_{AC} = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$  (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$V_{CC1}$	Supply Voltage		1.8		5.5	V
$V_{CC2}$	Supply Voltage		2.5		5.5	V
$V_{CC3}$	Supply Voltage		2.7		5.5	V
$V_{CC4}$	Supply Voltage		4.5		5.5	V
$I_{CC}$	Supply Current	$V_{CC} = 5.0\text{V}$	READ at 1.0 MHz	0.5	2.0	mA
			WRITE at 1.0 MHz	0.5	2.0	mA
$I_{SB1}$	Standby Current	$V_{CC} = 1.8\text{V}$		0	0.1	$\mu\text{A}$
$I_{SB2}$	Standby Current	$V_{CC} = 2.5\text{V}$		6.0	10.0	$\mu\text{A}$
$I_{SB3}$	Standby Current	$V_{CC} = 2.7\text{V}$		6.0	10.0	$\mu\text{A}$
$I_{SB4}$	Standby Current	$V_{CC} = 5.0\text{V}$		17	30	$\mu\text{A}$
$I_{IL}$	Input Leakage	$V_{IN} = 0\text{V}$ to $V_{CC}$		0.1	1.0	$\mu\text{A}$
$I_{OL}$	Output Leakage	$V_{IN} = 0\text{V}$ to $V_{CC}$		0.1	1.0	$\mu\text{A}$
$V_{IL1}^{(1)}$	Input Low Voltage	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	-0.1		0.8	V
$V_{IH1}^{(1)}$	Input High Voltage		2.0		$V_{CC} + 1$	
$V_{IL2}^{(1)}$	Input Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	0.0		$V_{CC} \times 0.3$	V
$V_{IH2}^{(1)}$	Input High Voltage		$V_{CC} \times 0.7$		$V_{CC} + 1$	
$V_{OL1}$	Output Low Voltage	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	$I_{OL} = 2.1\text{ mA}$		0.4	V
$V_{OH1}$	Output High Voltage		$I_{OH} = -0.4\text{ mA}$	2.4		V
$V_{OL2}$	Output Low Voltage	$1.8\text{V} \leq V_{CC} \leq 2.7\text{V}$	$I_{OL} = 0.15\text{ mA}$		0.2	V
$V_{OH2}$	Output High Voltage		$I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 0.2$		V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.





## AC Characteristics

Applicable over recommended operating range from  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = \text{As Specified}$ ,  
 $CL = 1$  TTL Gate and  $100$  pF (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f <sub>SK</sub>	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		2	MHz
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		1	
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		0.5	
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		0.25	
t <sub>SKH</sub>	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	500			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	1000			
t <sub>SKL</sub>	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	500			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	1000			
t <sub>CS</sub>	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	500			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	1000			
t <sub>CSS</sub>	CS Setup Time	Relative to SK	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	50		ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	50			
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	200			
t <sub>DIS</sub>	DI Setup Time	Relative to SK	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100		ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	200			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	400			
t <sub>CSH</sub>	CS Hold Time	Relative to SK	0			ns
t <sub>DIH</sub>	DI Hold Time	Relative to SK	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100		ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	200			
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$	400			
t <sub>PD1</sub>	Output Delay to '1'	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		250		
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		500		
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		1000		
t <sub>PD0</sub>	Output Delay to '0'	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		250		
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		500		
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		1000		
t <sub>SV</sub>	CS to Status Valid	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		250		
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		500		
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		1000		
t <sub>DF</sub>	CS to DO in High Impedance	AC Test	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		100	ns
		CS = V <sub>IL</sub>	$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$		100	
		$2.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		200		
		$1.8\text{V} \leq V_{CC} \leq 5.5\text{V}$		400		
t <sub>WP</sub>	Write Cycle Time		0.1		10	ms
		$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$		1		ms

Instruction Set for the AT93C46

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A <sub>6</sub> - A <sub>0</sub>	A <sub>5</sub> - A <sub>0</sub>			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXX	11XXXX			Write enable must precede all programming modes.
ERASE	1	11	A <sub>6</sub> - A <sub>0</sub>	A <sub>5</sub> - A <sub>0</sub>			Erase memory location A <sub>n</sub> - A <sub>0</sub> .
WRITE	1	01	A <sub>6</sub> - A <sub>0</sub>	A <sub>5</sub> - A <sub>0</sub>	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes memory location A <sub>n</sub> - A <sub>0</sub> .
ERAL	1	00	10XXXXXX	10XXXX			Erases all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V.
WRAL	1	00	01XXXXXX	01XXXX	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V.
EWDS	1	00	00XXXXXX	00XXXX			Disables all programming instructions.

2

Instruction Set for the AT93C57

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A <sub>7</sub> - A <sub>0</sub>	A <sub>6</sub> - A <sub>0</sub>			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXXX	11XXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A <sub>7</sub> - A <sub>0</sub>	A <sub>6</sub> - A <sub>0</sub>			Erase memory location A <sub>n</sub> - A <sub>0</sub> .
WRITE	1	01	A <sub>7</sub> - A <sub>0</sub>	A <sub>6</sub> - A <sub>0</sub>	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes memory location A <sub>n</sub> - A <sub>0</sub> .
ERAL	1	00	10XXXXXXXX	10XXXXXX			Erases all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXXX	01XXXXXX	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V.
EWDS	1	00	00XXXXXXXX	00XXXXXX			Disables all programming instructions.





## Instruction Set for the AT93C56 and AT93C66

Instruction	SB	Op Code	Address		Data		Comments
			x 8	x 16	x 8	x 16	
READ	1	10	A <sub>8</sub> - A <sub>0</sub>	A <sub>7</sub> - A <sub>0</sub>			Reads data stored in memory, at specified address.
EWEN	1	00	11XXXXXXXX	11XXXXXXXX			Write enable must precede all programming modes.
ERASE	1	11	A <sub>8</sub> - A <sub>0</sub>	A <sub>7</sub> - A <sub>0</sub>			Erases memory location A <sub>n</sub> - A <sub>0</sub> .
WRITE	1	01	A <sub>8</sub> - A <sub>0</sub>	A <sub>7</sub> - A <sub>0</sub>	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes memory location A <sub>n</sub> - A <sub>0</sub> .
ERAL	1	00	10XXXXXXXX	10XXXXXXXX			Erases all memory locations. Valid only at V <sub>CC</sub> = 4.5V to 5.5V.
WRAL	1	00	01XXXXXXXX	01XXXXXXXX	D <sub>7</sub> - D <sub>0</sub>	D <sub>15</sub> - D <sub>0</sub>	Writes all memory locations. Valid when V <sub>CC</sub> = 5.0V ± 10% and Disable Register cleared.
EWDS	1	00	00XXXXXXXX	00XXXXXXXX			Disables all programming instructions.

## Functional Description

The AT93C46/56/57/66 is accessed via a simple and versatile 3-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

**READ (READ):** The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic '0') precedes the 8 or 16 bit data output string.

**ERASE/WRITE (EWEN):** To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or Vcc power is removed from the part.

**ERASE (ERASE):** The Erase (ERASE) instruction programs all bits in the specified memory location to the logical '1' state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (tcs). A logic '1' at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

**WRITE (WRITE):** The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (tcs). A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A READY/BUSY status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, twp.

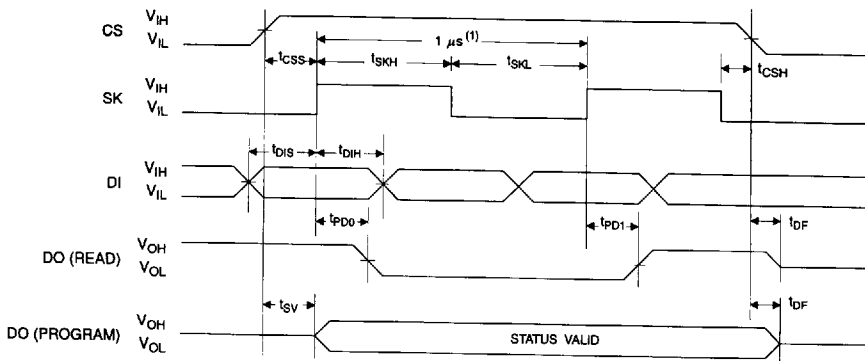
**ERASE ALL (ERAL):** The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (tcs). The ERAL instruction is valid only at Vcc = 5.0V ± 10%.

**WRITE ALL (WRAL):** The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the READY/BUSY status of the part if CS is brought high after being kept low for a minimum of 250 ns (tcs). The WRAL instruction is valid only at Vcc = 5.0V ± 10%.

**ERASE/WRITE DISABLE (EWDS):** To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

## Timing Diagrams

### Synchronous Data Timing



Note: 1. This is the minimum SK period.

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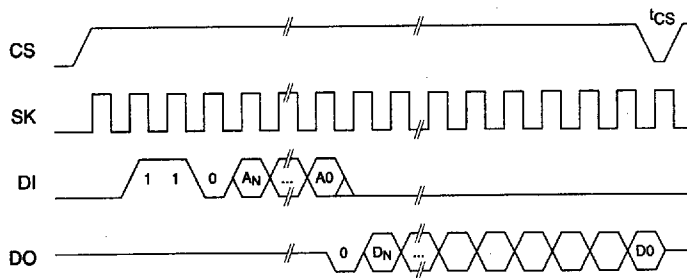
## Organization Key for Timing Diagrams

I/O	AT93C46 (1K)		AT93C56 (2K)		AT93C57 (2K)		AT93C66 (4K)	
	x 8	x 16	x 8	x 16	x 8	x 16	x 8	x 16
AN	A <sub>6</sub>	A <sub>5</sub>	A <sub>8</sub> <sup>(1)</sup>	A <sub>7</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>8</sub>	A <sub>7</sub>
DN	D <sub>7</sub>	D <sub>15</sub>	D <sub>7</sub>	D <sub>15</sub>	D <sub>7</sub>	D <sub>15</sub>	D <sub>7</sub>	D <sub>15</sub>

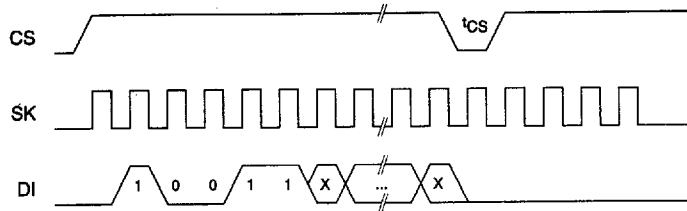
Note: 1. A<sub>8</sub> is a DON'T CARE value, but the extra clock is required.

## Timing Diagrams (Continued)

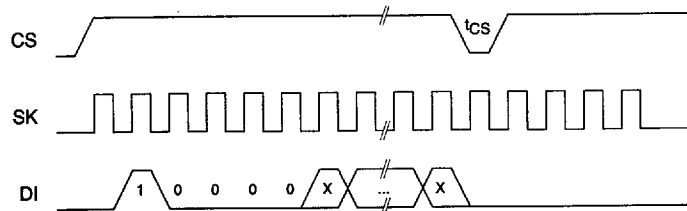
### READ Timing {



### EWEN Timing



### EWDS Timing

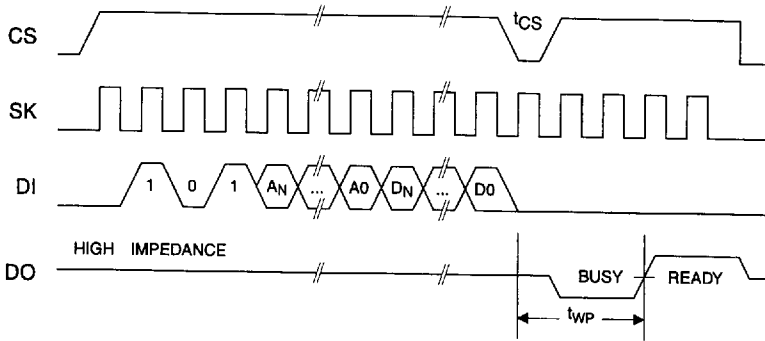


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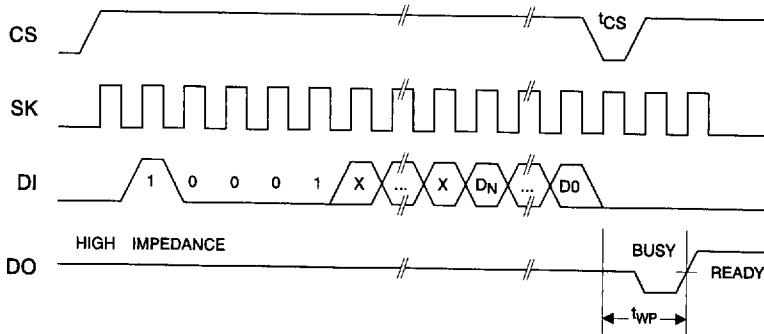


Timing Diagrams (Continued)

WRITE Timing

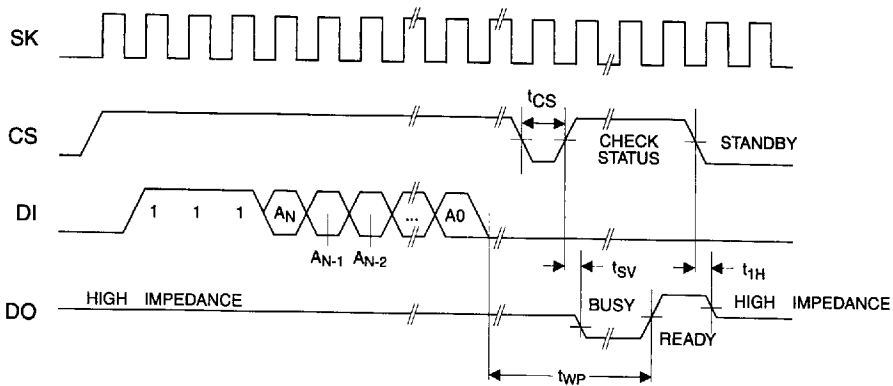


WRAL Timing<sup>(1)</sup>



Note: 1. Valid only at  $V_{CC} = 4.5V$  to  $5.5V$ .

ERASE Timing

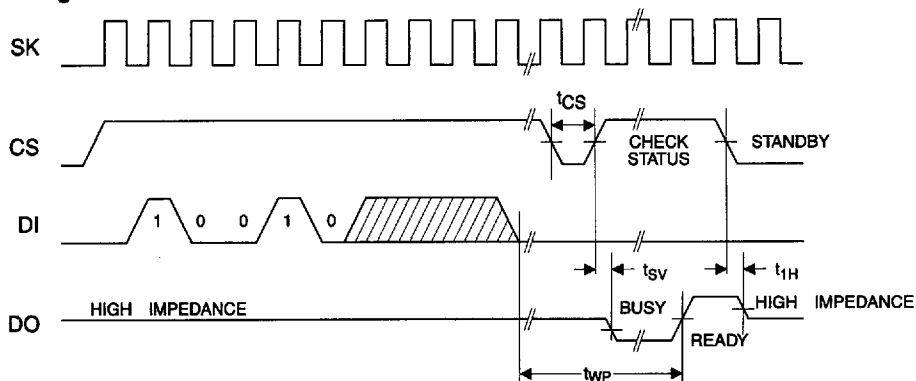


(continued)



## Timing Diagrams (Continued)

### TERAL Timing <sup>(1)</sup>



Note: 1. Valid only at  $V_{CC} = 4.5V$  to  $5.5V$ .

**Ordering Information**

<b>twp (max)</b> <b>(ms)</b>	<b>icc (max)</b> <b>(<math>\mu</math>A)</b>	<b>lsb (max)</b> <b>(<math>\mu</math>A)</b>	<b>fMAX</b> <b>(kHz)</b>	<b>Ordering Code</b>	<b>Package</b>	<b>Operation Range</b>
10	2000	30.0	2000	AT93C46-10PC AT93C46-10SC AT93C46R-10SC AT93C46W-10SC	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C46-10PC-2.7 AT93C46-10SC-2.7 AT93C46R-10SC-2.7 AT93C46W-10SC-2.7	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C46-10PC-2.5 AT93C46-10SC-2.5 AT93C46R-10SC-2.5 AT93C46W-10SC-2.5	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C46-10PC-1.8 AT93C46-10SC-1.8 AT93C46R-10SC-1.8 AT93C46W-10SC-1.8	8P3 8S1 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C46-10PI AT93C46-10SI AT93C46R-10SI AT93C46W-10SI	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C46-10PI-2.7 AT93C46-10SI-2.7 AT93C46R-10SI-2.7 AT93C46W-10SI-2.7	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C46-10PI-2.5 AT93C46-10SI-2.5 AT93C46R-10SI-2.5 AT93C46W-10SI-2.5	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C46-10PI-1.8 AT93C46-10SI-1.8 AT93C46R-10SI-1.8 AT93C46W-10SI-1.8	8P3 8S1 8S1 8S2	Industrial (-40°C to 85°C)





## Ordering Information

Package Type	
<b>8P3</b>	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8S2</b>	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
<b>Blank</b>	Standard Device (4.5V to 5.5V)
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>-2.5</b>	Low Voltage (2.5V to 5.5V)
<b>-1.8</b>	Low Voltage (1.8V to 5.5V)
<b>R</b>	Rotated Pinout

## Ordering Information

twp (max) (ms)	icc (max) ( $\mu$ A)	lsb (max) ( $\mu$ A)	fMAX (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C56-10PC AT93C56-10SC AT93C56W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C56-10PC-2.7 AT93C56-10SC-2.7 AT93C56W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C56-10PC-2.5 AT93C56-10SC-2.5 AT93C56W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C56-10PC-1.8 AT93C56-10SC-1.8 AT93C56W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C56-10PI AT93C56-10SI AT93C56W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C56-10PI-2.7 AT93C56-10SI-2.7 AT93C56W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C56-10PI-2.5 AT93C56-10SI-2.5 AT93C56W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C56-10PI-1.8 AT93C56-10SI-1.8 AT93C56W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
<b>8P3</b>	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8S2</b>	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
<b>Blank</b>	Standard Device (4.5V to 5.5V)
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>-2.5</b>	Low Voltage (2.5V to 5.5V)
<b>-1.8</b>	Low Voltage (1.8V to 5.5V)





## Ordering Information

t <sub>WP</sub> (max) (ms)	I <sub>CC</sub> (max) ( $\mu$ A)	I <sub>SB</sub> (max) ( $\mu$ A)	f <sub>MAX</sub> (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C57-10PC AT93C57-10SC AT93C57W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C57-10PC-2.7 AT93C57-10SC-2.7 AT93C57W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C57-10PC-2.5 AT93C57-10SC-2.5 AT93C57W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C57-10PC-1.8 AT93C57-10SC-1.8 AT93C57W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C57-10PI AT93C57-10SI AT93C57W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C57-10PI-2.7 AT93C57-10SI-2.7 AT93C57W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C57-10PI-2.5 AT93C57-10SI-2.5 AT93C57W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C57-10PI-1.8 AT93C57-10SI-1.8 AT93C57W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
<b>8P3</b>	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
<b>8S1</b>	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
<b>8S2</b>	8 Lead, 0.200" Wide, Plastic Gull Wing Small Outline (EIAJ SOIC)
Options	
<b>Blank</b>	Standard Device (4.5V to 5.5V)
<b>-2.7</b>	Low Voltage (2.7V to 5.5V)
<b>-2.5</b>	Low Voltage (2.5V to 5.5V)
<b>-1.8</b>	Low Voltage (1.8V to 5.5V)

**Ordering Information**

twp (max) (ms)	icc (max) ( $\mu$ A)	lsb (max) ( $\mu$ A)	fMAX (kHz)	Ordering Code	Package	Operation Range
10	2000	30.0	2000	AT93C66-10PC AT93C66-10SC AT93C66W-10SC	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	800	10.0	1000	AT93C66-10PC-2.7 AT93C66-10SC-2.7 AT93C66W-10SC-2.7	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	600	10.0	500	AT93C66-10PC-2.5 AT93C66-10SC-2.5 AT93C66W-10SC-2.5	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	80	0.1	250	AT93C66-10PC-1.8 AT93C66-10SC-1.8 AT93C66W-10SC-1.8	8P3 8S1 8S2	Commercial (0°C to 70°C)
10	2000	30.0	2000	AT93C66-10PI AT93C66-10SI AT93C66W-10SI	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	800	10.0	1000	AT93C66-10PI-2.7 AT93C66-10SI-2.7 AT93C66W-10SI-2.7	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	600	10.0	500	AT93C66-10PI-2.5 AT93C66-10SI-2.5 AT93C66W-10SI-2.5	8P3 8S1 8S2	Industrial (-40°C to 85°C)
10	80	0.1	250	AT93C66-10PI-1.8 AT93C66-10SI-1.8 AT93C66W-10SI-1.8	8P3 8S1 8S2	Industrial (-40°C to 85°C)

Package Type	
<b>8P3</b>	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
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<b>-1.8</b>	Low Voltage (1.8V to 5.5V)

