DS04–21322–1aE

FUJITSU

DATA SHEET

MB15B01 ASSP

DUAL INPUT PLL FREQUENCY SYNTHESIZER

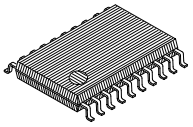
DUAL SERIAL INPUT PLL FREQUENCY SYNTHESIZER WITH 1.1GHz PRESCALER

The Fujitsu MB15B01 is a 1.1 GHz dual serial input PLL (Phase Locked Loop) frequency synthesizer designed for cellular phones, cordless phones and other radio applications.

The MB15B01 has two PLL circuits on a single chip: PLL1 and PLL2. An analog switch is provided for each PLL circuit to decrease lock up time. Separate power supply pins are provided for each PLL circuit.

Two 1.1 GHz dual modulus prescalers are included inside and enables a pulse swallow function.

It operates with a supply voltage of 3.0V typ. and dissipates 13 mA typ. of current realized through the use of Fujitsu's unique Bi-CMOS technology.

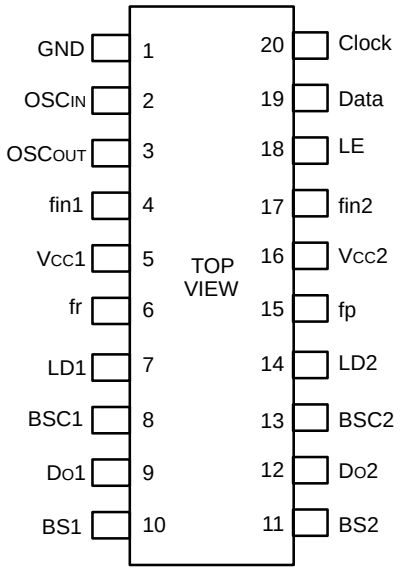


PLASTIC FLAT PACKAGE
FPT-20P-M03

FEATURES

- High operating frequency: fin = 1.1 GHz (Pin = –10 dBm, Vcc = 3V)
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 8 to 16,383
- Serial input 18-bit programmable divider consisting of:
  – Binary 7-bit swallow counter: 0 to 127
  – Binary 11-bit programmable counter: 16 to 2,047
  Each programmable counter can be controlled independently.
- Low power supply voltage: V_{CC} = 2.7 to 3.5V
- Low power supply current: I_{CC} (total) = 13 mA typ. (Vcc = 3V)
- Power saving function : I_{CC1} = I_{CC2} = 100 µA typ (Vcc = 3V)
- On-chip analog switches achieve fast lock up time
- Digital lock detector
- Wide operating temperature: Ta = –30 to 80°C
- Plastic 20-pin SSOP package

PIN ASSIGNMENT



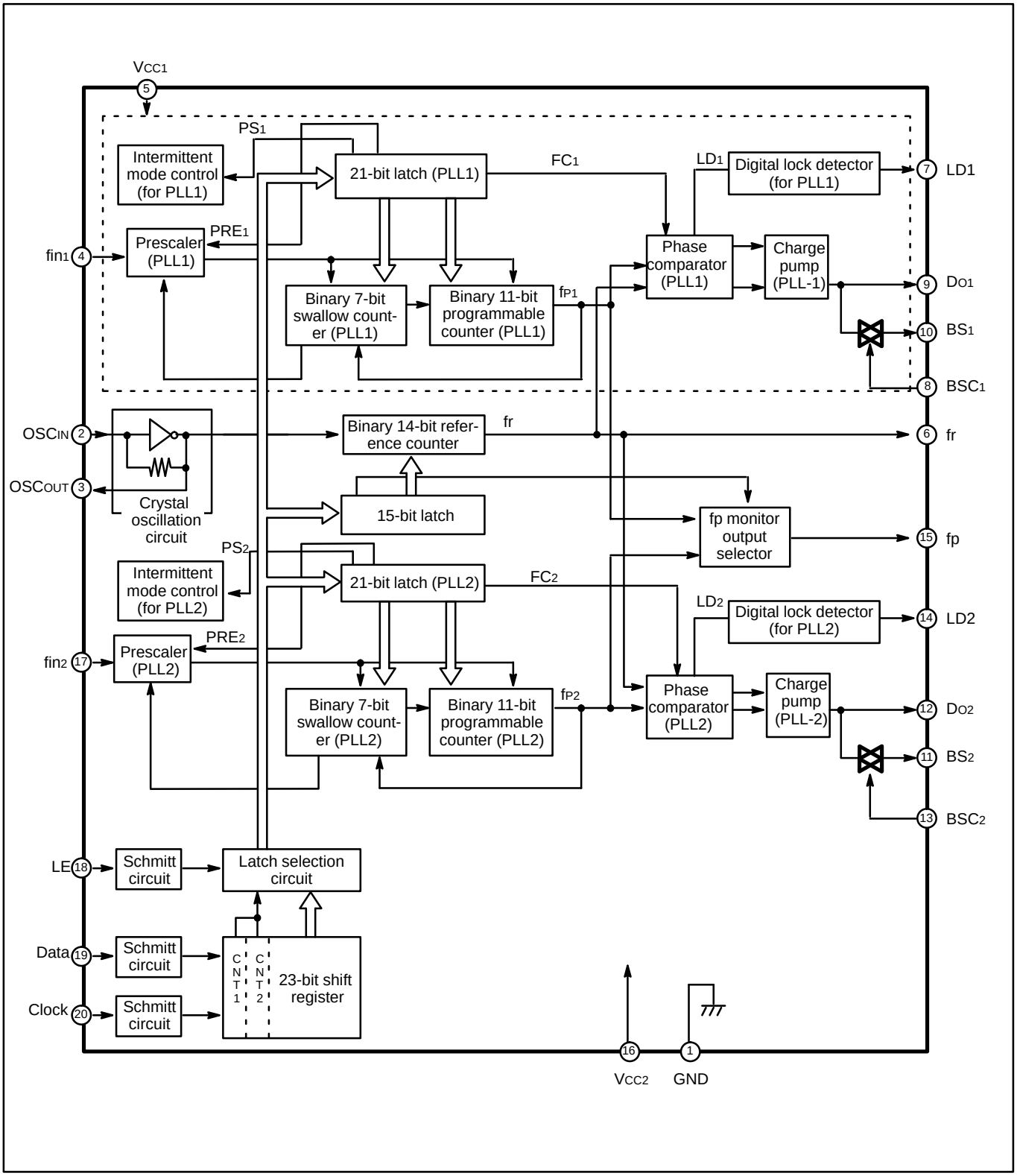
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Remark	Value	Unit
Power Supply Voltage	V_{CC}		–0.5 to 5.0	V
Output Voltage	V_{OUT}		–0.5 to V_{CC} +0.5	V
Open Drain Voltage	V_{OOP}	fr, fp	–0.5 to + 5.0	V
Output Current	I_{OUT}		±10	mA
Storage Temperature	T_{STG}		–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



PIN DESCRIPTIONS

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>I/O</th><th>Descriptions</th></tr>
<tr><td>1</td><td>GND</td><td>–</td><td>Ground.</td></tr>
<tr><td>2
3</td><td>OSCIN
OSCOUT</td><td>I
O</td><td>Oscillator input pin.
Oscillator output pin.
A crystal is connected between OSCIN pin and OSCOUT pin.</td></tr>
<tr><td>4</td><td>fin1</td><td>I</td><td>Prescaler input pin of PLL1 section.
The connection with VCO should be AC.</td></tr>
<tr><td>5</td><td>VCC1</td><td>–</td><td>Power supply voltage input pin of PLL1 section.
When power is OFF, latched data of PLL1 section is cancelled.</td></tr>
<tr><td>6</td><td>fr</td><td>O</td><td>Monitor pin for programmable reference divider output. (Open drain output)</td></tr>
<tr><td>7</td><td>LD1</td><td>O</td><td>Lock detect signal output pin of PLL1 section.
<table>
<tr><td>Status</td><td>LD pin output level</td></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>8</td><td>BSC1</td><td>I</td><td>Analog switch control pin of PLL1 section.
<table>
<tr><td>BSC1</td><td>BS1 pin output</td></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>9</td><td>DO1</td><td>O</td><td>Charge pump output pin of PLL1 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>10</td><td>BS1</td><td>O</td><td>Analog switch output pin of PLL1 section, and controlled by BSC1.</td></tr>
<tr><td>11</td><td>BS2</td><td>O</td><td>Analog switch output pin of PLL2 section, and controlled by BSC2.</td></tr>
<tr><td>12</td><td>DO2</td><td>O</td><td>Charge pump output pin of PLL2 section.
Phase characteristics of the phase detector can be reversed depending upon FC-bit setting.</td></tr>
<tr><td>13</td><td>BSC2</td><td>I</td><td>Analog switch control pin of PLL2 section.
<table>
<tr><td>BSC2</td><td>BS2 pin output</td></tr>
<tr><td>L</td><td>High-impedance</td></tr>
<tr><td>H</td><td>Charge pump output</td></tr>
</table></td></tr>
<tr><td>14</td><td>LD2</td><td>O</td><td>Lock detection signal output pin of PLL2 section.
<table>
<tr><td>Status</td><td>LD pin output level</td></tr>
<tr><td>Lock</td><td>H</td></tr>
<tr><td>Unlock</td><td>L</td></tr>
</table></td></tr>
<tr><td>15</td><td>fp</td><td>O</td><td>Monitor pin for programmable divider output. (Open drain output)
This pin outputs divided frequency of PLL1 section or PLL2 section depending upon FP bit setting.
<table>
<tr><td>FP bit</td><td>Output</td></tr>
<tr><td>H</td><td>PLL1 section (fp1)</td></tr>
<tr><td>L</td><td>PLL2 section (fp2)</td></tr>
</table></td></tr>
</table>

PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	I/O	Descriptions
16	$V_{CC}2$	–	Power supply voltage input pin for PLL2 section, programmable reference divider, shift register, and crystal oscillator. When power is OFF, latched data of PLL2 section and reference counter is cancelled.
17	fin2	I	Prescaler input pin of PLL2 section. The connection with VCO should be AC.
18	LE	I	Load enable input pin. This pin is followed by a schmitt trigger circuit. When this pin is high, the data stored in the shift register is transferred into the latch depending on a control data.
19	Data	I	Serial data input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. The stored data in the shift register is transferred to one of PLL1 programmable counter, PLL2 programmable counter and programmable reference counter depending upon control data settings.
20	Clock	I	Clock input pin of 23-bit shift register. This pin is followed by a schmitt trigger circuit. On rising edge of the clock, one bit of data is transferred into the shift register.

FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled ocillator (VCO)

P: Preset divide ratio of dual modulus prescaler (64 or 128)

N: Preset divide ratio of binary 11-bit programmable counter (16 to 2,047)

A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)

f_{OSC}: Reference oscillation frequency

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16,383)

FUNCTIONAL DESCRIPTIONS

SERIAL DATA INPUT

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable counters of PLL1 section and PLL2 section, and programmable reference counter are controlled individually.
Serial data of binary data is entered via Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Control bits		Destination of serial data
CN1	CN2	
L	L	Reference counter
L	H	Programmable counter of PLL1
H	H	Programmable counter of PLL2

SHIFT REGISTER CONFIGURATION

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
CN1	CN2	FP	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14

R1 to R14 : Divide ratio setting bit for the programmable counter (8 to 16,383)
FP : Test purpose bit (monitor output fp1/fp2 selection)
CN1, 2 : Control bit

Programmable Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	PS	PRE	FC	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

N1 to N11 : Divide ratio setting bit for the programmable counter (16 to 2,047)
A1 to A7 : Divide ratio setting bit for the swallow counter (0 to 127)
FC : Phase control bit for the phase detector
PRE : Divide ratio setting bit for the prescaler (64/65, 128/129)
PS : Power saving control bit
CN1, 2 : Control bit

BINARY 14-BIT PROGRAMMABLE REFERENCE COUNTER DATA SETTING

Divide Ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 8 is prohibited.
• Divide ratio (R) range = 8 to 16383

BINARY 11-BIT PROGRAMMABLE COUNTER DATA SETTING

Divide Ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 16 is prohibited.
• Divide ratio (N) range = 16 to 2047

BINARY 7-BIT SWALLOW COUNTER DATA SETTING

Divide Ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

PRESCALER DATA SETTING

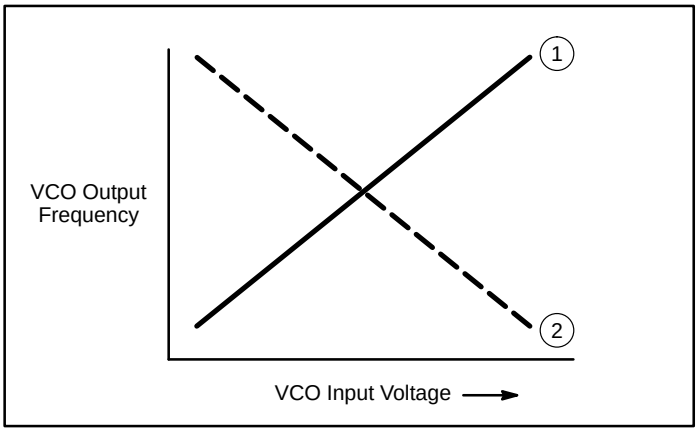
Divide Ratio	PRE
64/65	1
128/129	0

Note: • Divide ratio for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.

PHASE COMPARATOR PHASE CONTROL DATA SETTING

	FC = H	FC = L
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO Polarity	①	②

Note: • Z = High-impedance
• Depending upon the VCO polarity, FC bit should be set.
• Phase characteristic for each PLL1 and PLL2 is set by the serial data at that time of divide ratio setting for each programmable divider.



POWER SAVING FUNCTION CONTROL (INTERMITTENT OPERATION)

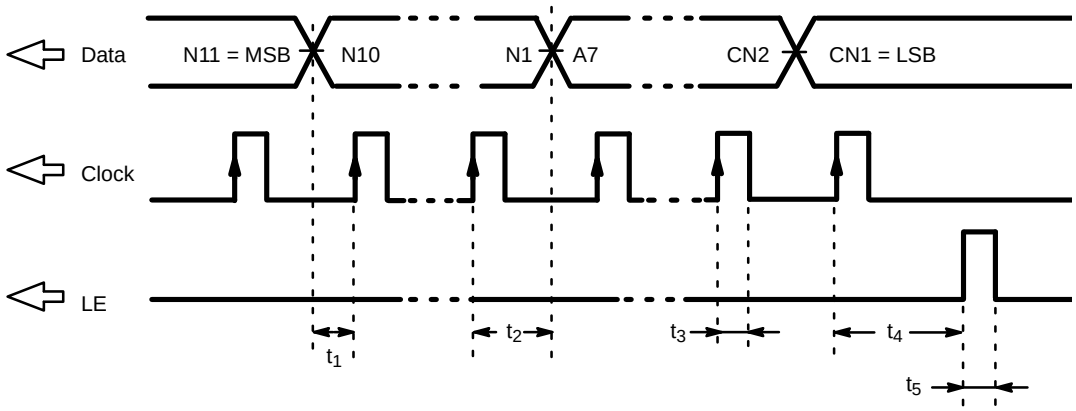
	PS	
	H	L
PLL1's section	ON	OFF
PLL2's section and common section	ON	OFF

Note:
- Power saving mode for each PLL1 and PLL2 is selected by the serial data at that time of divide ratio setting for each programmable divider.
- Common section ; Crystal oscillator circuit, reference counter
- Just after powering up, please set PS bit to "L" at first.

Intermittent operation limits power consumption by shutting down or start the internal circuits case by case. If device operation resumes uncontrolled, the error signal output from the phase comparator may exceed the limit due to an undefined phase relationship between the reference frequency (f_R) and the comparison frequency (f_P) and frequency lock is lost. To prevent this, an intermittent operation control circuit is provided to decrease the variation in the locking frequency by forcibly correcting phase of both frequencies to limit the error signal output.

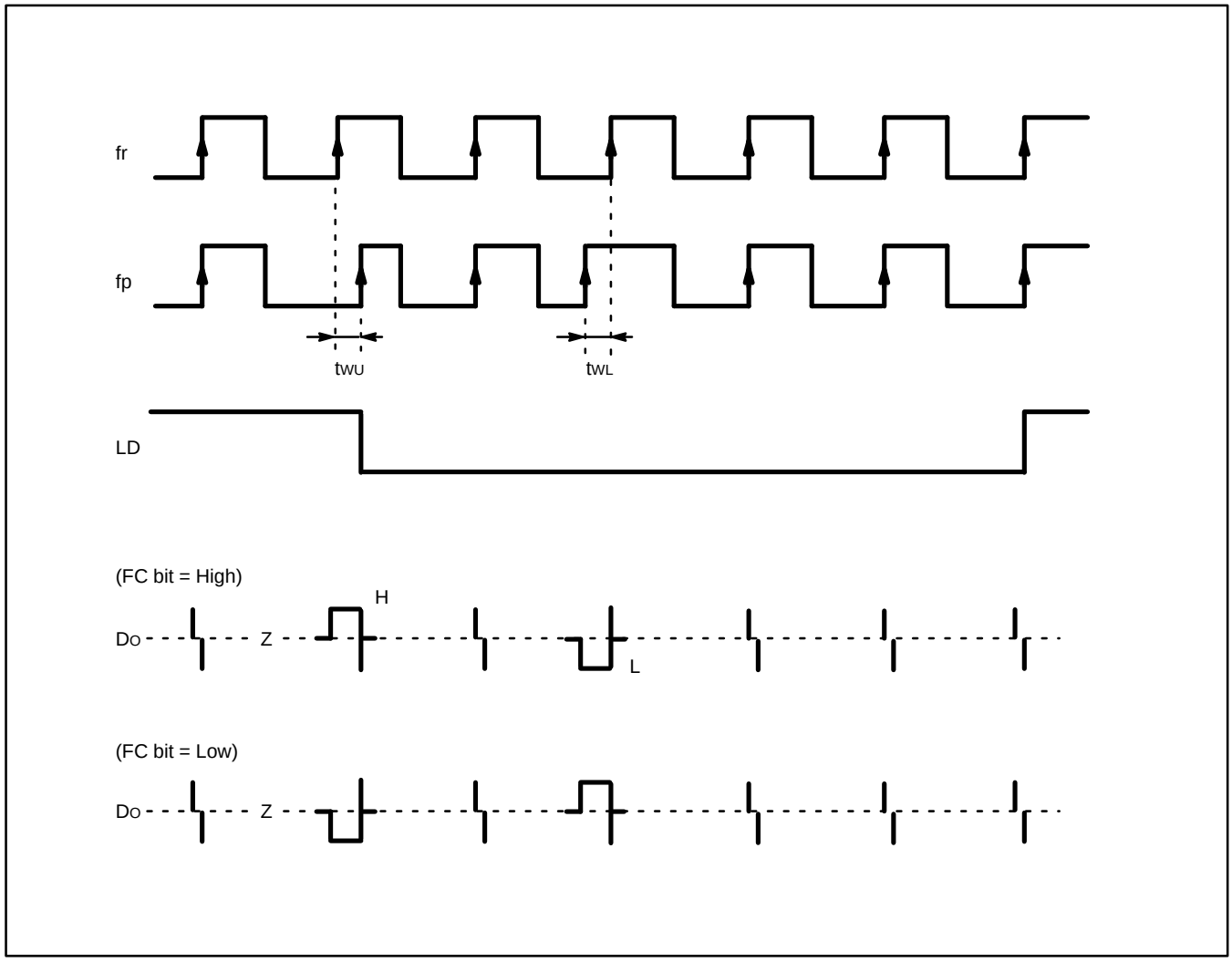
SERIAL DATA INPUT TIMING

t1 (>100ns) : Data set up time t2 (>1000ns) : Data hold time t3 (>300ns) : Clock pulse width
t4 (>100ns) : LE set up time to the rising edge of the last clock t5 (>800ns) : LE pulse width



On rising edge of the clock, one bit of the data is transferred into the shift register.

PHASE DETECTOR OUTPUT WAVEFORM



Note:
- Phase error detection range = –2π to +2π
- LD output becomes low when phase error is twU or more.
- LD output becomes high when phase error is twL or less and continues to be so for three cysles or more.
- twL and twL depend on OSCin input frequency.
  twU ≧8/fosc (e. g. twU ≧625ns, foscin = 12.8 MHz)
  twL ≦16/fosc (e. g. twL ≦1250ns, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power Supply Voltage	V_{CC}	2.7	3.0	3.5	V	$V_{CC}1 = V_{CC}2$
Input Voltage	V_{IN}	GND	–	V_{CC}	V	
Operating Temperature	Ta	–30	–	+80	°C	

HANDLING PRECAUTIONS

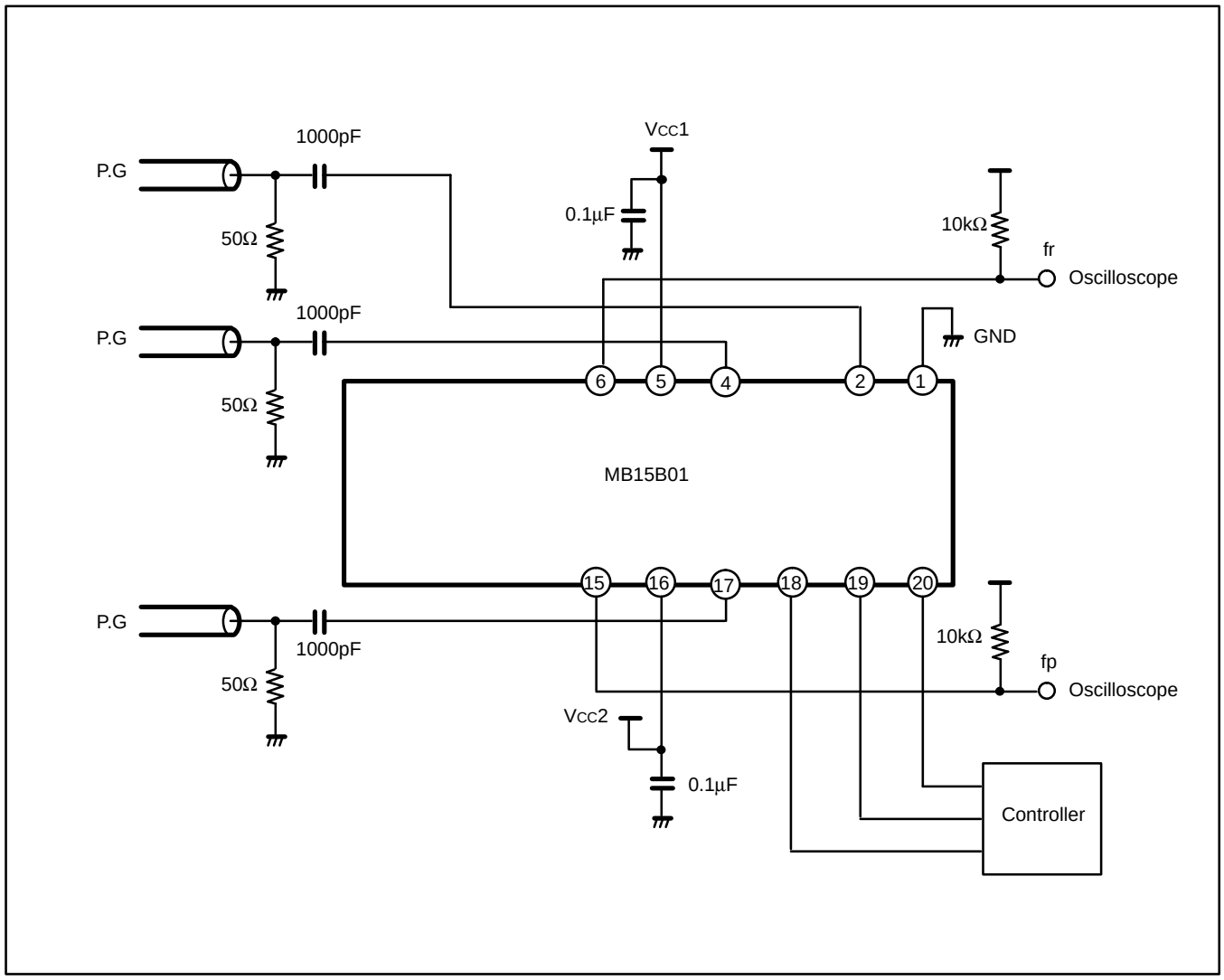
- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover work-benches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

ELECTRICAL CHARACTERISTICS

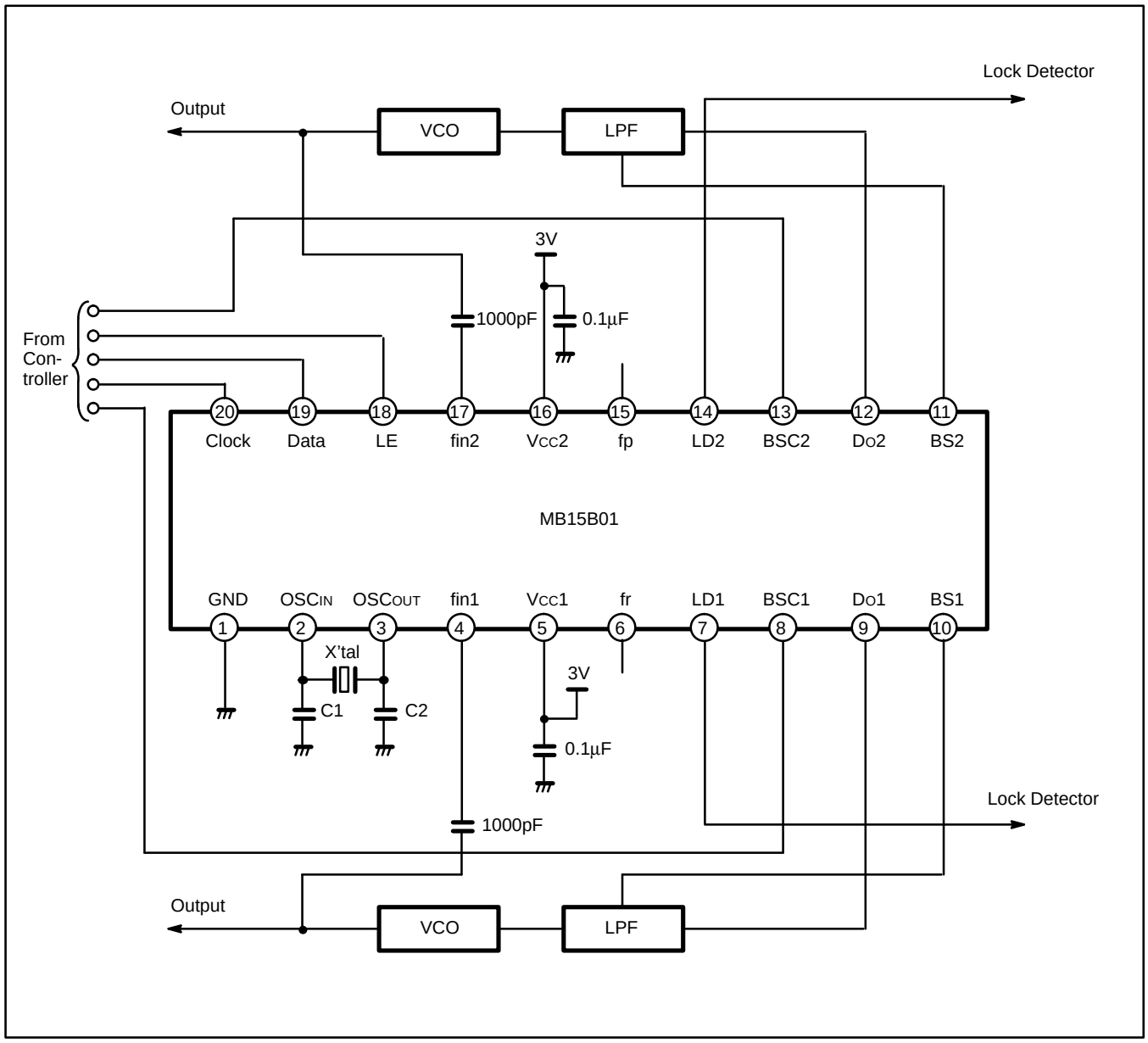
Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power Supply Current		$I_{CC}1$	PLL1 section	–	6.0 (0.1)*1	–	mA
		$I_{CC}2$	PLL2 & common sections	–	7.0 (0.1)*1	–	
Operating Frequency	fin	fin		100	–	1100	MHz
	OSC_{IN}	f_{OSC}		–	12.8	20.0	
Input Sensitivity	fin	Pfin	50Ω	–10	–	0	dBm
	OSC_{IN}	V_{OSC}		0.5	–	–	Vp-p
High–level Input Voltage	Data, Clock LE, BSC	V_{IH}		V_{CC}x0.7+0.4	–	–	V
Low-level Input Voltage		V_{IL}		–	–	V_{CC}x0.3–0.4	
High–level Input Current	Data, Clock LE, BSC	I_{IH}		–	1.0	–	µA
Low-level Input Current		I_{IL}		–	–1.0	–	
Input Current	OSC_{IN}	I_{OSC}		–	±50	–	
High–level Output Voltage	LD	V_{OH}	V_{CC} = 3.0V	2.2	–	–	V
Low-level Output Voltage		V_{OL}	V_{CC} = 3.0V	–	–	0.4	
High–impedance Cutoff Current	D_O, BS	I_{OFF}		–	–	1.1	µA
Output Current	LD	I_{OH}		–1.0	–	–	mA
		I_{OL}		–	–	1.0	
	Do1, 2	I_{OH}	V_{CC} = 3.0V	–	–2.5	–	mA
		I_{OL}	V_{CC} = 3.0V	–	5.0	–	
Analog Switch ON Resistance		R_{ON}		–	50	–	Ω

*1 : The value in ( ) is power supply current in power saving mode.

TEST CIRCUIT (PRESCALER INPUT SENSITIVITY TEST)



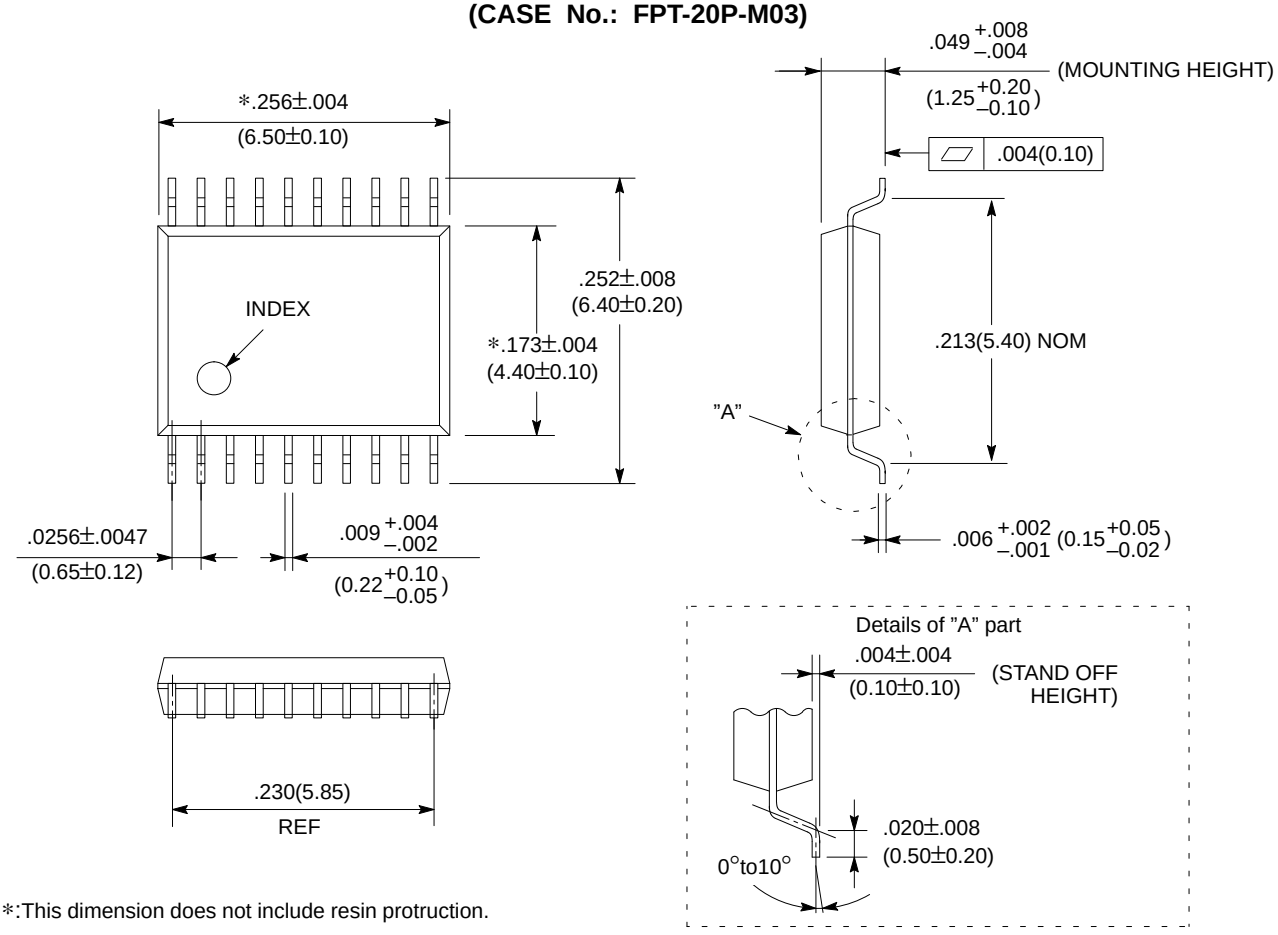
APPLICATION EXAMPLE



Note: C1, C2 : depends on a crystal oscillator.
Clock, Data, LE : involves a schmitt circuit.
When input pins are open, please insert the pull down/up resistor individually to prevent oscillation.

PACKAGE DIMENSION

20-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-20P-M03)



*:This dimension does not include resin protruction.

Dimensions in
inches (millimeters)

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