IC WORKS

W42C27

PRELIMINARY, November 1994

CPU Frequency Generator

FEATURES

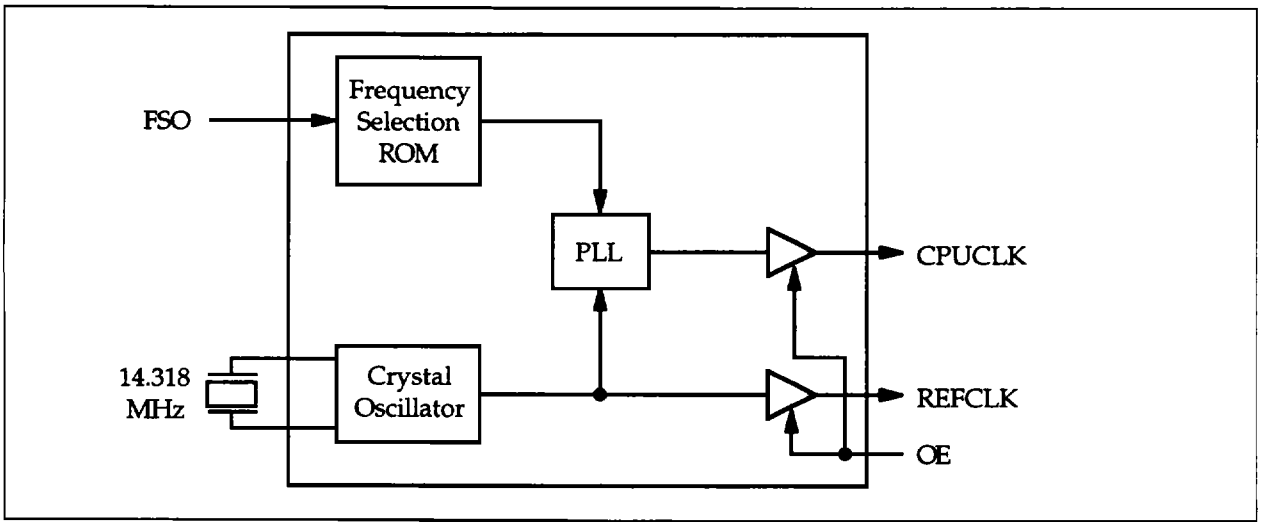
- Small 8 pin SOIC/DIP package
- W42C27-12 Supports PCI applications
  Selectable 25 or 33 MHz output
- W42C27-13 supports Fibre Channel applications - Generates 106.25 MHz for FC-AL chip sets
- Custom options available with metal layer changes
- 3.3V and 5V operation supported
- New proprietary crystal oscillator circuitry provides low REFOUT jitter, excellent duty cycle
- Integral PLL loop filter components ensure stable PLL operation in noisy system environment
- Output clocks are TTL and CMOS level compatible
- High performance, low power CMOS

FUNCTIONAL DESCRIPTION

The W42C27 is a low cost, small-footprint general purpose clock generator IC. This single-PLL clock device incorporates an improved crystal oscillator and provides up to two output clocks. On-chip loop filter components ensure stable operation even with the noise typical of a digital system. Device functionality, including input/output options and frequency selection, is determined by a single metal mask that allows quick-turn customization capability. Both 3.3 and 5 Volt operation is supported.

The W42C27-12 option supports PCI clock applications with its selectable 25 or 33 MHz output. Its 14.318 MHz reference clock can be derived from the 14.318 MHz output from another clock device. The W42C27-13 is useful for FC-AL (Fibre Channel Arbitrated Loop) applications that require a 106.25 MHz reference clock.

FUNCTIONAL BLOCK DIAGRAM: W42C27-12



W42C27-12 OPTION DESCRIPTION

The standard W42C27-12 option provides a selectable 25 or 33 MHz clock output that is useful for PCI clock applications. Like other IC WORKS clock devices, for frequency reference the W42C27-12 can utilize an external 14.318 MHz crystal, or it can use an externally generated 14.318 MHz clock signal. Therefore, in non-synchronous PCI/CPU system applications, the W42C27-12 can use the 14.318 MHz output from the main system clock, such as the W48C54, thereby eliminating the need for an extra crystal. The IC WORKS W40C06 Clock Buffer is ideal for distribution of the 33 MHz PCI clock generated by the W42C27-12.

W42C27-13 OPTION DESCRIPTION

The standard W42C27-13 option provides a fixed 106.25 MHz output clock that is useful in FC-AL (Fibre Channel Arbitrated Loop) applications. FC-AL chip sets, such as the Vitesse VSC7105/7106, require a 106.25 MHz input reference clock.

Unlike other IC WORKS' clock products, the W42C27-14 requires a 17.0 MHz crystal or reference clock source. To maintain the 106.25 MHz +/- 50 ppm accuracy required by FC-AL applications, the 17.0 MHz crystal needs to be controlled to within +/- 50 ppm (the 106.25 MHz output is derived by the PLL ratio of 25/4 x 17.0 MHz). To facilitate precise frequency control of the crystal oscillator, external crystal load capacitors are used and required with the W42C27-13 option; no internal load capacitors are implemented at device pin X1 or X2 (again unlike other IC WORKS' clock devices). The required load capacitance value for accurate crystal oscillation frequency is specified by the crystal manufacturer. Stray capacitance of X1 and X2 is about 5 pf. To ensure minimal jitter from the W42C27-13 (target maximum absolute jitter from CLKOUT is +/- 100 ppm) only one clock output is provided (there is no REFCLK output).

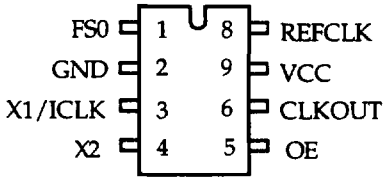
IMPROVED CRYSTAL OSCILLATOR CIRCUIT

The W42C27 incorporates a new crystal oscillator circuit designed to provide 50% duty cycle over a range of operating conditions including the addition of external crystal load capacitors to pins X1 and X2. (Crystal load capacitance is sometimes increased to match a particular crystal load requirement when absolute frequency accuracy is important.) Duty cycle is also maintained when using an external clock source (connected to pin X1, pin X2 is left open), as long as the external clock has good duty cycle.

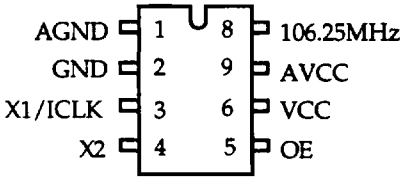
Crystal load capacitance of the W42C27 is about 10 pf (excluding the W42C27-13 option), which is becoming an industry standard. This helps to control frequency accuracy, assuming that a crystal which specifies a 10 pf load condition is used. The circuit exhibits about 50% less clock jitter from the REFCLK output when compared to similar devices.

PIN CONFIGURATIONS:

W42C27-12
Top View



W42C27-13
Top View



Note 2: Not guaranteed when Vcc < 4.5V.

FREQUENCY SELECTION :

ω42C27-12

INPUT = 14.318 MHz

Select Address	CLKOUT
FS0	(MHz)
0	25
1	33.3

ω42C27-13

INPUT = 17.0 MHz

CLKOUT = 106.25 MHz

PIN DESCRIPTIONS: ω42C27

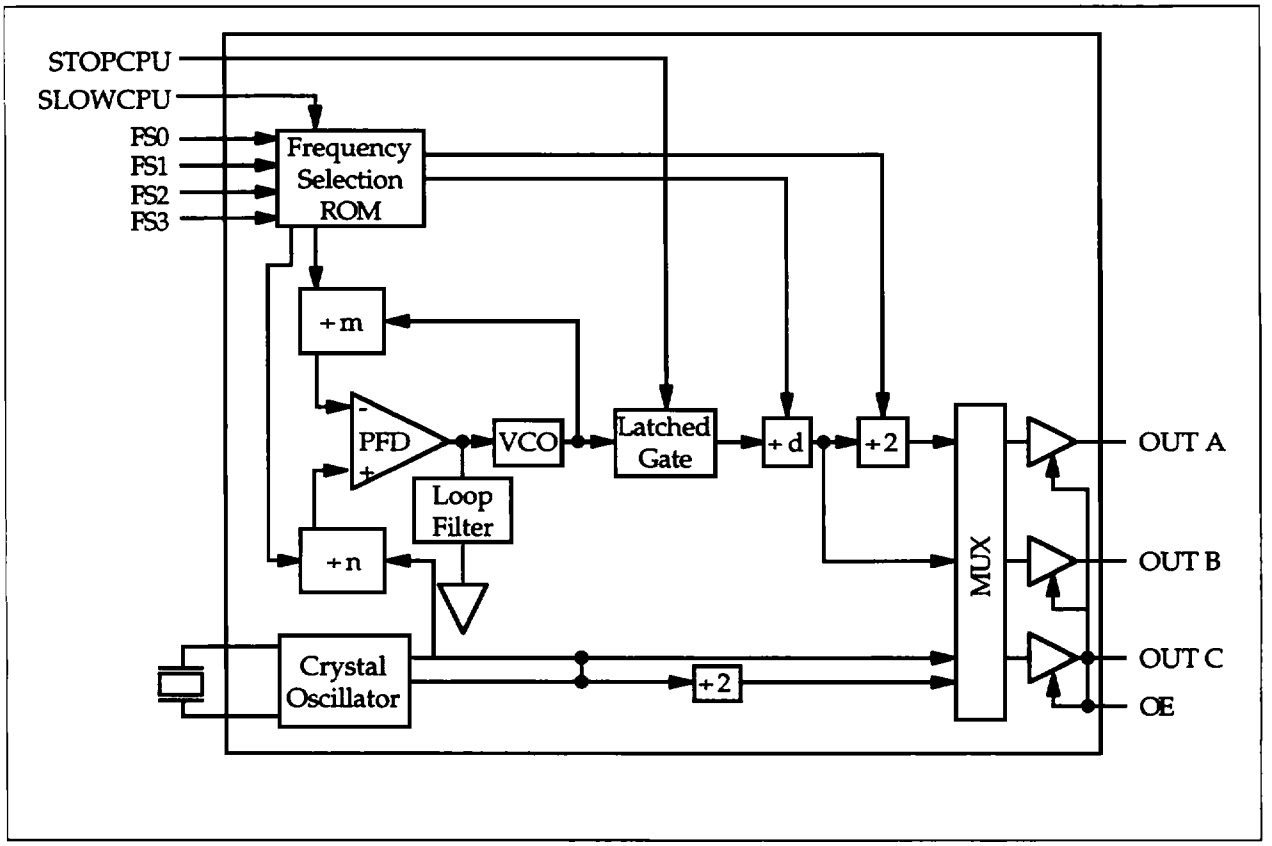
Pin Name	Input/ Output	Function
106.25 MHz	O	106.25 MHz reference clock for FC-AL chip sets
AGND	-	Analog ground connection
AVCC	-	Analog power supply connection
CLKOUT	O	Clock output (refer to Frequency Selection Table)
FS0	I	Frequency Selection input, (1)
GND	-	Ground connection
OE	I	Output Enable, puts clock outputs in high impedance state when low, (1)
REFCLK	O	Reference Clock output, outputs crystal or input clock frequency (14.318 MHz)
VCC	-	Power supply connection
X1/ICLK	I	Crystal connection or external clock frequency input (14.318 MHz)
X2	O	Crystal connection, leave this pin unconnected when using external clock

Note 1: All inputs, except for X1/ICLK, have an internal pull-up resistor. Unconnected inputs will assume a logic high condition.

W42C27 CUSTOMIZATION

As with other IC WORKS' clock generator devices, the W42C27 is mask customizable to fit individual needs. Customizable features include frequency selection and various input and output functions. Please contact IC WORKS for further information.

FUNCTIONAL BLOCK DIAGRAM: W42C27 BASE FEATURE SET



ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Voltage on Any Pin with Respect to Ground	$V_{CC}V_{IN}$	-0.5 to 7.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Ambient Temperature Under Bias	T_B	-55 to +125	°C
Operating Temperature	T_A	0 to +70	°C

Note 1: Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AT 5.0V

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5\ V \pm 10\ \%$)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Note 2			25mA	mA
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = .1$ mA	Vcc - .4V			V
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4			V
Input Capacitance	C_I	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		10		pF
Input Low Current	I_{IL}	$V_{IN} = 0V$ (incls pull-up resistor)			-100	µA
Input High Current	I_{IH}	$V_{IN} = V_{CC}$			10	µA
Input Pull-Up Resistor	R_P	$V_{IN} = 0V$		250		kΩ

Note 2: ɯ42C27-12 with no load, with 14.318 MHz crystal input, and CPUCLK running at 33 MHz. Power supply current varies with frequency.

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\ \%$)

Parameter	Symbol	Min	Typ	Max	Unit
Output Frequency	F_O	2		120	MHz
Input Frequency	F_I	2	14.318	32	MHz
Output Rise Time, 0.8 to 2.0V, 25pF Load	T_R		1	2	ns
Output Rise Time, 20 to 80% V_{CC}, 25pF Load	T_R		2	4	ns
Output Fall Time, 2.0 to 0.8V, 25pF Load	T_F		1	2	ns
Output Fall Time, 80 to 20% V_{CC}, 25pF Load	T_F		2	4	ns
Duty Cycle, 15pF Load	D_T	40	50	60	%
Jitter, 1 Sigma, All Frequencies	T_{J1S}			± 150	ps
Jitter, Absolute, All Frequencies	T_{JABS}			± 250	ps
Powerup Time, Off to stated output frequency	T_{PU}		15	30	ms

ELECTRICAL CHARACTERISTICS AT 3.3V

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 3.3V \pm 10\%$) (Note 2)

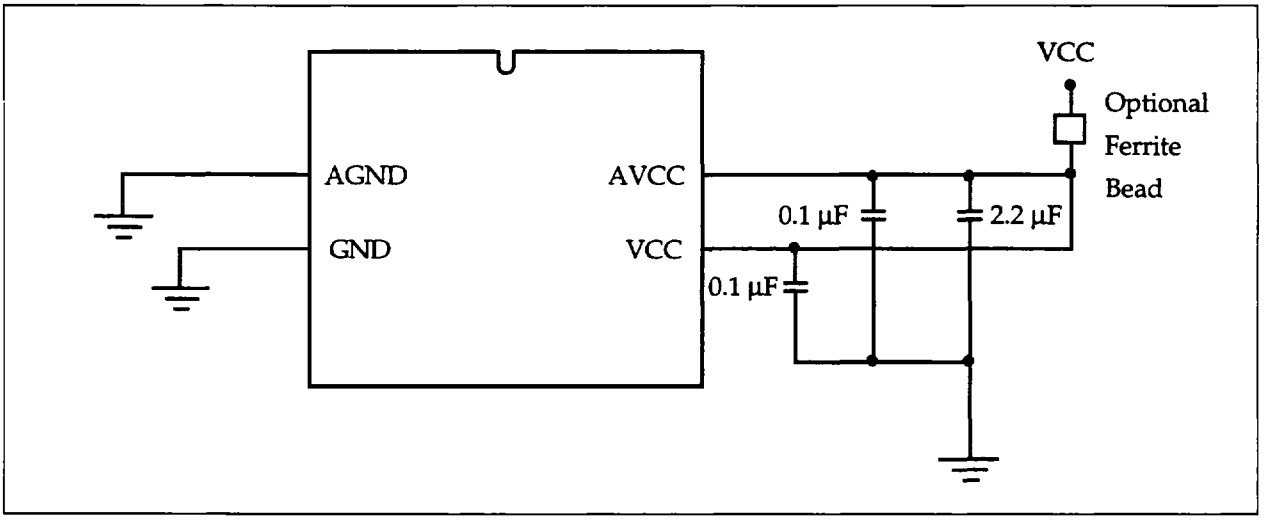
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current	I_{CC}	Note 2			20mA	mA
Input Low Voltage	V_{IL}				0.15Vcc	V
Input High Voltage	V_{IH}		0.7Vcc			V
Output Low Voltage	V_{OL}	$I_{OL} = 8$ mA			0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4			V
Input Capacitance	C_I	Except X1, X2			10	pF
Load Capacitance	C_L	Pins X1, X2		10		pF
Input Low Current	I_{IL}	V_{IN} = 0V (includes pull-up res.)			-100	µA
Input High Current	I_{IH}	V_{IN} = Vcc			10	µA
Input Pull-Up Resistor	R_P	V_{IN} = 0V		250		kΩ

Note 2: W42C27-12 with no load, with 14.318 MHz crystal input, and CLK1 running at 33 MHz. Power supply current varies with frequency and output load capacitance.

AC CHARACTERISTICS ($0°C \le T_A \le 70°C$, $V_{CC} = 3.3V \pm 10\%$)

Parameter	Symbol	Min	Typ	Max	Unit
Output Frequency (CPUCLK)	F_O	2		80	MHz
Input Frequency	F_I	2	14.318	32	MHz
Input Clock Rise Time	$ICLK_R$			20	ns
Input Clock Fall Time	$ICLK_F$			20	ns
Output Rise Time, 20 to 80% Vcc, 15pF load	T_R		2	4	ns
Output Fall Time, 80 to 20% Vcc, 15pF Load	T_F		2	4	ns
Duty Cycle, 15pF Load	D_T	40	50	60	%
Jitter, 1 Sigma, All Frequencies	T_{J1S}			± 150	ps
Jitter, Absolute, All Frequencies	T_{JABS}			± 250	ps
Powerup Time, Off to stated output frequency	T_{PU}		15	30	ms

RECOMMENDED CIRCUIT CONFIGURATION



RECOMMENDED BOARD LAYOUT: ICW42C27

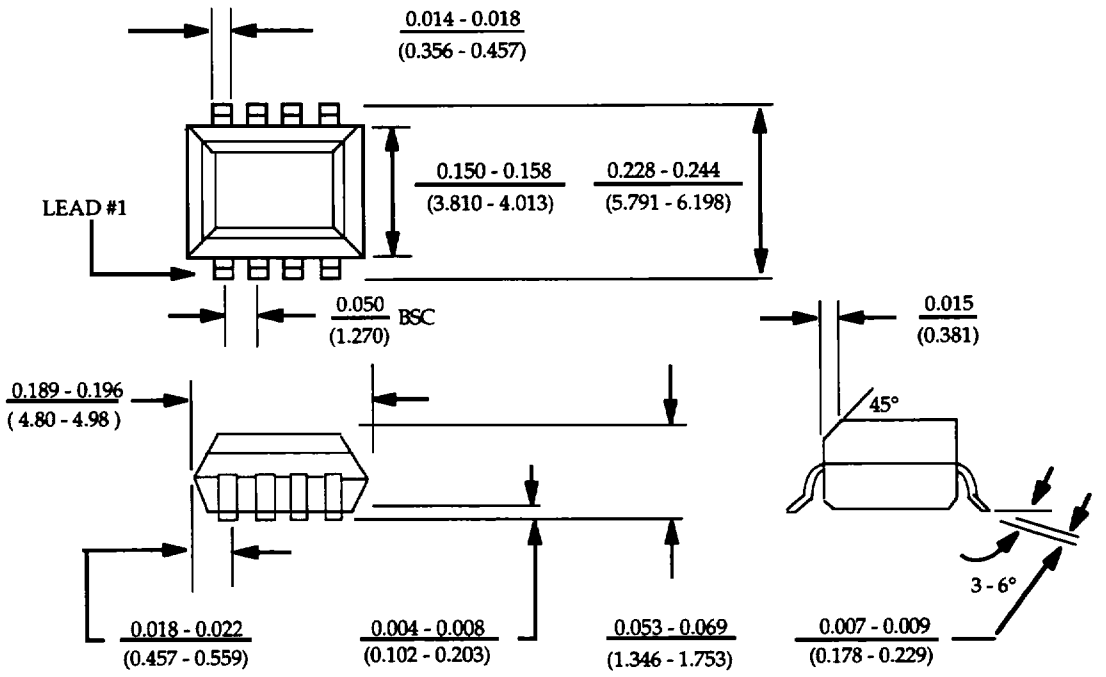
For optimum performance in system applications, the above power supply decoupling scheme should be used. GND pins are connected directly to the ground plane.

VCC decoupling is important to reduce phase jitter and EMI radiation. The 0.1µF decoupling capacitor should be placed as close to each VCC pin as possible, otherwise the increased trace inductance will negate its decoupling capability. The 2.2µF decoupling capacitor shown is optional but will improve power supply rejection. For further EMI protection, the VCC connection can be made via a ferrite bead, as shown above.

When using the ICW42C27, unused input select pins may be tied to either ground or VCC, or may be left unconnected; since internal pull-up resistors are incorporated on all logic input pins, an unconnected input will assume a logic 1 condition. Output clocks should use a series termination resistor (about 33 ohms) placed as close to the clock outputs as possible; this will also help to decrease jitter, EMI and clock signal ringing.

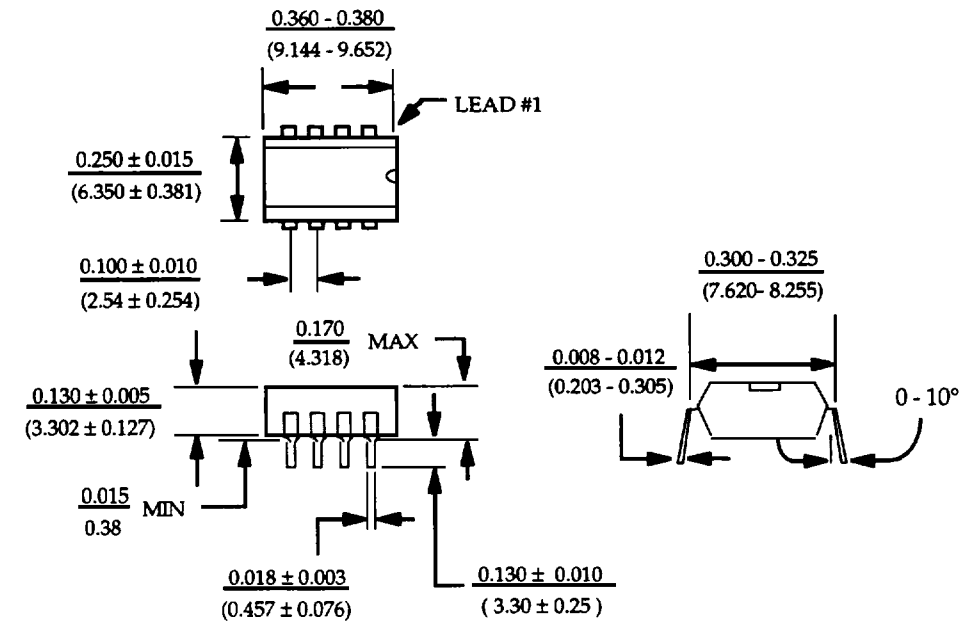
PACKAGING INFORMATION

Plastic SOIC (8pin 150 mil)



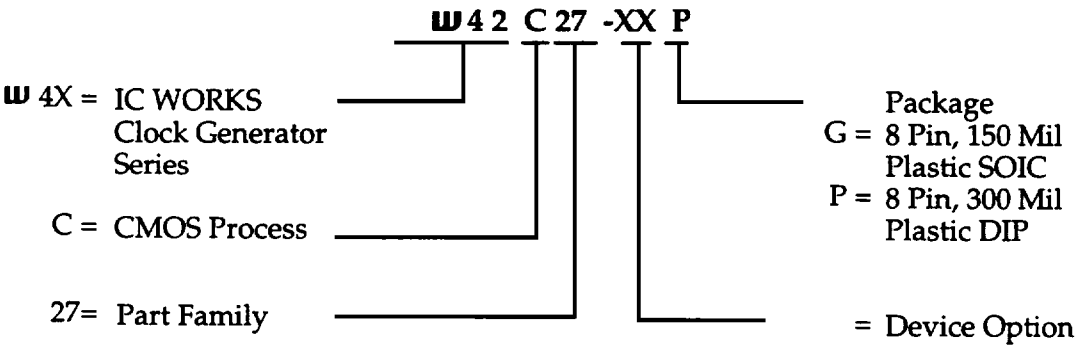
Note: All linear dimensions are in inches and parenthetically in millimeters, min-max.

Plastic DIP (8 pin 300 mil)



Note: All linear dimensions are in inches and parenthetically in millimeters, min-max.

ORDERING INFORMATION



VALID PART NUMBERS

W42C27-12
W42C27-13

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