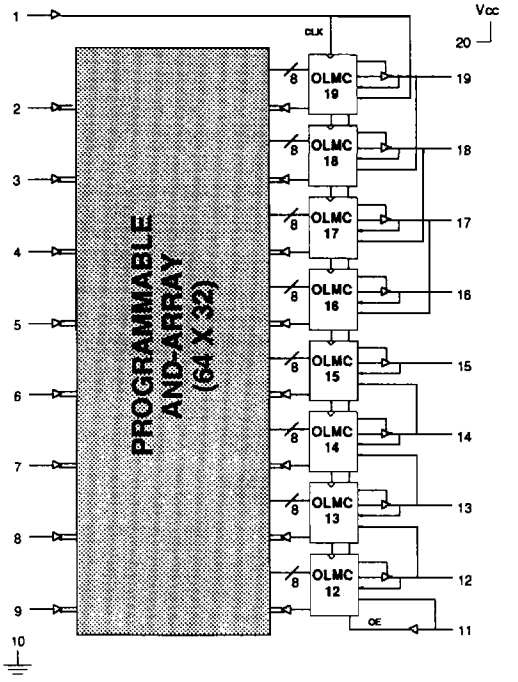
GAL16V8B
GAL16V8A

High Performance E²CMOS PLD

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **7.5 ns Maximum Propagation Delay**
  - **Fmax = 100 MHz**
  - **5 ns Maximum from Clock Input to Data Output**
  - **TTL Compatible 24 mA Outputs**
  - **UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **75mA Typ Icc on Low Power Device**
  - **45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS (GAL16V8B)**
- **E² CELL TECHNOLOGY**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **100% Tested/Guaranteed 100% Yields**
  - **High Speed Electrical Erasure (<100ms)**
  - **20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - ***Maximum Flexibility for Complex Logic Designs***
  - **Programmable Output Polarity**
  - **Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **DMA Control**
  - **State Machine Control**
  - **High Speed Graphics Processing**
  - **Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

FUNCTIONAL BLOCK DIAGRAM



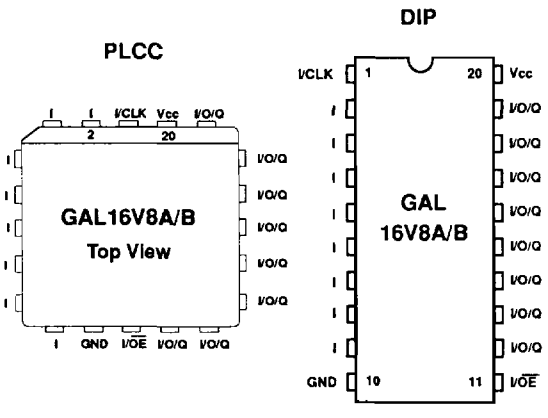
DESCRIPTION

The GAL16V8B, at 7.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E^2) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8A/B are the PAL architectures listed in the table of the macrocell description section. GAL16V8A/B devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

PIN CONFIGURATION



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December 1991

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} .....–0.5 to +7V
Input voltage applied .....–2.5 to V_{CC} +1.0V
Off-state output voltage applied .....–2.5 to V_{CC} +1.0V
Storage Temperature .....–65 to 150°C
Ambient Temperature with
Power Applied .....–55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) .....0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground .....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
I_{IL}[1]	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \le V_{IN} \le V_{CC}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	24	mA
I_{OH}	High Level Output Current		—	—	–3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 25MHz Outputs Open (no load)	—	75	115	mA

1) The leakage current is due to the internal pull-up resistor on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25 C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	8	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION		-7		-10		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd}	1	*Input or I/O to Combinational Output*	*8 outputs switching*	3	7.5	3	10	ns
			1 output switching	—	7	—	—	ns
t_{co}	1	Clock to Output Delay		2	5	2	7	ns
t_{cf}[2]	—	Clock to Feedback Delay		—	3	—	6	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑		7	—	10	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑		0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)		83.3	—	58.8	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)		100	—	62.5	—	MHz
	1	Maximum Clock Frequency with No Feedback		100	—	62.5	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High		5	—	8	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low		5	—	8	—	ns
t_{en}	2	Input or I/O to Output		3	9	3	10	ns
	2	OE↓ to Output		2	6	2	10	ns
t_{dis}	3	Input or I/O to Output		2	9	2	10	ns
	3	OE↑ to Output		1.5	6	1.5	10	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

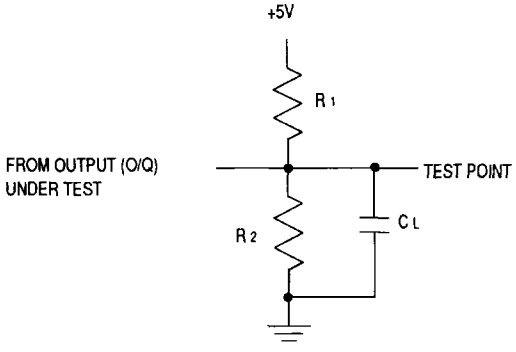
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{CC} ..... –0.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. *Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).*

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION			MIN.	TYP.[2]	MAX.	UNITS
V_{IL}	Input Low Voltage				Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage				2.0	—	Vcc+1	V
I_{IL}	Input or I/O Low Leakage Current	$0V \le V_{IN} \le V_{IL}$ (MAX.)			—	—	-10	µA
I_{IH}	Input or I/O High Leakage Current	$V_{IH} \le V_{IN} \le V_{CC}$			—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}			—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}			2.4	—	—	V
I_{OL}	Low Level Output Current				—	—	24	mA
I_{OH}	High Level Output Current				—	—	–3.2	mA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V	V_{OUT} = 0.5V	T_A = 25°C	–30	—	–150	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V Outputs Open (no load)	f_{toggle} = 15MHz	L -25	—	75	90	mA
			f_{toggle} = 25MHz	L -10/-15	—	75	115	mA
			f_{toggle} = 15MHz	Q -15/-25	—	45	55	mA

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and T_A = 25 °C

CAPACITANCE (T_A = 25 C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	-10		-15		-25		UNITS
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
tpd	1	Input or I/O to Combinational Output	3	10	3	15	3	25	ns
tco	1	Clock to Output Delay	2	7	2	10	2	12	ns
tcf[2]	—	Clock to Feedback Delay	—	7	—	8	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	15	—	ns
th	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	0	—	ns
fmax[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	58.8	—	45.5	—	37	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	50	—	40	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	41.6	—	MHz
twh[4]	—	Clock Pulse Duration, High	8	—	8	—	12	—	ns
twl[4]	—	Clock Pulse Duration, Low	8	—	8	—	12	—	ns
ten	2	Input or I/O to Output Enabled	—	10	—	15	—	25	ns
	2	OE↓ to Output Enabled	—	10	—	15	—	20	ns
tdis	3	Input or I/O to Output Disabled	—	10	—	15	—	25	ns
	3	OE↑ to Output Disabled	—	10	—	15	—	20	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Descriptions** section.
3) Refer to **fmax Descriptions** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

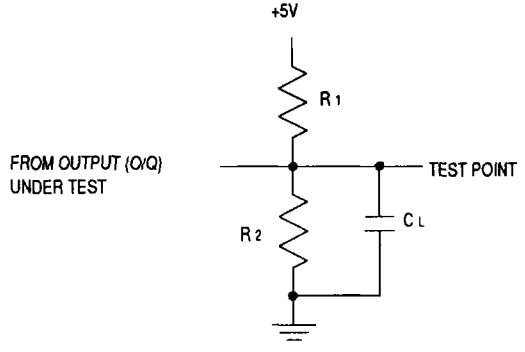
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R1	R2	CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF



C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

GAL16V8A/B ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
7.5	7	5	115	GAL16V8B-7LP	20-Pin Plastic DIP
			115	GAL16V8B-7LJ	20-Lead PLCC
10	10	7	115	GAL16V8B-10LP	20-Pin Plastic DIP
			115	GAL16V8B-10LJ	20-Lead PLCC
			115	GAL16V8A-10LP	20-Pin Plastic DIP
			115	GAL16V8A-10LJ	20-Lead PLCC
15	12	10	55	GAL16V8A-15QP	20-Pin Plastic DIP
			55	GAL16V8A-15QJ	20-Lead PLCC
			115	GAL16V8A-15LP	20-Pin Plastic DIP
			115	GAL16V8A-15LJ	20-Lead PLCC
25	15	12	55	GAL16V8A-25QP	20-Pin Plastic DIP
			55	GAL16V8A-25QJ	20-Lead PLCC
			90	GAL16V8A-25LP	20-Pin Plastic DIP
			90	GAL16V8A-25LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
10	10	7	130	GAL16V8B-10LPI	20-Pin Plastic DIP
			130	GAL16V8B-10LJI	20-Lead PLCC
15	12	10	130	GAL16V8B-15LPI	20-Pin Plastic DIP
			130	GAL16V8B-15LJI	20-Lead PLCC
			130	GAL16V8A-15LPI	20-Pin Plastic DIP
			130	GAL16V8A-15LJI	20-Lead PLCC
20	13	11	65	GAL16V8A-20QPI	20-Pin Plastic DIP
			65	GAL16V8A-20QJI	20-Lead PLCC
25	15	12	65	GAL16V8A-25QPI	20-Pin Plastic DIP
			65	GAL16V8A-25QJI	20-Lead PLCC
			130	GAL16V8A-25LPI	20-Pin Plastic DIP
			130	GAL16V8A-25LJI	20-Lead PLCC

PART NUMBER DESCRIPTION