6A OPEN-DRAIN MOSFET DRIVER

FEATURES

- Independently-Programmable Rise and Fall Times
- High Peak Output Current ..... 6A Peak
- Low Output Impedance ..... 2.5Ω Typ
- High Speed t_R, t_F ..... <30 ns with 1800 pF Load
- Short Delay Times ..... 55ns Typ
- Wide Operating Range ..... 4.5V to 18V

APPLICATIONS

- Motor Controls
- Self-Commutating MOSFET Bridge Driver
- Driving Bipolar Transistors
- Driver for Nonoverlapping Totem Poles
- Reach-Up/Reach-Down Driver

RUGGED

- Tough CMOS Construction
- Latch-Up Protected: Will Withstand >1.5 mA Reverse Current (Either Polarity)
- Input Withstands Negative Swings Up to –5V
- ESD Protected 4kV

GENERAL DESCRIPTION

The TC4401 is a CMOS buffer-driver constructed with complementary MOS outputs, where the drains of the final output totem pole have been left disconnected so individual connections can be made to the pull-up and pull-down sections of the output. This allows the insertion of individual drain current-limiting resistors in the pull-up and pull-down sections of the output, thus allowing the user to define the rates of rise and fall times desired for a capacitive load, or a reduced output swing if driving a resistive load, or to limit base current when driving a bipolar transistor. Minimum rise and fall times, with no resistors, will be less than 30 ns for a 2500-pF load. There is no upper limit.

For driving MOSFETs in motor-control applications, where slow-on/fast-off operation is desired, the TC4401 is superior to the previously-used technique of adding a diode-resistor combination between the driver output and the MOSFET, because it allows accurate control of turn-on, while maintaining fast turn-off and maximum noise immunity for the device being driven.

When used to drive bipolar transistors, this driver maintains the high speeds common to other Teledyne drivers and allows insertion of a base current-limiting resistor, while providing a separate half-output for fast turn-off. By proper positioning of the resistor, either npn or pnp transistors can be driven.

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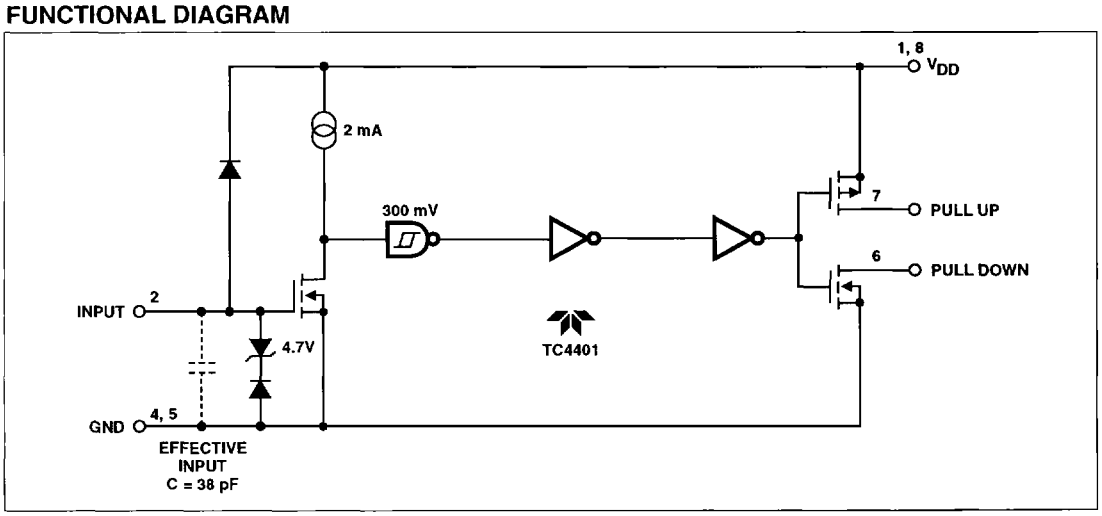
FUNCTIONAL DIAGRAM



TC4401

For driving many loads in low-power regimes, this driver, because it has very low quiescent current (<150 µA) and eliminates shoot-through currents in the output stage, requires significantly less power than similar drivers, and can be helpful in meeting low-power budgets.

Because neither drain in an output is dependent on the other (though they do switch simultaneously), this device can also be used as an open-drain buffer/driver where both drains are available in one device, thus minimizing chip count. An unused open drain should be returned to the supply rail its device source are connected to (pull-down to ground, pull-up to V_{DD}), to prevent static damage. Alternatively, in situations where timing resistors, or other means of limiting crossover currents are used, multiple TC4401's may be paralleled for greater current-carrying capacity.

The TC4401 is built using Teledyne Components' new Tough CMOS process and is capable of giving reliable service in the most demanding electrical environments: it will not latch under any conditions within its power and voltage ratings; it is not subject to damage when up to 5V of noise spiking of either polarity occurs on the ground pin; and it can accept, without damage or logic upset, up to 1.5 amp of reverse current (of either polarity) being forced back into the outputs. All terminals are fully protected against up to 2 kV of electrostatic discharge.

ORDERING INFORMATION

Part No.	Logic	Package	Temperature Range
TC4401CPA	Inverting	8-Pin PDIP	0°C to +70°C
TC4401EPA	Inverting	8-Pin PDIP	–40°C to +85°C
TC4401COA	Inverting	8-Pin SOIC	0°C to +70°C
TC4401EOA	Inverting	8-Pin SOIC	–40°C to +85°C
TC4401IJA	Inverting	8-Pin CerDIP	–25°C to +85°C
TC4401MJA	Inverting	8-Pin CerDIP	–55°C to +125°C

PIN CONFIGURATIONS

NC = NO CONNECTION

NOTE: 1. Duplicate pins must both be connected for proper operation.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +22V
Input Voltage ..... V_{DD} + 0.3V to GND - 5.0V
Input Current (V_{IN} > V_{DD}) 50mA
Power Dissipation, T_A ≤25°C
PDIP 1W
SOIC 500mW
CerDIP 800mW
Derating Factors (To Ambient)
PDIP ..... 8 mW/°C
SOIC ..... 4 mW/°C
CerDIP ..... 6.4 mW/°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Chip Temperature ..... +150°C
Operating Temperature Range
C Version ..... 0°C to +70°C
I Version ..... –25°C to +85°C
E Version ..... –40°C to +85°C
M Version ..... –55°C to +125°C

Lead Temperature (Soldering, 10 sec) ..... +300°C

Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

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ELECTRICAL CHARACTERISTICS: T_A = +25°C with 4.5V ≤ V_{DD} ≤ 18V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	1.8	—	V
V_{IL}	Logic 0 Low Input Voltage		—	1.3	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_{DD}	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.1	2.8	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	1.5	2.5	Ω
I_{PK}	Peak Output Current	V_{DD} = 18V	—	6	—	A
I_{REV}	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300 µs	>1.5	—	—	A
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	25	35	ns
t_{D1}	Delay Time	Figure 1	—	55	75	ns
t_{D2}	Delay Time	Figure 1	—	55	75	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 55	1.5 150	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

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ELECTRICAL CHARACTERISTICS:

Measured over operating temperature range with $4.5V \leq V_{DD} \leq 18V$, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
V_{IH}	Logic 1 High Input Voltage		2.4	—	—	V
V_{IL}	Logic 0 Low Input Voltage		—	—	0.8	V
V_{IN} (Max)	Input Voltage Range		–5	—	V_{DD}+0.3	V
I_{IN}	Input Current	$0V \leq V_{IN} \leq V_S$	–10	—	10	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	V_{DD}–0.025	—	—	V
V_{OL}	Low Output Voltage	See Figure 1	—	—	0.025	V
R_O	Output Resistance, High	I_{OUT} = 10 mA, V_{DD} = 18V	—	3	5	Ω
R_O	Output Resistance, Low	I_{OUT} = 10 mA, V_{DD} = 18V	—	2.3	5	Ω
Switching Time (Note 1)						
t_R	Rise Time	Figure 1, C_L = 2500 pF	—	32	60	ns
t_F	Fall Time	Figure 1, C_L = 2500 pF	—	34	60	ns
t_{D1}	Delay Time	Figure 1	—	50	100	ns
t_{D2}	Delay Time	Figure 1	—	65	100	ns
Power Supply						
I_S	Power Supply Current	V_{IN} = 3V V_{IN} = 0V	— —	0.45 60	3 400	mA µA
V_{DD}	Operating Input Voltage		4.5	—	18	V

NOTE: 1. Switching times guaranteed by design.

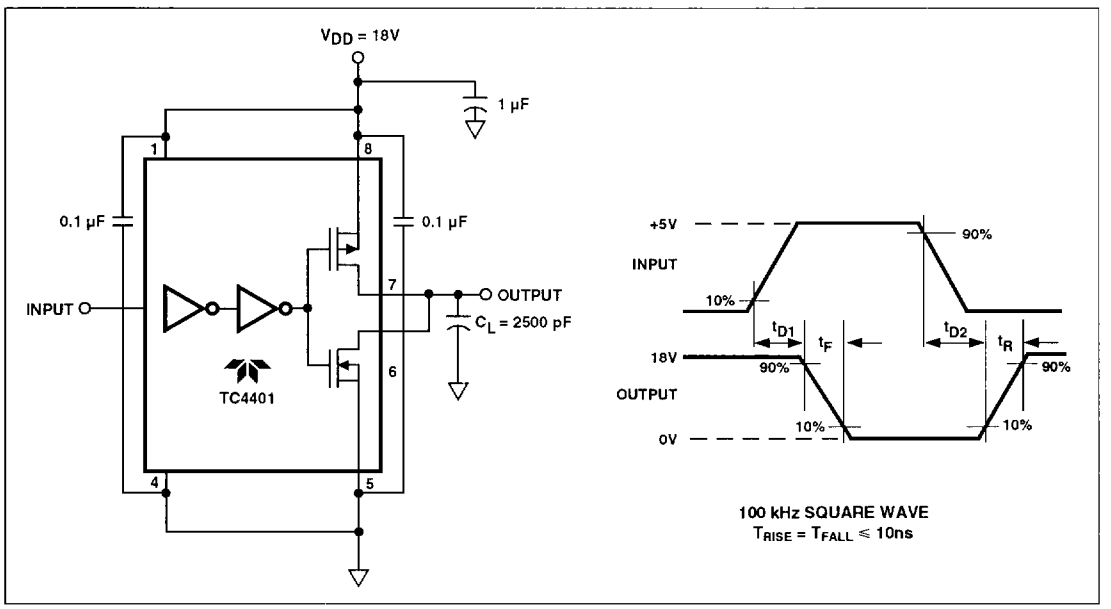
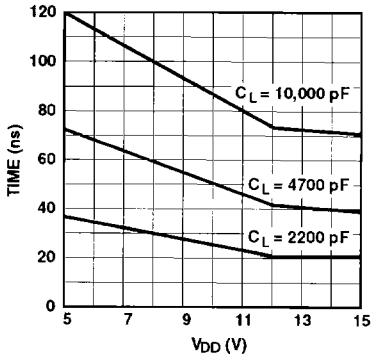


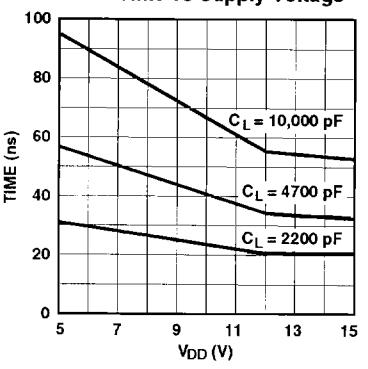
Figure 1. Switching Time Test Circuit

TYPICAL CHARACTERISTICS CURVES

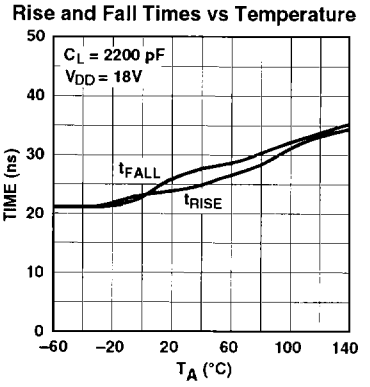
Rise Time vs Supply Voltage



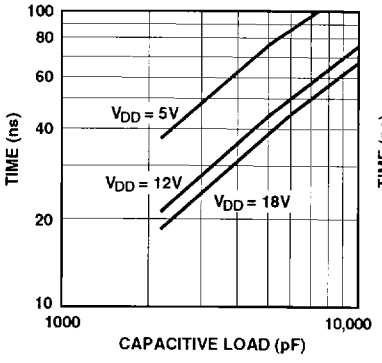
Fall Time vs Supply Voltage



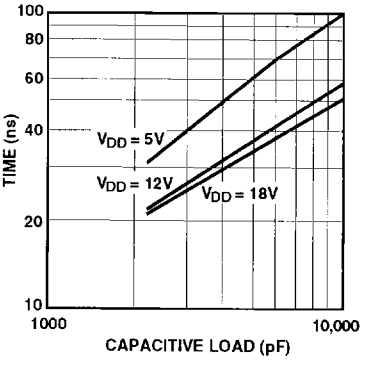
Rise and Fall Times vs Temperature



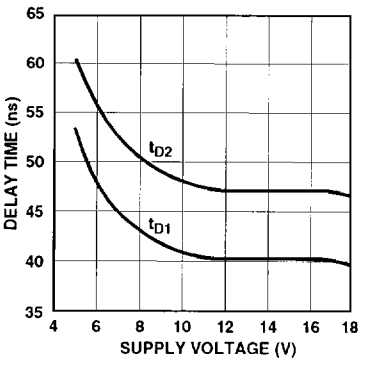
Rise Time vs Capacitive Load



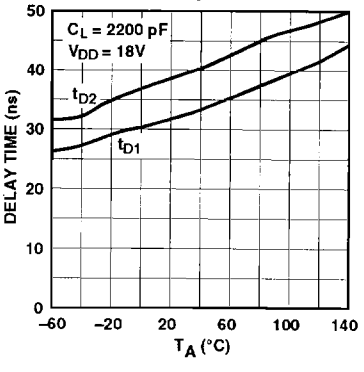
Fall Time vs Capacitive Load



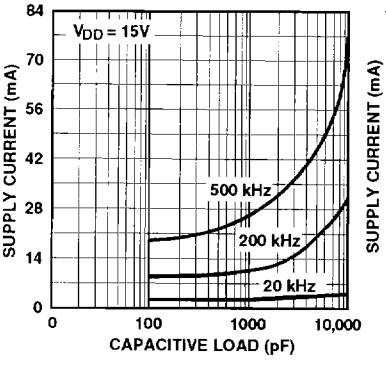
Propagation Delay Time vs Supply Voltage



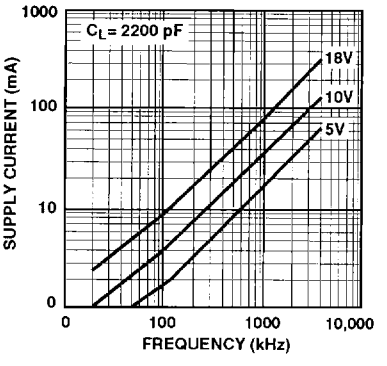
Propagation Delay Time vs Temperature



Supply Current vs Capacitive Load



Supply Current vs Frequency



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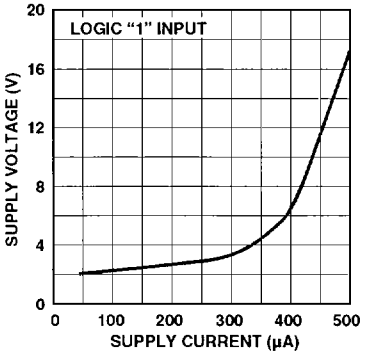
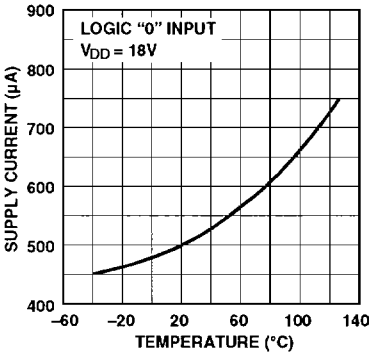
TYPICAL CHARACTERISTICS CURVES (Cont.)

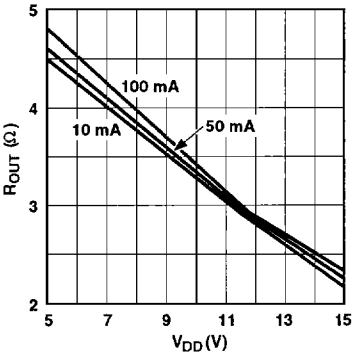
Quiescent Power Supply Current vs Supply Voltage



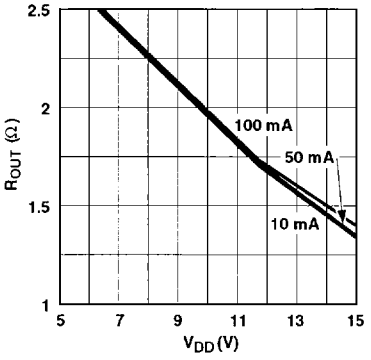
Quiescent Power Supply Current vs Temperature



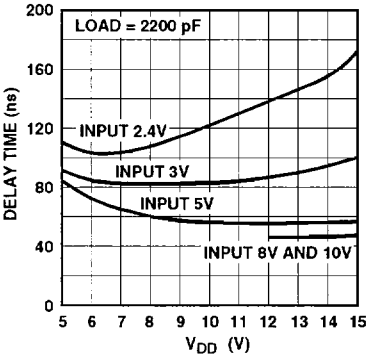
High-State Output Resistance



Low-State Output Resistance



Effect of Input Amplitude on Propagation Delay



POWER-ON OSCILLATION

It is extremely important that all MOSFET DRIVER applications be evaluated for the possibility of having HIGH-POWER OSCILLATIONS occurring during the POWER-ON cycle.

POWER-ON OSCILLATIONS are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit POWER-ON OSCILLATION problems is to place approximately 10 kΩ in series with the input of the MOSFET driver.

TYPICAL APPLICATIONS