# 512Kx32 SRAM MODULE *PRELIMINARY**

## FEATURES

- Access Times of 17, 20, 25, 35, 45, 55nS
- Packaging
  - 66 pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402), SMD Number 5962-94611 (Pending)
  - 68 lead, 40mm Hermetic CQFP, 5.1mm (0.200") (Package 501) SMD Number 5962-95624 (Pending)
  - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") Package Under Development (Package 502)
  - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3)
- Organized as 512Kx32, User Configurable as 1024Kx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32-XHX - 13 grams typical
  WS512K32-XG4X - 20 grams typical

* *This data sheet describes a product under development and is subject to change, without notice.*



## FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH2X, SMD 5962-94611 (Pending)

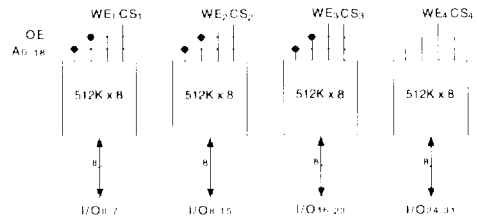
### TOP VIEW

| 1 | 12 | 23 | 34 | 45 | 56 |
|---|---|---|---|---|---|
| I/O0 | WE2 | I/O15 | I/O24 | VCC | I/O31 |
| I/O8 | CS2 | I/O14 | I/O25 | CS4 | I/O30 |
| I/O13 | GND | I/O13 | I/O26 | WE4 | I/O29 |
| A13 | I/O11 | I/O12 | A6 | I/O27 | I/O28 |
| A14 | A10 | OE | A7 | A1 | A0 |
| A15 | A11 | A18 | NC | A4 | A3 |
| A16 | A12 | WE1 | A8 | A5 | A2 |
| A17 | VCC | I/O7 | A9 | WE3 | I/O23 |
| I/O9 | CS1 | I/O6 | I/O16 | CS3 | I/O22 |
| I/O1 | NC | I/O5 | I/O17 | GND | I/O21 |
| I/O2 | I/O3 | I/O4 | I/O18 | I/O19 | I/O20 |
| 11 | 22 | 33 | 44 | 55 | 66 |

### PIN DESCRIPTION

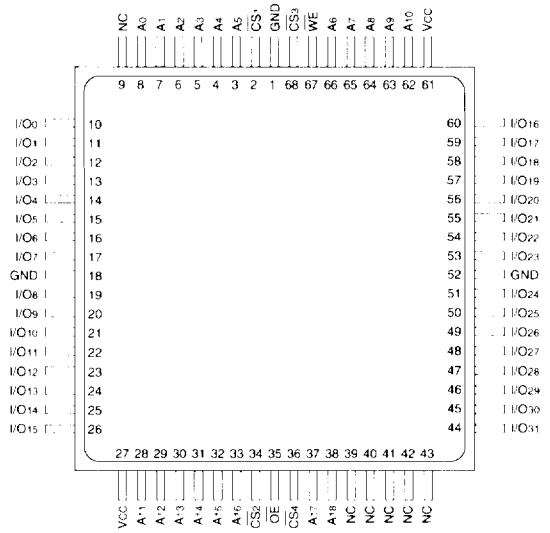
| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-18 | Address Inputs |
| $\overline{WE}_{1-4}$ | Write Enables |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| VCC | Power Supply |
| GND | Ground |
| NC | Not Connected |

### BLOCK DIAGRAM



## FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4X, SMD 5962-95624 (Pending)

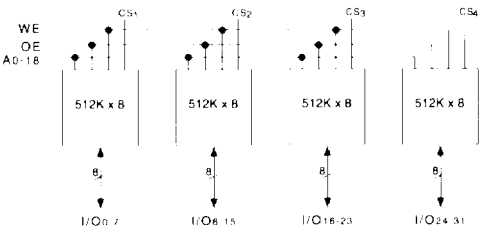
### TOP VIEW




### PIN DESCRIPTION

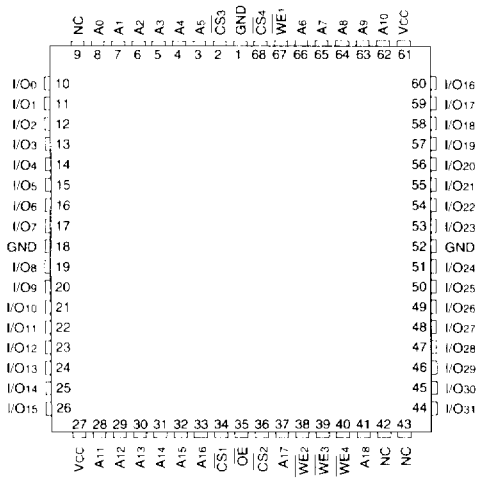
| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-18 | Address Inputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | Power Supply |
| GND | Ground |
| NC | Not Connected |

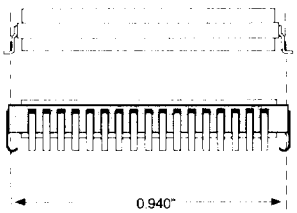
### BLOCK DIAGRAM




## FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2X

### TOP VIEW



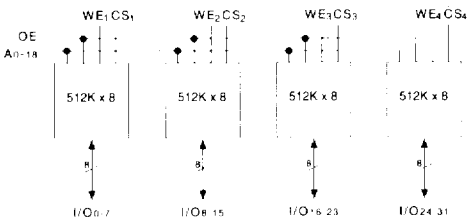




The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

### PIN DESCRIPTION

| | |
|---|---|
| I/O0-31 | Data Inputs/Outputs |
| A0-18 | Address Inputs |
| $\overline{WE}_{1-4}$ | Write Enables |
| $\overline{CS}_{1-4}$ | Chip Selects |
| $\overline{OE}$ | Output Enable |
| $V_{CC}$ | Power Supply |
| GND | Ground |

### BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Operating Temperature | $T_A$ | -55 | +125 | °C |
| Storage Temperature | $T_{STG}$ | -65 | +150 | °C |
| Signal Voltage Relative to GND | $V_G$ | -0.5 | $V_{CC}$+0.5 | V |
| Junction Temperature | $T_J$ | | 150 | °C |
| Supply Voltage | $V_{CC}$ | -0.5 | 7.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.5 | V |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}$ + 0.3 | V |
| Input Low Voltage | $V_{IL}$ | -0.5 | +0.8 | V |
| Operating Temp (Mil) | $T_A$ | -55 | +125 | °C |

## TRUTH TABLE

| $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Mode | Data I/O | Power |
|---|---|---|---|---|---|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | H | H | Out Disable | High Z | Active |
| L | X | L | Write | Data In | Active |

## CAPACITANCE

($T_A$ = +25°C)

| Parameter | Symbol | Conditions | Max | Unit |
|---|---|---|---|---|
| $\overline{OE}$ capacitance | $C_{OE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 50 | pF |
| $\overline{WE}_{1-4}$ capacitance HIP (PGA) | $C_{WE}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 20 | pF |
| CQFP G4 | | | 50 | |
| CQFP G2 | | | 20 | |
| $\overline{CS}_{1-4}$ capacitance | $C_{CS}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 20 | pF |
| Data I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V, f = 1.0 MHz | 20 | pF |
| Address input capacitance | $C_{AD}$ | $V_{IN}$ = 0 V, f = 1.0 MHz | 50 | pF |

This parameter is guaranteed by design but not tested.

## DC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter | Symbol | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = 5.5, $V_{IN}$ = GND to $V_{CC}$ | | 10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | | 10 | µA |
| Operating Supply Current x 32 Mode | $I_{CC \times 32}$ | $\overline{CS}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 400 | mA |
| Standby Current | $I_{SB}$ | $\overline{CS}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, f = 5MHz, $V_{CC}$ = 5.5 | | 40 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8mA, $V_{CC}$ = 4.5 | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4.0mA, $V_{CC}$ = 4.5 | 2.4 | | V |

NOTE: DC test conditions: $V_{IH}$ = $V_{CC}$ -0.3V, $V_{IL}$ = 0.3V

## DATA RETENTION CHARACTERISTICS

($T_A$ = -55°C to +125°C)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Data Retention Supply Voltage | $V_{DR}$ | $\overline{CS}$ ≥ $V_{CC}$ -0.2V | 2.0 | | 5.5 | V |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3V | | 2.0 | 8.0* | mA |

* Also available in Low Power version, please call factory for information.

## AC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter<br>Read Cycle | Symbol | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | nS |
| Address Access Time | $t_{AA}$ | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | nS |
| Output Hold from Address Change | $t_{OH}$ | 4 | | 4 | | 5 | | 5 | | 5 | | 5 | | nS |
| Chip Select Access Time | $t_{ACS}$ | | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | nS |
| Output Enable to Output Valid | $t_{OE}$ | | 9 | | 10 | | 12 | | 25 | | 35 | | 45 | nS |
| Chip Select to Output in Low Z | $t_{CLZ}$[1] | 3 | | 3 | | 3 | | 4 | | 4 | | 4 | | nS |
| Output Enable to Output in Low Z | $t_{OLZ}$[1] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Chip Disable to Output in High Z | $t_{CHZ}$[1] | | 8 | | 8 | | 10 | | 15 | | 15 | | 15 | nS |
| Output Disable to Output in High Z | $t_{OHZ}$[1] | | 8 | | 8 | | 10 | | 15 | | 15 | | 15 | nS |

1. This parameter is guaranteed by design but not tested.

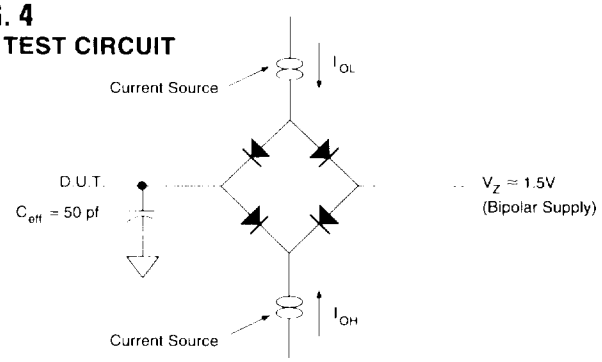
## AC CHARACTERISTICS

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_A$ = -55°C to +125°C)

| Parameter<br>Write Cycle | Symbol | -17 | | -20 | | -25 | | -35 | | -45 | | -55 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 17 | | 20 | | 25 | | 35 | | 45 | | 55 | | nS |
| Chip Select to End of Write | $t_{CW}$ | 13 | | 13 | | 15 | | 25 | | 35 | | 45 | | nS |
| Address Valid to End of Write | $t_{AW}$ | 13 | | 13 | | 15 | | 25 | | 35 | | 45 | | nS |
| Data Valid to End of Write | $t_{DW}$ | 9 | | 10 | | 11 | | 20 | | 30 | | 40 | | nS |
| Write Pulse Width | $t_{WP}$ | 13 | | 13 | | 15 | | 25 | | 35 | | 45 | | nS |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Address Hold Time | $t_{AH}$ | 0 | | 1 | | 2 | | 2 | | 2 | | 2 | | nS |
| Output Active from End of Write | $t_{OW}$[1] | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | nS |
| Write Enable to Output in High Z | $t_{WHZ}$[1] | | 8 | | 11 | | 13 | | 15 | | 15 | | 15 | nS |
| Data Hold Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | nS |

1. This parameter is guaranteed by design but not tested.

## FIG. 4
## AC TEST CIRCUIT

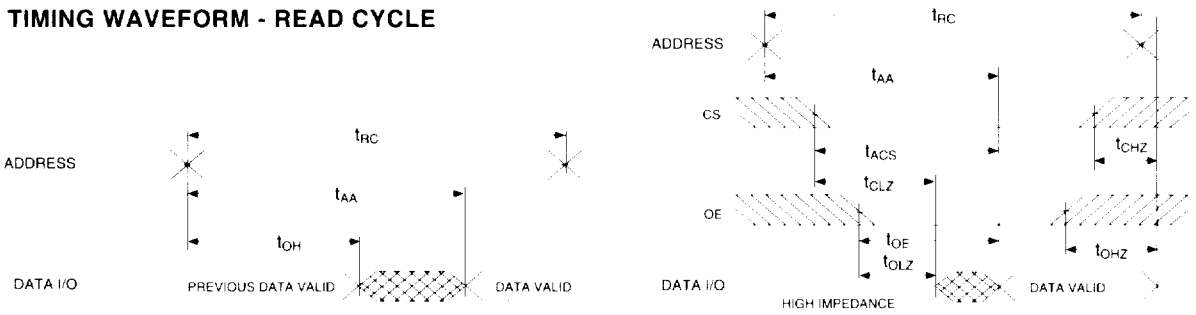



## AC TEST CONDITIONS

| Parameter | Typ | Unit |
|---|---|---|
| Input Pulse Levels | $V_{IL}$ = 0, $V_{IH}$ = 3.0 | V |
| Input Rise and Fall | 5 | nS |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

**NOTES:**
$V_Z$ is programmable from -2V to +7V.
$I_{OL}$ & $I_{OH}$ programmable from 0 to 16mA.
Tester Impedance $Z_0$ = 75 Ω.
$V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ & $I_{OH}$ are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

## FIG. 5
### TIMING WAVEFORM - READ CYCLE

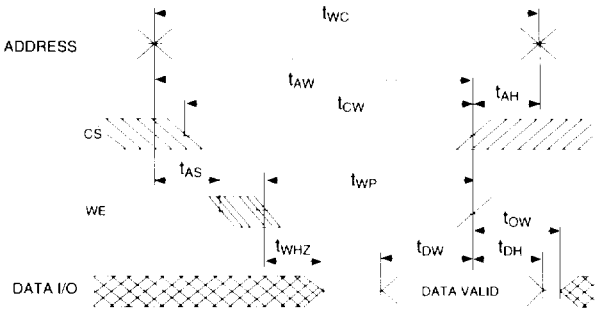



READ CYCLE 1 (CS = OE = $V_{IL}$, WE = $V_{IH}$)

READ CYCLE 2 (WE = $V_{IH}$)

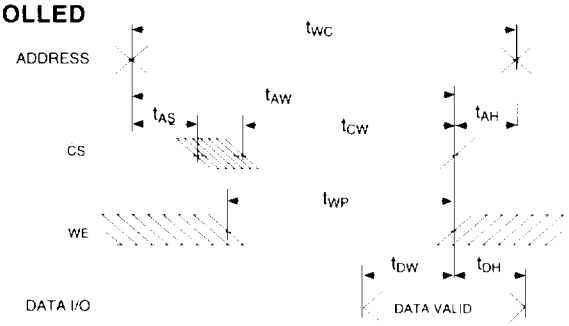
4 SRAM MODULES

## FIG. 6
### WRITE CYCLE - $\overline{WE}$ CONTROLLED



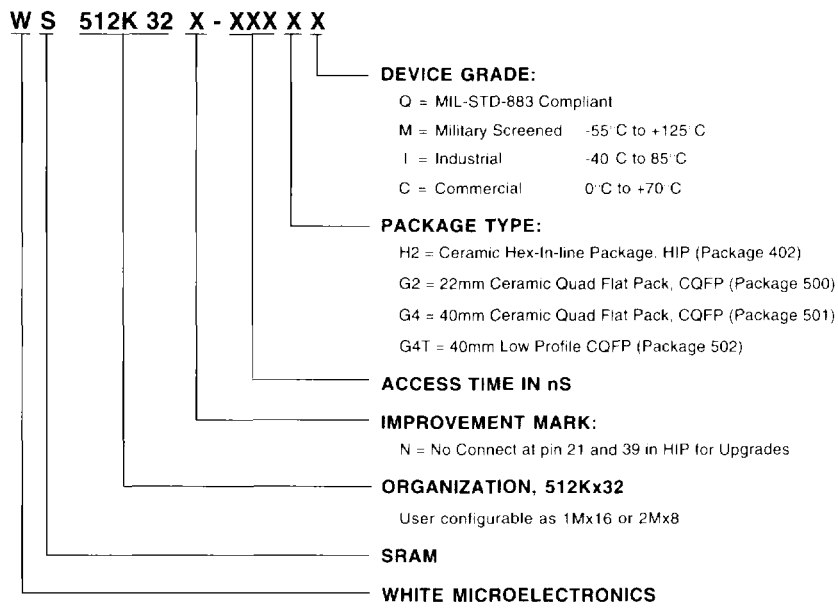

WRITE CYCLE 1, WE CONTROLLED (OE = $V_{IH}$)

## FIG. 7
### WRITE CYCLE - $\overline{CS}$ CONTROLLED




WRITE CYCLE 2, CS CONTROLLED (OE = $V_{IH}$)

## ORDERING INFORMATION




| Device Type | Speed | Package | SMD Number |
|---|---|---|---|
| 512K x 32 SRAM Module | 55nS | 66 pin HIP | 5962-94611 05HXX* |
| 512K x 32 SRAM Module | 45nS | 66 pin HIP | 5962-94611 06HXX* |
| 512K x 32 SRAM Module | 35nS | 66 pin HIP | 5962-94611 07HXX* |
| 512K x 32 SRAM Module | 25nS | 66 pin HIP | 5962-94611 08HXX* |
| 512K x 32 SRAM Module | 20nS | 66 pin HIP | 5962-94611 09HXX* |
| 512K x 32 SRAM Module | 17nS | 66 pin HIP | 5962-94611 10HXX* |
| 512K x 32 SRAM Module | 55nS | 68 pin CQFP | 5962-95624 05HXX* |
| 512K x 32 SRAM Module | 45nS | 68 pin CQFP | 5962-95624 06HXX* |
| 512K x 32 SRAM Module | 35nS | 68 pin CQFP | 5962-95624 07HXX* |
| 512K x 32 SRAM Module | 25nS | 68 pin CQFP | 5962-95624 08HXX* |
| 512K x 32 SRAM Module | 20nS | 68 pin CQFP | 5962-95624 09HXX* |
| 512K x 32 SRAM Module | 17nS | 68 pin CQFP | 5962-95624 10HXX* |

* Pending