

Features

256Kx4 bit CMOS Static

Random Access Memory

- Fast Access Times of 25, 35, 45 and 55ns
- \bar{E} and \bar{G} Functions for Bus Control
- 2V Data Retention Function (ED184256LPS)
- TTL Compatible I/O
- Common Data Inputs and Outputs
- Fully Static, No Clocks

Thru-hole and Surface Mount Package Options

- Ceramic DIP, 400 mils Wide, No. 101
- 28 Pad Ceramic LCC, No 76
- 28 Lead Ceramic SOJ, No. 77
- 32 Pad Ceramic LCC, No. 211

Single +5V ($\pm 10\%$) Supply Operation

256Kx4 Monolithic CMOS Static RAM, High Speed

The ED184256CS is a high speed, high performance, megabit density monolithic Static RAM organized as 256Kx4 bits.

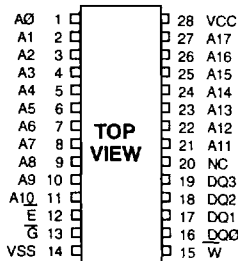
Inputs and outputs are TTL compatible and allow for direct interfacing with common system bus architecture.

A low power version, ED184256LPS, includes a 2V Data Retention Function for battery back-up operation.

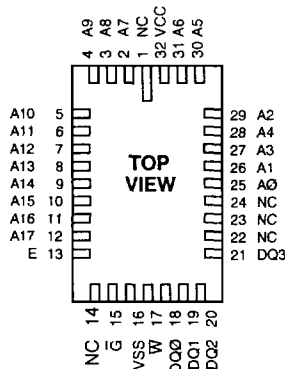
Military product is compliant to Appendix A of MIL-PRF-38535.

2

Pin Configurations and Block Diagram



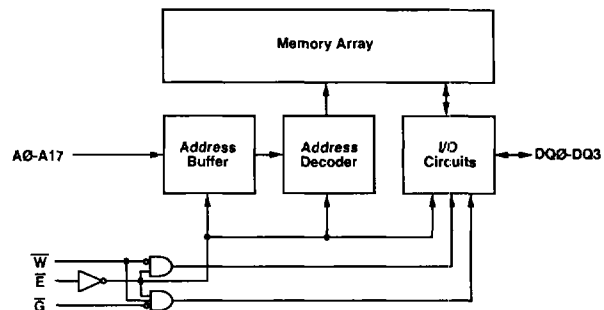
28 Pin DIP
28 pad LCC
28 Lead CSOJ



32 pad LCC

Pin Names

| | |
|-----------|--------------------------|
| A0-A17 | Address Inputs |
| \bar{E} | Chip Enable |
| \bar{W} | Write Enable |
| \bar{G} | Output Enable |
| DQ0-DQ3 | Common Data Input/Output |
| VCC | Power (+5V $\pm 10\%$) |
| VSS | Ground |
| NC | No Connection |



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Absolute Maximum Ratings*

| | |
|------------------------------------|-----------------|
| Voltage on any pin relative to VSS | -0.5V to 7.0V |
| Operating Temperature TA (Ambient) | |
| Military | -55°C to +125°C |
| Industrial | -40°C to +85°C |
| Storage Temperature | |
| Ceramic | -65°C to +150°C |
| Power Dissipation | 1 Watt |
| Output Current | 40 mA |
| Junction Temperature, TJ | 175°C |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

| Parameter | Sym | Min | Typ | Max | Units |
|--------------------|-----|------|-----|---------|-------|
| Supply Voltage | VCC | 4.5 | 5.0 | 5.5 | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | VCC+0.5 | V |
| Input Low Voltage | VIL | -0.3 | -- | 0.8 | V |

AC Test Conditions

| | |
|--------------------------------|-------------|
| Input Pulse Levels | VSS to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | Figure 1 |

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF Figure 2)

Figure 1

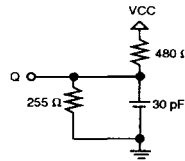
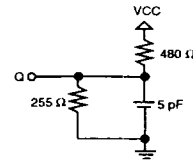


Figure 2



DC Electrical Characteristics

| Parameter | Sym | Conditions | Min | Typ* | Max | Units |
|------------------------------------|------|---|-----------|------|----------|----------|
| Operating Power Supply Current | ICC1 | $\bar{W}, \bar{E} = VIL, I/O = 0mA, \text{Min Cycle}$ | | | 180 | mA |
| Standby (TTL) Power Supply Current | ICC2 | $\bar{E} \geq VIH, VIL \geq VIN \geq VIH$ | | | 20 | mA |
| Full Standby Power Supply Current | ICC3 | $\bar{E} \geq VCC-0.2V$ $VIN \geq VCC-0.2V$ or $VIN \leq 0.2V$ | CS LPS | 1 | 5 2 | mA mA |
| Input Leakage Current | ILI | $VIN = 0V \text{ to } VCC$ | -- | -- | ± 5 | μA |
| Output Leakage Current | ILO | $V I/O = 0V \text{ to } VCC$ | -- | -- | ± 10 | μA |
| Output High Voltage | VOH | $I/OH = -4.0mA$ | 2.4 | | | V |
| Output Low Voltage | VOL | $I/OH = 8.0mA$ | | | 0.4 | V |

*Typical: TA=25°C, VCC=5.0V

Truth Table

| \bar{G} | \bar{E} | \bar{W} | Mode | Output | Power |
|-----------|-----------|-----------|-----------------|--------|------------|
| X | H | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | Output Deselect | High Z | ICC1 |
| L | L | H | Read | DOUT | ICC1 |
| X | L | L | Write | DIN | ICC1 |

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|------------------------|------|-----|-----------|
| | | LCC | CSOJ, DIP |
| Input (Except DQ Pins) | CI | 6 | 12 pF |
| Control (DQ Pins) | CD/Q | 8 | 14 pF |

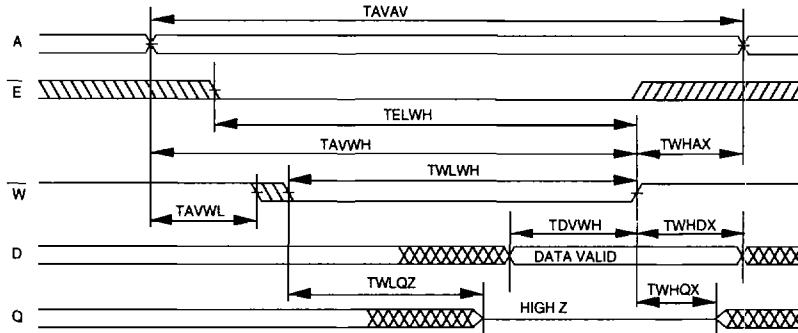
These parameters are sampled, not 100% tested.

AC Characteristics Write Cycle

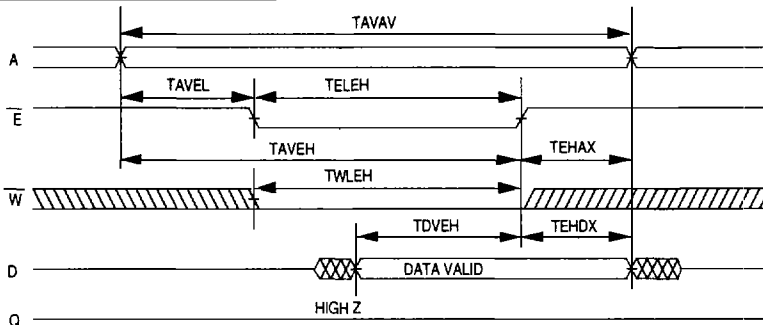
| Parameter | Symbol | | 25ns | | 35ns | | 45ns | | 55ns | | Units |
|-------------------------------------|--------|------|------|-----|------|-----|------|-----|------|-----|-------|
| | JEDEC | Alt. | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | TWC | 25 | | 35 | | 45 | | 55 | | ns |
| Chip Enable to End of Write | TELWH | TCW | 20 | | 30 | | 35 | | 40 | | ns |
| | TELEH | TCW | 20 | | 30 | | 35 | | 40 | | ns |
| Address Setup Time | TAVWL | TAS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| | TAVEL | TAS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| Address Valid to End of Write | TAVWH | TAW | 20 | | 30 | | 35 | | 40 | | ns |
| | TAVEH | TAW | 20 | | 30 | | 35 | | 40 | | ns |
| Write Pulse Width | TWLWH | TWP | 20 | | 30 | | 35 | | 40 | | ns |
| | TWLEH | TWP | 20 | | 30 | | 35 | | 40 | | ns |
| Write Recovery Time | TWHAX | TWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| | TEHAX | TWR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| Data Hold Time | TWHDX | TDH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| | TEHDX | TDH | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ns |
| Write to Output in High Z (1) | TWLQZ | TWHZ | 0 | 10 | 0 | 15 | 0 | 20 | 0 | 20 | ns |
| Data to Write Time | TDVWH | TDW | 15 | | 20 | | 25 | | 25 | | ns |
| | TDVEH | TDW | 15 | | 20 | | 25 | | 25 | | ns |
| Output Active from End of Write (1) | TWHQX | TWLZ | 3 | | 3 | | 3 | | 3 | | ns |

Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - W Controlled



Write Cycle 2 - E Controlled

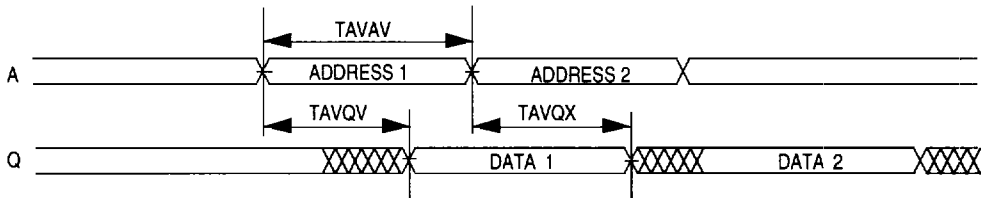


AC Characteristics Read Cycle

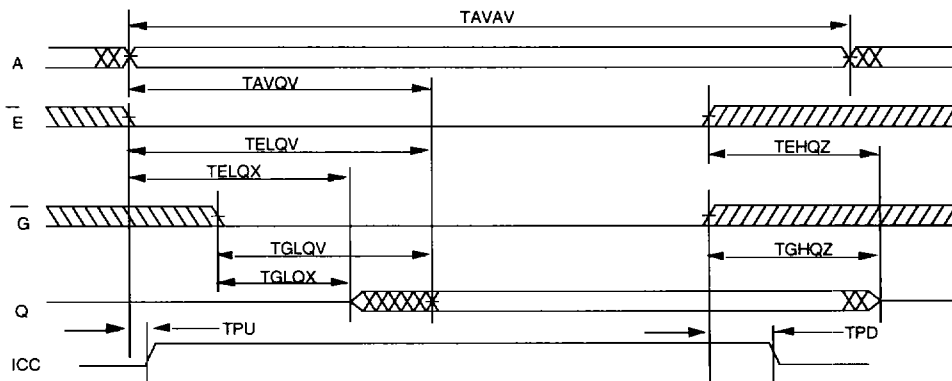
| Parameter | Symbol | 25ns | | 35ns | | 45ns | | 55ns | | Units |
|--|-------------|------|-----|------|-----|------|-----|------|-----|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV TRC | 25 | | 35 | | 45 | | 55 | | ns |
| Address Access Time | TAVQV TAA | | 25 | | 35 | | 45 | | 55 | ns |
| Chip Enable Access Time | TELQV TACS | | 25 | | 35 | | 45 | | 55 | ns |
| Chip Enable to Output in Low Z (1) | TELQX TCLZ | 3 | | 3 | | 3 | | 3 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ TCHZ | | 12 | | 20 | | 25 | | 25 | ns |
| Output Hold from Address Change | TAVQX TOH | 3 | | 3 | | 3 | | 3 | | ns |
| Output Enable to Output Valid | TGLQV TOE | | 10 | | 20 | | 25 | | 25 | ns |
| Output Enable to Output in Low Z (1) | TGLQX TOLZ | 0 | | 0 | | 0 | | 0 | | ns |
| Output Disable to Output in High Z (1) | TGHQZ TOHZ | | 10 | | 20 | | 25 | | 25 | ns |
| Chip Enable to Power Up | TELICCH TPU | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Enable to Power Down | TEHICCL TPD | | 25 | | 35 | | 45 | | 55 | ns |

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - W High, G, E Low



Read Cycle 2 - W High



2

Data Retention Characteristics

Low Power (LPS) Version Only

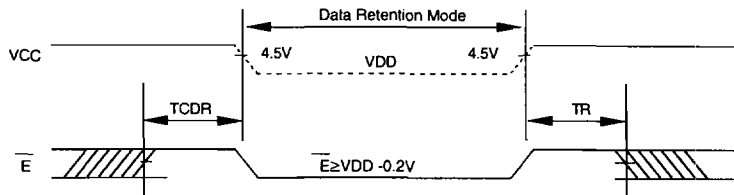
(TA = -55°C to +125°C)

| Characteristic | Sym | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------------|-------|---------------------------|--------|-----|-----|---------|
| Data Retention Voltage | VDD | VDD = 2.0V | 2 | -- | -- | V |
| Data Retention Quiescent Current | ICCDR | $\bar{E} \geq VDD - 0.2V$ | -- | 500 | 750 | μA |
| Chip Disable to Data Retention Time | TCDR | VIN \geq VDD - 0.2V | 0 | -- | -- | ns |
| Operation Recovery Time | TR | or VIN \leq 0.2V | TAVAV* | | -- | ns |

Note 1: Parameter guaranteed, but not tested.

*Read Cycle Time

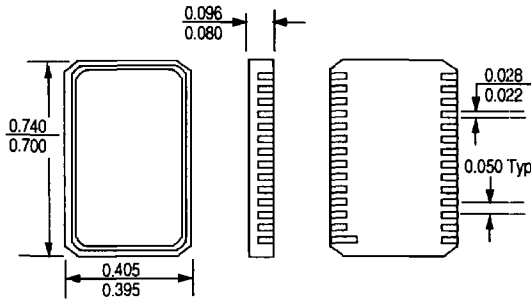
Data Retention E Controlled



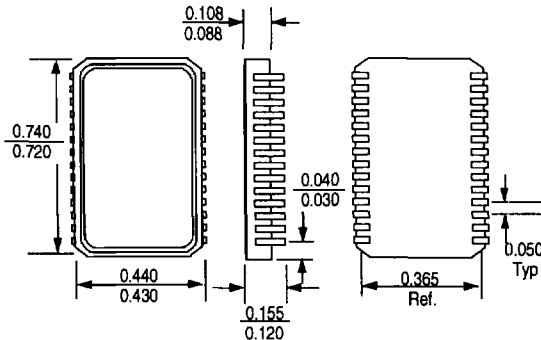
Package Description

Package Descriptions

Package No. 76
28 Pad LCC

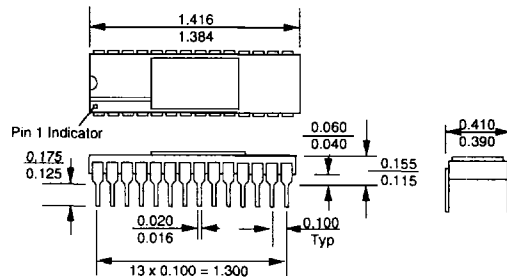


Package No. 77
28 Pin Ceramic SOJ
J-Leaded Package

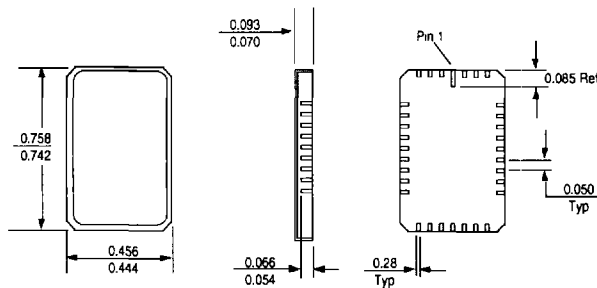


Package Description

Package No. 101
28 Pin Sidebrazed Ceramic
Dual-in-line Package
400 mils wide



Package No. 211
32 pad LCC



Ordering Information

| Part No. | Speed | Package |
|------------------|-------|---------|
| Standard Power | ns | No. |
| EDI84256CS25LB | 25 | 76 |
| EDI84256CS35LB | 35 | 76 |
| EDI84256CS45LB | 45 | 76 |
| EDI84256CS55LB | 55 | 76 |
| EDI84256CS25L32B | 25 | 211 |
| EDI84256CS35L32B | 35 | 211 |
| EDI84256CS45L32B | 45 | 211 |
| EDI84256CS55L32B | 55 | 211 |
| EDI84256CS25NB | 25 | 77 |
| EDI84256CS35NB | 35 | 77 |
| EDI84256CS45NB | 45 | 77 |
| EDI84256CS55NB | 55 | 77 |
| EDI84256CS25TB | 25 | 101 |
| EDI84256CS35TB | 35 | 101 |
| EDI84256CS45TB | 45 | 101 |
| EDI84256CS55TB | 55 | 101 |

| Low Power | Speed | Package |
|---------------------|-------|---------|
| with Data Retention | ns | No |
| EDI84256LPS25LB | 25 | 76 |
| EDI84256LPS35LB | 35 | 76 |
| EDI84256LPS45LB | 45 | 76 |
| EDI84256LPS55LB | 55 | 76 |
| EDI84256LPS25L32B | 25 | 211 |
| EDI84256LPS35L32B | 35 | 211 |
| EDI84256LPS45L32B | 45 | 211 |
| EDI84256LPS55L32B | 55 | 211 |
| EDI84256LPS25NB | 25 | 77 |
| EDI84256LPS35NB | 35 | 77 |
| EDI84256LPS45NB | 45 | 77 |
| EDI84256LPS55NB | 55 | 77 |
| EDI84256LPS25TB | 25 | 101 |
| EDI84256LPS35TB | 35 | 101 |
| EDI84256LPS45TB | 45 | 101 |
| EDI84256LPS55TB | 55 | 101 |

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