



CAT24FC01, CAT24FC02

1-kb/2-kb I²C Serial EEPROM

FEATURES

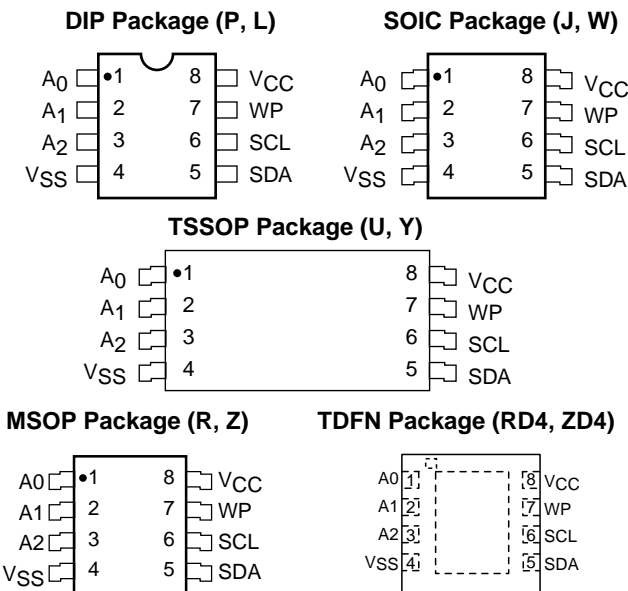
- 400 kHz (2.5 V) and 100 kHz (1.7 V) I²C bus compatible
- 1.7 to 5.5 volt operation
- Low power CMOS technology
 - zero standby current
- 16-byte page write buffer
- Industrial and extended temperature ranges
- Self-timed write cycle with auto-clear
- 1,000,000 program/erase cycles
- 100 year data retention
- 8-pin DIP, 8-pin SOIC, 8-pin TSSOP and TDFN packages
 - “Green” package option available
- 256 x 8 memory organization
- Hardware write protect

DESCRIPTION

The CAT24FC01/2 is a 1-kb/2-kb Serial CMOS EEPROM internally organized as 128/256 words of 8 bits each. Catalyst’s advanced CMOS technology substantially reduces device power requirements.

The CAT24FC01/2 features a 16-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP, 8-pin SOIC, 8-pin TSSOP and TDFN packages.

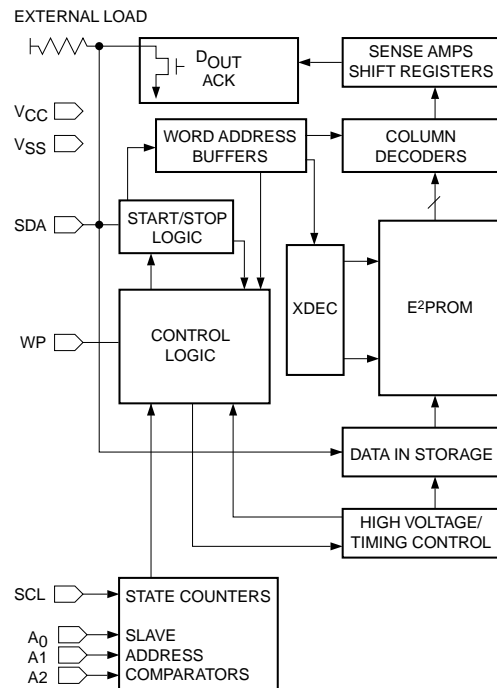
PIN CONFIGURATION



PIN FUNCTIONS

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V _{CC}	1.7 V to 5.5 V Power Supply
V _{SS}	Ground

BLOCK DIAGRAM



* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground ⁽¹⁾	-2.0 V to V _{CC} + 2.0 V
V _{CC} with Respect to Ground	-2.0 V to +7.0 V
Package Power Dissipation Capability (T _A = 25°C)	1.0 W

Lead Soldering Temperature (10 seconds) 300°C
 Output Short Circuit Current⁽²⁾ 100 mA

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Typ	Max	Units
N _{END} ⁽³⁾	Endurance	MIL-STD-883, Test Method 1033	1,000,000			Cycles/Byte
T _{DR} ⁽³⁾	Data Retention	MIL-STD-883, Test Method 1008	100			Years
V _{ZAP} ⁽³⁾	ESD Susceptibility	MIL-STD-883, Test Method 3015	4000			Volts
I _{LTH} ⁽³⁾⁽⁴⁾	Latch-up	JEDEC Standard 17	100			mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.7 V to 5.5 V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I _{CC}	Power Supply Current (Read)	f _{SCL} = 100 kHz		1		mA
I _{CC}	Power Supply Current (Write)	f _{SCL} = 100 kHz		3		mA
I _{SB} ⁽⁵⁾	Standby Current (V _{CC} = 5.0 V)	V _{IN} = GND or V _{CC}		0		μA
I _{LI}	Input Leakage Current	V _{IN} = GND to V _{CC}		1		μA
I _{LO}	Output Leakage Current	V _{OUT} = GND to V _{CC}		1		μA
V _{IL}	Input Low Voltage		-1		V _{CC} x 0.3	V
V _{IH}	Input High Voltage		V _{CC} x 0.7		V _{CC} + 1.0	V
V _{OL1}	Output Low Voltage (V _{CC} = 3.0 V)	I _{OL} = 3 mA		0.4		V
V _{OL2}	Output Low Voltage (V _{CC} = 1.7 V)	I _{OL} = 1.5 mA		0.5		V

CAPACITANCE T_A = 25°C, f = 400 kHz, V_{CC} = 5 V

Symbol	Test	Conditions	Min	Typ	Max	Units
C _{I/O} ⁽³⁾	Input/Output Capacitance (SDA)	V _{I/O} = 0 V			8	pF
C _{IN} ⁽³⁾	Input Capacitance (other pins)	V _{IN} = 0 V			6	pF

Note:

- (1) The minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1.0 V to V_{CC} + 1.0 V.
- (5) Standby Current, I_{SB} = 0 μA (<900 nA).

A.C. CHARACTERISTICS

$V_{CC} = 1.7\text{ V}$ to 5.5 V , unless otherwise specified.

Read & Write Cycle Limits

Symbol	Parameter	1.7 V - 5.5 V		2.5 V - 5.5 V		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$T_I^{(1)}$	Noise Suppression Time Constant at SCL, SDA Inputs		100		100	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out		3.5		0.9	μs
$t_{BUF}^{(1)}$	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.3		μs
$t_{HD:STA}$	Start Condition Hold Time	4		0.6		μs
t_{LOW}	Clock Low Period	4.7		1.3		μs
t_{HIGH}	Clock High Period	4		0.6		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		ns
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
$t_R^{(1)}$	SDA and SCL Rise Time		1		0.3	μs
$t_F^{(1)}$	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4		0.6		μs
t_{DH}	Data Out Hold Time	100		100		ns

Power-Up Timing⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

Write Cycle Limits

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			5	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus

interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

FUNCTIONAL DESCRIPTION

The CAT24FC01/2 supports the I²C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. Data transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24FC01/2 operates as a Slave device. Both the Master and Slave devices can operate as either transmitter or receiver, but the Master device controls which mode is activated. A maximum of 8 devices may be connected to the bus as determined by the device address inputs A0, A1, and A2.

all data transfers into or out of the device. This is an input pin.

SDA: Serial Data/Address

The CAT24FC01/2 bidirectional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

A0, A1, A2: Device Address Inputs

These inputs set device address when cascading multiple devices. A maximum of eight devices can be cascaded when using the device.

WP: Write Protect

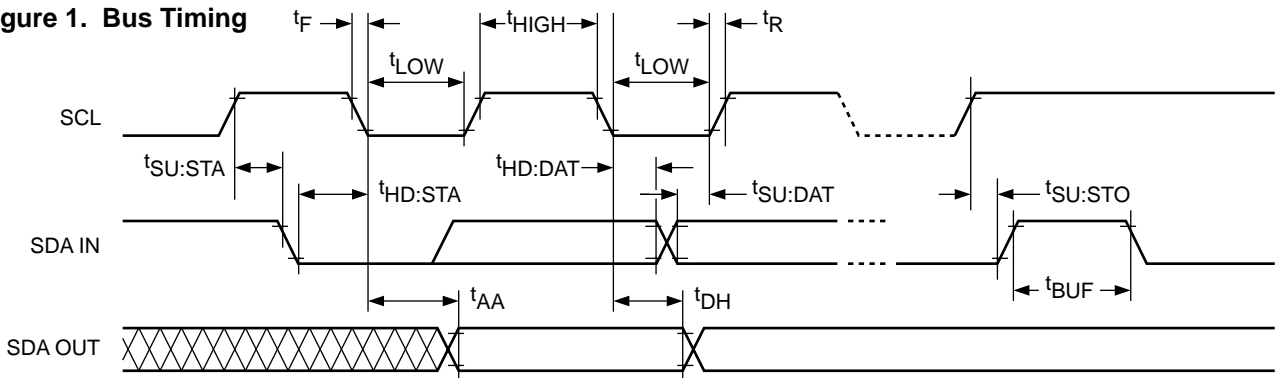
This input, when tied to GND, allows write operations to the entire memory. For CAT24FC01/2 when this pin is tied to V_{CC}, the entire array of memory is write protected. When left floating, memory is unprotected.

PIN DESCRIPTIONS

SCL: Serial Clock

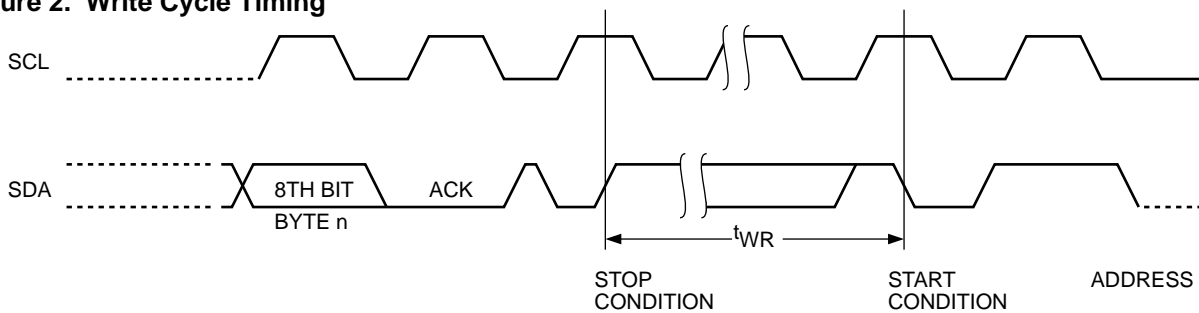
The CAT24FC01/2 serial clock input pin is used to clock

Figure 1. Bus Timing



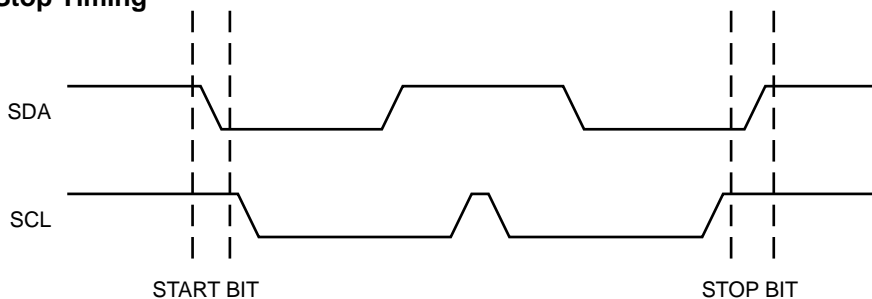
5020 FHD F03

Figure 2. Write Cycle Timing



5020 FHD F04

Figure 3. Start/Stop Timing



5020 FHD F05

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/W bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24FC01/2. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24FC01/2 acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24FC01/2 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to 15 additional bytes. After each byte has been transmitted the CAT24FC01/2 will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 16 bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all 16 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24FC01/2 in a single write cycle.

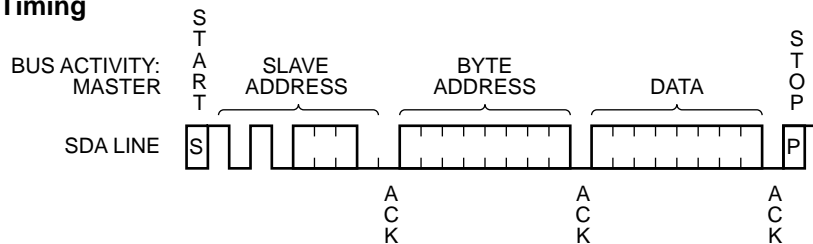
Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24FC01/2 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24FC01/2 is still busy with the write operation, no ACK will be returned. If the CAT24FC01/2 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

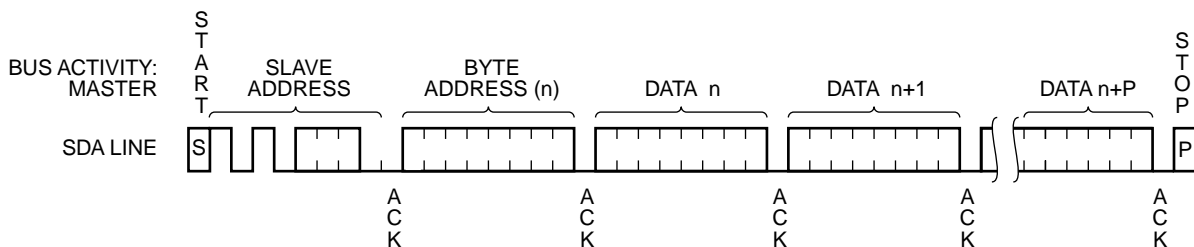
The CAT24FC01/2 is designed with a hardware protect pin that enables the user to protect the entire memory. The hardware protection feature of the CAT24FC01/2 is designed into the part to provide added flexibility to the design engineers. The write protection feature of CAT24FC01/2 allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to Vcc, the entire memory array is protected and becomes read only. The entire memory becomes write protected regardless of whether the write protect register has been written or not. When WP pin is tied to Vcc, the user cannot program the write protect register. If the WP pin is left floating or tied to Vss, the device can be written into.

Figure 6. Byte Write Timing



5020 FHD F08

Figure 7. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

5020 FHD F09

Read Operations

The READ operation for the CAT24FC01/2 is initiated in the same manner as the write operation with the one exception that the R/\overline{W} bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24FC01/2's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N + 1. If N = 255 for 24FC02, then the counter will 'wrap around' to address 0 and continue to clock out data. If N = 127 for the CAT24FC01, the counter will not wrap around. After the CAT24FC02 receives its slave address information (with the R/\overline{W} bit set to one), it issues an acknowledge, then transmits the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to

read. After the CAT24FC01/2 acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/\overline{W} bit set to one. The CAT24FC01/2 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24FC01/2 sends the initial 8-bit data requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24FC01/2 will continue to output a byte for each acknowledge sent by the Master. The operation will terminate operation when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24FC01/2 is outputted sequentially with data from address N followed by data from address N + 1. The READ operation address counter increments all of the CAT24FC01/2 address bits so that the entire memory array can be read during one operation. If more than the 256 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing

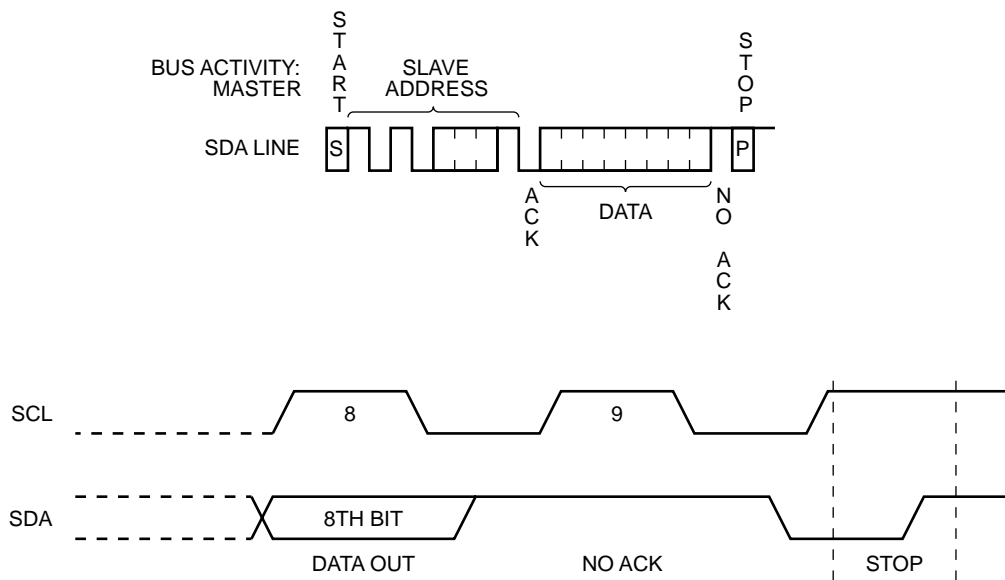


Figure 9. Selective Read Timing

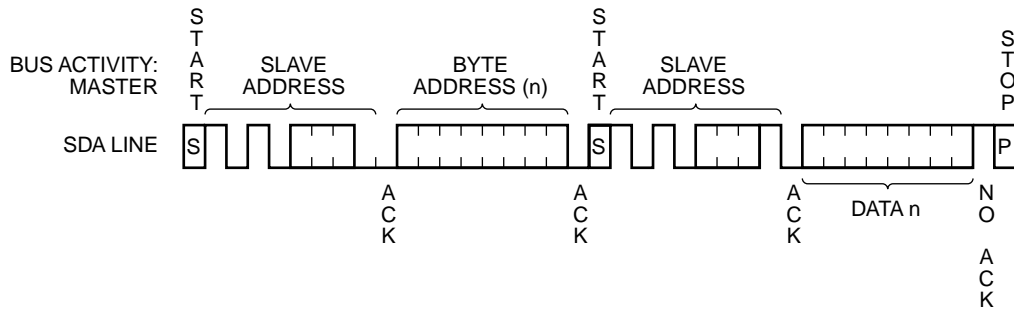
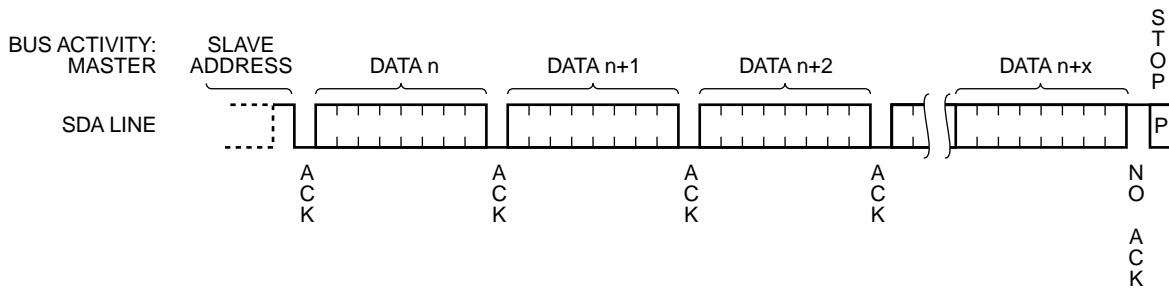
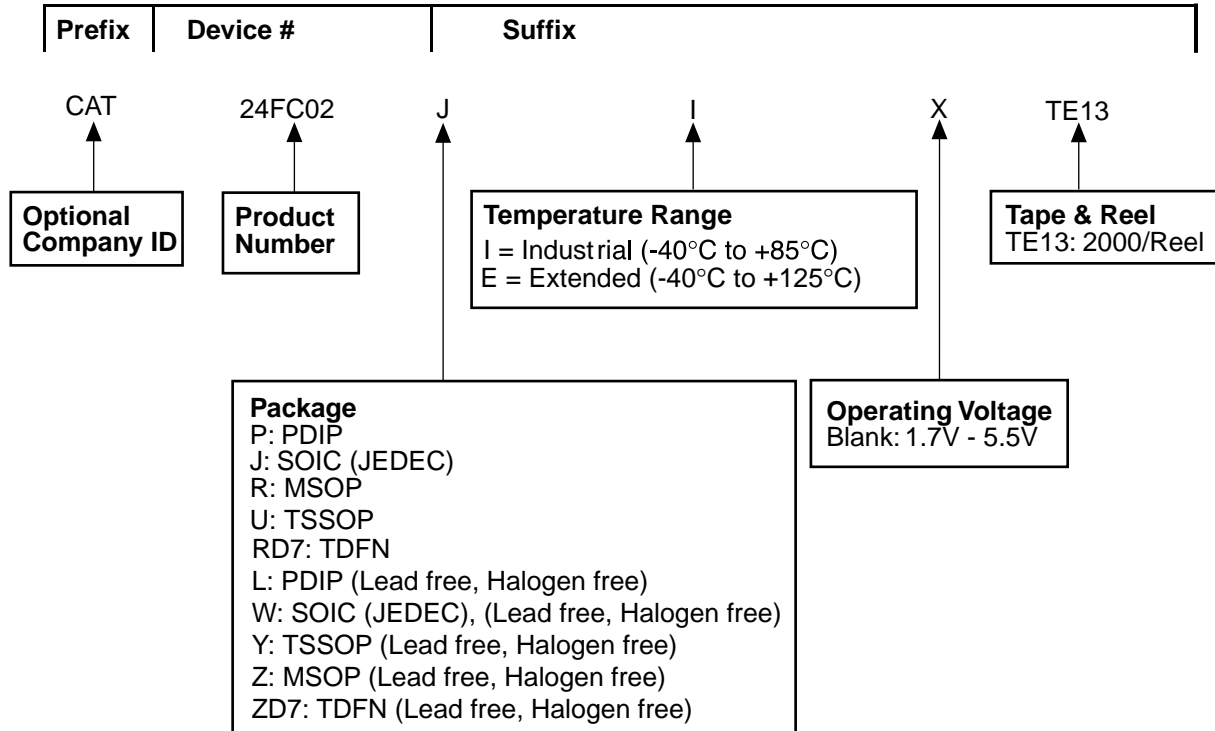


Figure 10. Sequential Read Timing



ORDERING INFORMATION



Notes:

(1) The device used in the above example is a 24FC02JI-TE13 (SOIC, Industrial Temperature, 1.7 Volt to 5.5 Volt Operating Voltage, Tape & Reel)

REVISION HISTORY

Date	Rev.	Reason
11/18/2003	A	Initial Issue
12/9/2003	B	Changed Industrial Temp to "I" from "Blank" in ordering information

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