HARRIS SEMICONDUCTOR

CD74FCT399T

December 1996

Fast CMOS Quad Dual-Port Register

Features

- **Advanced 0.8 micron CMOS Technology**
- **The CD74FCT399T is Pin Compatible With Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

These high-speed quad dual-port registers select 4-bit wide data from one of the two sources (Ports) under control of a common Select input (S). Synchronous with the LOW-to-HIGH transition of the Clock input (CP), the selected data is transferred to a 4-bit output register. The 4-bit D-type output register is fully edge-triggered. For predictable operation, the Data inputs (I_{AX}, I_{BX}) and Select input (S) must be stable one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input.

Ordering Information

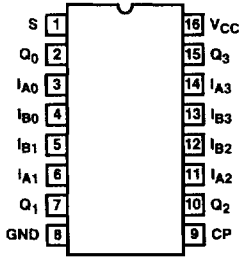
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT399ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT399CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT399TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT399ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT399CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT399TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT399ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT399CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT399TQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT399T
(SOIC, QSOP)
TOP VIEW

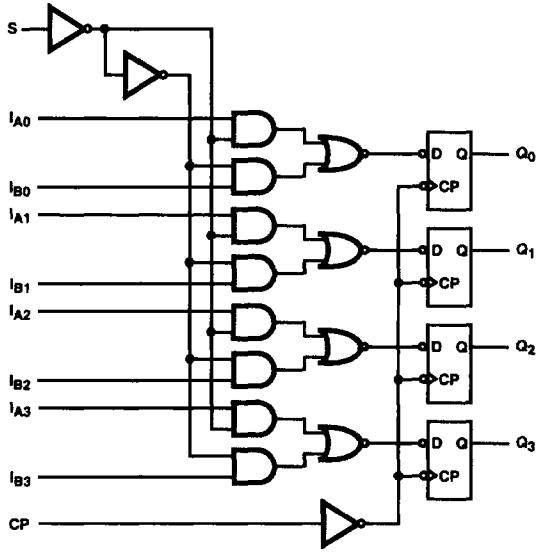


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4252**

Functional Block Diagram



TRUTH TABLE

INPUTS			OUTPUTS
S	I_A	I_B	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

NOTE:

1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock trasition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock trasition
   X = Don't Care

Pin Descriptions

PIN NAME	DESCRIPTION
S	Common Select Input
CP	Clock Pulse Input
I_{A0} - I_{A3}	Data Inputs from Source A
I_{B0} - I_{B3}	Data Inputs from Source B
Q_0 - Q_3	Register True Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package (M16.15-P)	110
SOIC Package (M16.3-P)	97
QSOP Package	140

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V 5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle S = GND, 50% Duty Cycle One Bit Toggling at f_i = 5MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle S = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	12.3 (Note 9)	mA

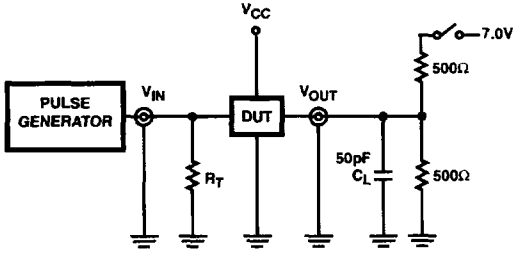
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
Propagation Delay CP to Q	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	3.0	10.0	2.5	7.0	2.5	5.6	ns
Setup Time, HIGH or LOW D to Q	t_{SU}		4.0	-	3.5	-	3.0	-	ns
Hold Time, HIGH or LOW D to Q	t_H		1.0	-	1.0	-	1.0	-	ns
Setup Time, HIGH or LOW S to CP	t_{SU}		9.0	-	8.5	-	3.0	-	ns
Hold Time, HIGH or LOW	t_H		0	-	0	-	0	-	ns
Clock Pulse Width (Note 13), HIGH or LOW	t_W		5.0	-	5.0	-	4.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_O
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuits and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

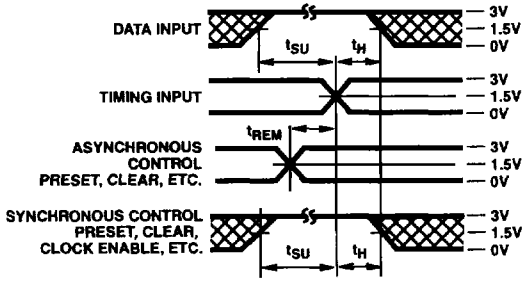


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

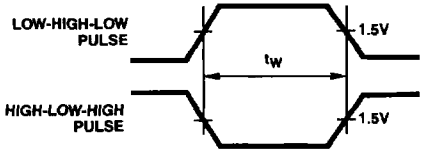


FIGURE 3. PULSE WIDTH

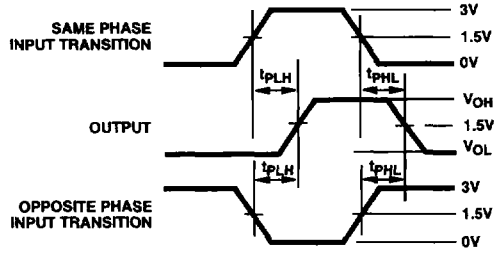


FIGURE 4. PROPAGATION DELAY