GD54/74HC259, GD54/74HCT259

8-BIT ADDRESSABLE LATCH/3-TO-8 LINE DECODER

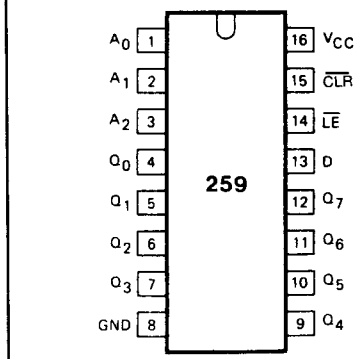
General Description

These devices are identical in pinout to the 54/74LS259. This 8-Bit Addressable latch can perform four basic functions in the addressable latch mode, data is read into the addressed stage of the latch. In the memory mode, the latch contents are storged regardless of any other inputs. in the 8-line decoder mode, data flows through to the addressed output. And in the clear mode, all stages are cleared to the low state. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Pin Configuration



Suffix-Blank : Plastic Dual In Line Package
Suffix-J : Ceramic Dual In Line Package
Suffix-D : Small Outline Package

Logic Diagram

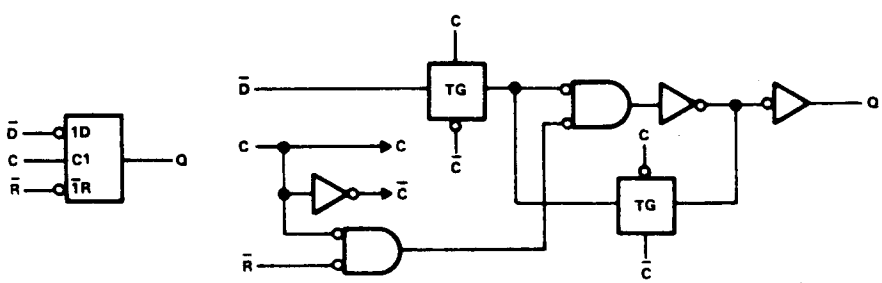


Fig. 1 Logic diagram (each latch)

Function Table

OPERATING MODES	INPUTS						OUTPUTS							
	$\overline{CLR}$	$\overline{LE}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
master clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
demultiplex (active HIGH) decoder (when D = H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q=d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q=d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q=d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q=d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
addressable latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	H	L	q_0	q_1	q_2	Q=d	q_4	q_5	q_6	q_7
	H	L	d	L	L	H	q_0	q_1	q_2	q_3	Q=d	q_5	q_6	q_7
	H	L	d	H	L	H	q_0	q_1	q_2	q_3	q_4	Q=d	q_6	q_7
	H	L	d	L	H	H	q_0	q_1	q_2	q_3	q_4	q_5	Q=d	q_7
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

H = HIGH voltage level
L = LOW voltage level
X = don't care
d = HIGH or LOW data one set-up time prior to the LOW-to-HIGI $\overline{LE}$ transition
q = lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared

Logic Diagram

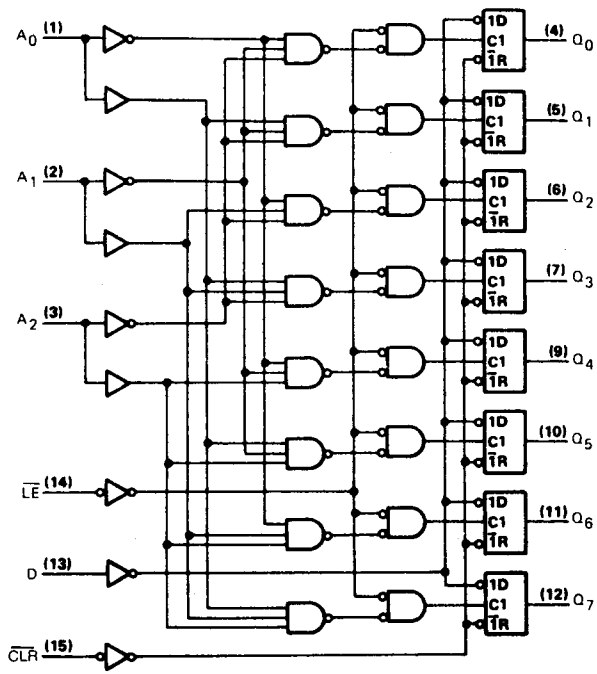


Fig. 2 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	DC Supply voltage		−0.5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for $V_I<-0.5$ or $V_I>V_{CC}+0.5V$		|20|	mA
I_O	DC output source or sink current	for $-0.5V<V_O<V_{CC}+0.5V$		|25|	mA
I_{CC}	DC V_{CC} or GND current			|50|	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C: derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in. from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		300 260	°C

Recommended Operating Conditions

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range V_{CC}: GD54/74HC Types	2	6	V
GD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A: GD74 Types	−40	+85	°C
GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f: GD54/74HC Types at 2V		1000	ns
at 4.5V		500	
at 6V		400	
GD54/74HCT Types at 4.5V		500	

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HC259		GD54HC259		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level input voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OH}=−20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			I_{OH}=−4mA I_{OH}=−5.2mA	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH} or V_{IL}	I_{OL}=20μA	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			I_{OL}=4mA I_{OL}=5.2mA	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC} or GND		6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC} (V)	T_A=25°C			GD74HCT259		GD54HCT259		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level input voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	V_{IN}=V_{IH}	I_{OH}=−20μA	4.5	4.4	4.5		4.4		4.4		V
		or V_{IL}	I_{OH}=−4mA	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	V_{IN}=V_{IH}	I_{OL}=20μA	4.5			0.1		0.1		0.1	V
		or V_{IL}	I_{OL}=4mA	4.5		0.17	0.26		0.33		0.4	
$\|I_{IN}\|$	Input leakage Current	V_{IN}=V_{CC}or GND		5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{out}=0μA		5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_W	Pulse width	$\overline{LE}$, $\overline{CLR}$ high or low	2.0	80	30		100		120		ns
			4.5	16	10		20		25		
			6.0	14	8		18		22		
t_{SU}	Setup time	Data after LE↓	2.0	60	30		100		120		ns
			4.5	12	10		20		25		
			6.0	10	8		18		22		
t_h	Hold time	Data before LE↓	2.0	3	0		3		3		ns
			4.5	3	0		3		3		
			6.0	3	0		3		3		

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT259		GD54HCT259		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH}/ t_{PHL}	Propagation Delay Time D to Qn	2.0		50	160		210		260	ns
		4.5		18	35		42		50	
		6.0		17	30		38		46	
t_{PLH}/ t_{PHL}	Propagation Delay Time An to Qn	2.0		50	160		210		260	ns
		4.5		18	35		42		50	
		6.0		17	30		38		46	
t_{PLH}/ t_{PHL}	Propagation Delay Time $\overline{LE}$ to Qn	2.0		48	150		200		250	ns
		4.5		17	33		40		48	
		6.0		16	28		36		42	
t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Qn	2.0		48	150		200		250	ns
		4.5		17	32		40		48	
		6.0		16	28		36		42	
t_{TLH}/ t_{THL}	Output Transition Time	2.0		25	70		85		100	ns
		4.5		8	15		18		22	
		6.0		7	13		16		19	

Timing Requirements for HCT : $t_r = t_f = 6ns$ $C_L = 50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A = 25°C$			GD74HCT259		GD54HCT259		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{LE}$, $\overline{CLR}$ high or low	4.5	16	10		20		25		ns
t_{su}	Setup time	Data after $\overline{LE}$ ↓	4.5	12	10		20		25		ns
t_h	Hold time	Data before $\overline{LE}$ ↓	4.5	3	0		3		3		ns

AC Characteristics for HCT: $t_r = t_f = 6ns$ $C_L = 50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A = 25°C$			GD74HCT259		GD54HCT259		UNIT
			MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation Delay Time D to Qn	4.5		20	38		46		55	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time An to Qn	4.5		20	38		46		55	ns
t_{PLH}/ t_{PHL}	Propagation Delay Time $\overline{LE}$ to Qn	4.5		19	36		44		52	ns
t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Qn	4.5		19	36		44		52	ns
t_{TLH}/ t_{THL}	Output Transition Time	4.5		8	15		18		22	ns

AC Waveforms

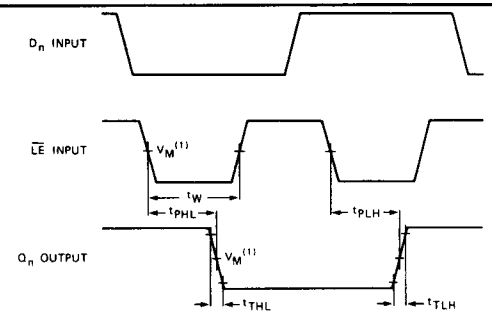


Fig. 3 Waveforms showing the enable input ($\overline{LE}$) to output (Qn) propagation delays, the enable input pulse width and the output transition times.

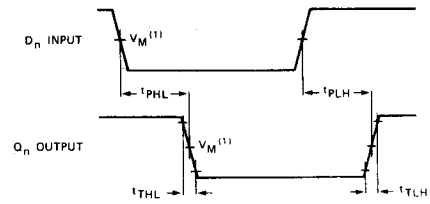


Fig. 4 Waveforms showing the date input (D) to output (Qn) propagation delays and the output transition times.

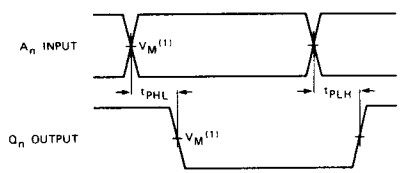


Fig. 5 Waveforms showing the address inputs (An) to outputs (Qn) propagation delays and the output transition times.

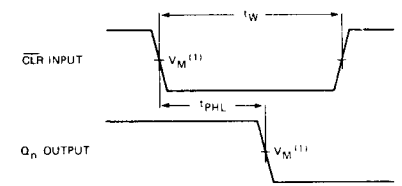


Fig. 6 Waveforms showing the conditional clear input ($\overline{CLR}$) to output (Qn) propagation delays.

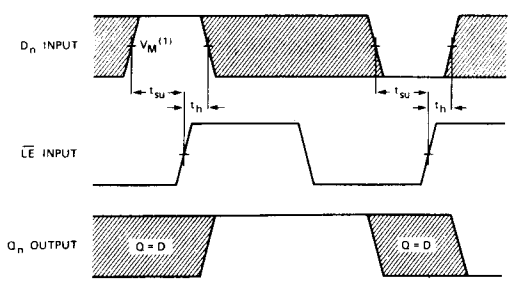


Fig. 7 Waveforms showing the data set-up and hold times for D input to $\overline{LE}$ input.

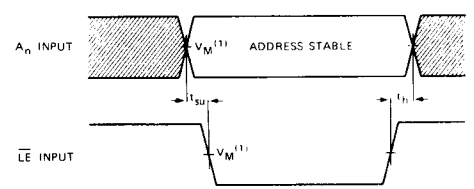


Fig. 8 Waveforms showing the address set-up and hold times for A inputs $\overline{LE}$ input.

Note to Figs 7 and 8
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M=50%; V_I=GND to V_{CC}.
HCT : V_M=1.3V; V_I=GND to 3V.