54F/74F374

Octal D-Type Flip-Flop With 3-State Outputs

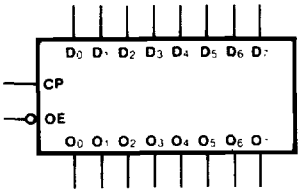
Description

The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

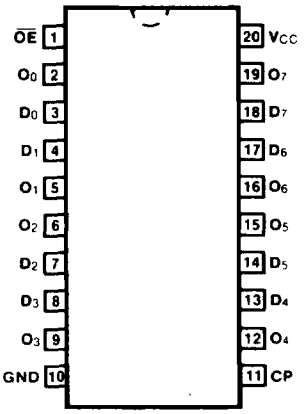
- **Edge-triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus-Oriented Applications**

Ordering Code: See Section 5

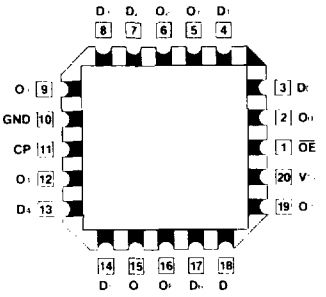
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
O_0-O_7	3-State Outputs	75/15 (12.5)

Functional Description

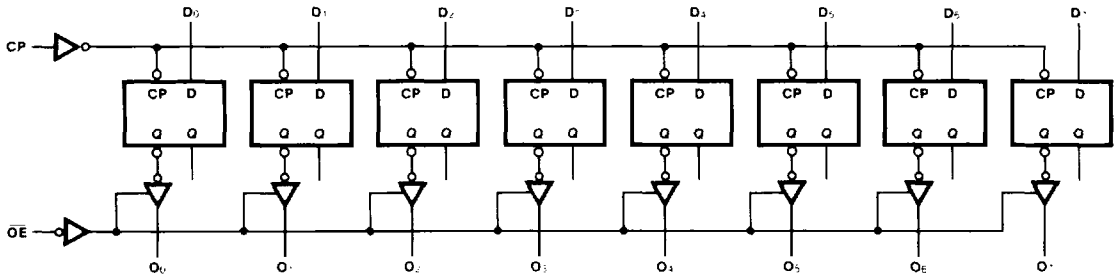
The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs		Outputs	
D_n	CP	$\overline{OE}$	O_n
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current (All Outputs OFF)		55	86	mA	V_{CC} = Max, D_n = Gnd $\overline{OE}$ = HIGH

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$			T_A, V_{CC} = Mil $C_L = 50\ pF$		T_A, V_{CC} = Com $C_L = 50\ pF$			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	140		60		70		MHz	3-1
t_{PLH}	Propagation Delay	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns	3-1
t_{PHL}	CP to O_n	4.0	6.5	8.5	4.0	11.0	4.0	10.0		3-7
t_{PZL}	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	ns	3-1
t_{PZL}		2.0	5.8	7.5	2.0	10.0	2.0	8.5		3-12
t_{PHZ}	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0		3-13
t_{PLZ}		2.0	4.3	5.5	2.0	7.5	2.0	6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
$t_s(H)$	Setup Time, HIGH or LOW	2.0			2.5		2.0		ns	3-5
$t_s(L)$	D_n to CP	2.0			2.0		2.0			
$t_h(H)$	Hold Time, HIGH or LOW	2.0			2.0		2.0			
$t_h(L)$	D_n to CP	2.0			2.5		2.0			
$t_w(H)$	CP Pulse Width	7.0			7.0		7.0		ns	3-7
$t_w(L)$	HIGH or LOW	6.0			6.0		6.0			