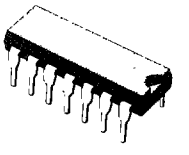
SGS-THOMSON MICROELECTRONICS

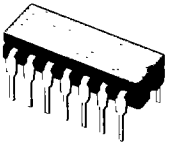
T74LS90
T74LS92/93

COUNTERS: LS90 DECADE LS92 DIVIDE BY TWELVE LS93 4-BIT BINARY

- LOW POWER CONSUMPTION TYPICALLY 45 mW
- HIGH COUNT RATES TYP 50 MHz
- CHOICE OF COUNTING MODES BCD, BI-QUINARY, DIVIDE-BY-TWELVE BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND MOS COMPATIBLE



B1
(Plastic Package)



D1
(Ceramic Package)

M1
(Micro Package)

C1
(Plastic Chip Carrier)

ORDER CODES :

T74LSXX D1	T74LSXX C1
T74LSXX B1	T74LSXX M1

DESCRIPTION

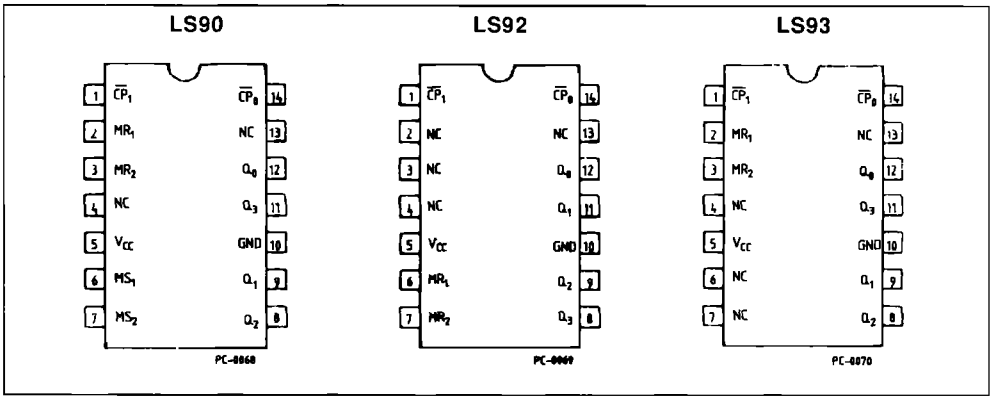
The T74LS90 T74LS92 and T74LS93 are high speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to from BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

PIN NAMES

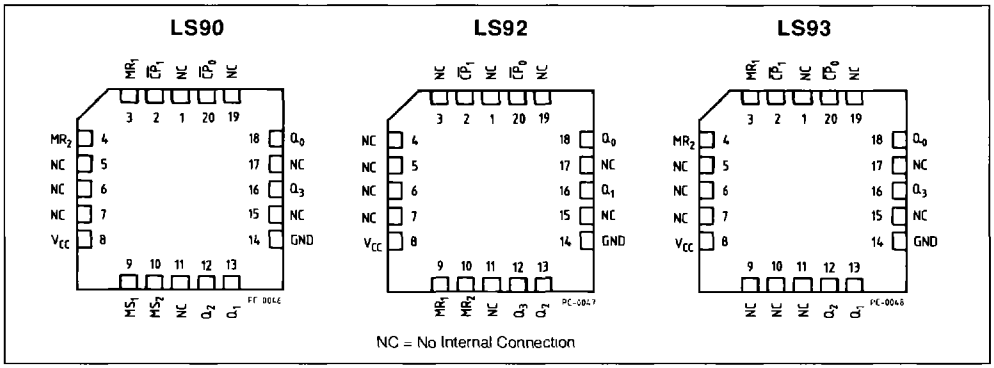
$\overline{CP}_0$	Clock (Active LOW Going Edge) Input to ÷ 2 Section
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to ÷ 5 Section (LS90), ÷ 6 Section (LS92)
$\overline{CP}_1$	Clock (Active LOW Going Edge) Input to ÷ 8 Section (LS93)
MR_1, MR_2	Master Reset (Clear) Inputs
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs
Q_0	Output from ÷ 2 Section
Q_1, Q_2, Q_3	Outputs from ÷ 6 (LS90), ÷ 6 (LS92), ÷ 8 (LS93) Section

Note : The Q_0 Outputs are guaranteed to drive the full fan out plus the $\overline{CP}_1$ input of the device

PIN CONNECTION (top view)



CHIP CARRIER



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.5 to 7	V
V_I	Input Voltage, Applied to Input	– 0.5 to 15	V
V_O	Output Voltage, Applied to Output	– 0.5 to 10	V
I_I	Input Current, into Inputs	– 30 to 5	mA
I_O	Output Current, Into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

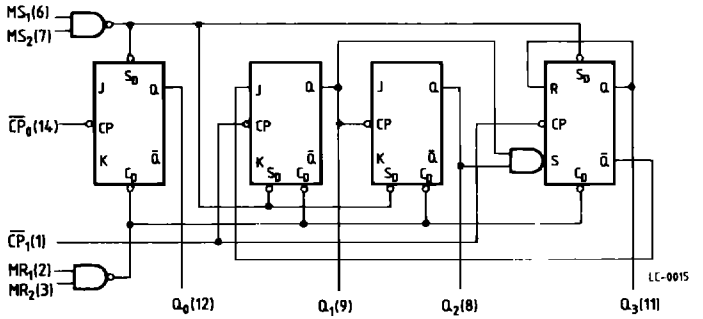
GUARANTEED OPERATING RANGE

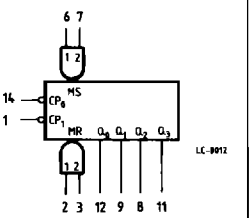
Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS90/92/93XX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

LOGIC DIAGRAM AND LOGIC SYMBOL

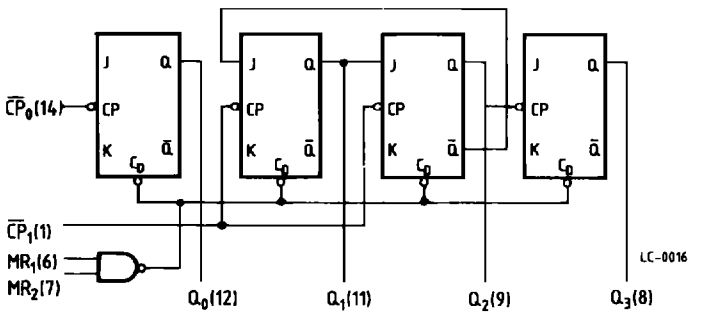
LS90

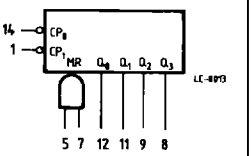




NC = Pins 4, 13

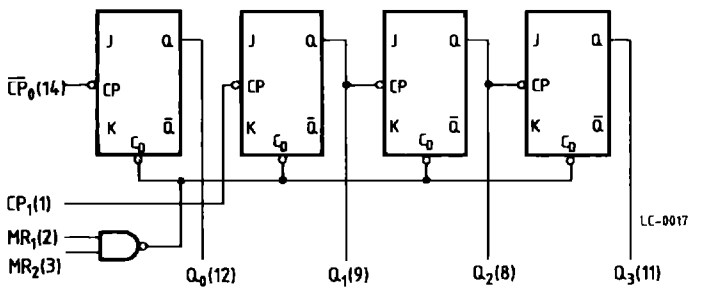
LS92

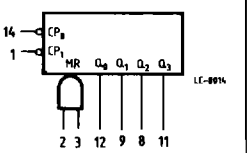




NC = Pins 2, 3, 4, 13

LS93





NC = Pins 4, 6, 7, 13

V_{CC} = Pin 5
GND = Pin 10
( ) = Pin numbers.

FUNCTIONAL DESCRIPTION

The LS90 LS92 and LS93 are 4-bit ripple type Decade, Divide-By-Twelve and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide by six (LS92) or divide-by-eigh (LS93) section. Each section has a separate clock input which initiates state change of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) is provided on the LS90 which overrrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

A. BCD Decade (8421) Counter - The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten counter. The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at outpt Q_0.

C. Divide-By-Two and Divide-By-Five counter - No external interconections are required. The first flip-flop is used as a binary element for the divide-by-two ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo12, Divide By Twelve Counter - The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receivers the incoming count and Q_3 produces a symmetrical divide by twelve square wave output.

B. Divide By Two and Divide By Six Counter - External interconnections are required. The first flip-flop is used as a binary element for the divide by two function. The $\overline{CP}_1$ input is used to obtain divide by three operation at the Q_1 and Q_2 outputs and divide by six at the Q_3 output.

LS93

A. 4-bit Ripple Counter - The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter - the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions fo 2, 4, and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple through counter.

MODE SELECTION LS90

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care.

MODE SELECTION LS92 AND LS93

RESET/INPUTS		OUTPUT			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

BCD COUNT SEQUENCE LS90

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

Note : Output Q_0 connected to input $\overline{CP}_1$ for BCD count.

TRUTH TABLE LS92

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H

Note : Output Q_0 connected to input $\overline{CP}_1$

TRUTH TABLE LS93

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note : Output Q_0 connected to input $\overline{CP}_1$

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Threshold Voltage for All Input		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Threshold Voltage for All Input		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS93) $\overline{CP_1}$ (LS90, LS92)			 2.0 120 40 80	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	MS, MR			0.1	V_{CC} = MAX, V_{IN} = 7.0 V		mA
	$\overline{CP_0}$, $\overline{CP_1}$ (LS93) $\overline{CP_1}$ (LS90, LS92)			0.4 0.8	V_{CC} = MAX, V_{IN} = 5.5 V		mA
I_{IL}	Input LOW Current MS, MR $\overline{CP_0}$ $\overline{CP_1}$ (LS93) $\overline{CP_1}$ (LS90, LS92)			 - 0.4 - 2.4 - 1.6 - 3.2	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{IN} = 0 V		mA
I_{CC}	Power Supply Current		9	15	V_{CC} = MAX		mA

Notes : 1 Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions
2 Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC SET-UP REQUIREMENTS: T_A = 25 °C, V_{CC} = 5.0 V

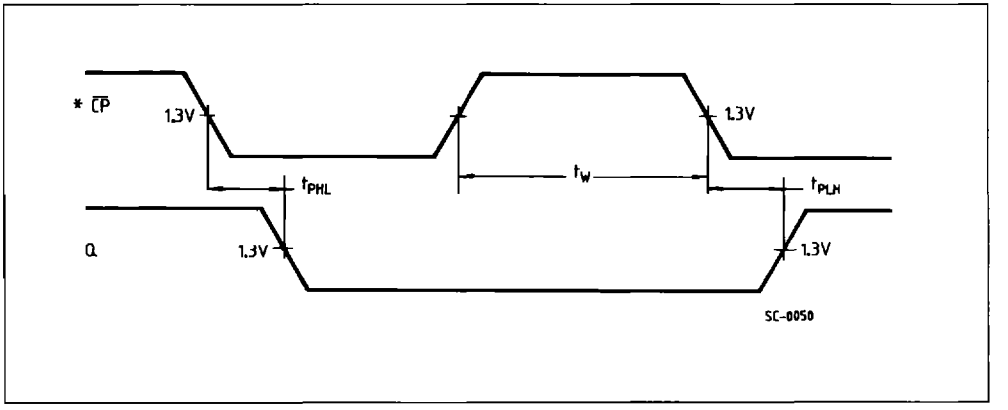
Symbol	Parameter	Limits						Note	Units
		LS90		LS92		LS93			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_w	$\overline{CP_0}$ Pulse Width	15		15		15		Fig. 1	ns
t_w	CP_1 Pulse Width	30		30		30		Fig. 1	
t_w	MR Pulse Width	30		30		30		Fig. 2	
t_w	MS Pulse Width	30						Fig. 2, 3	
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		Fig. 2	
t_{rec}	Recovery Time MS to $\overline{CP}$	25						Fig. 2, 3	

RECOVERY TIME (trec) - is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH to LOW in order to recognize and transfer HIGH data to Q output

AC CHARACTERISTICS $T_A = 25\ °C$. $V_{CC} = 5.0\ V$, $C_L = 15\ pF$

Symbol	Parameter	Limits						Note	Unit
		LS90		LS92		LS93			
		Min.	Max.	Min.	Max.	Min.	Max.		
f_{MAX}	$\overline{CP}_0$ Input Count Frequency	32		32		32		Fig. 1	MHz
f_{MAX}	$\overline{CP}_1$ Input Count Frequency	16		16		16		Fig. 1	MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		16 18		16 18		16 18	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_1 Output		16 21		16 21		16 21	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_2 Output		32 35		16 21		32 35	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_1$ Input to Q_3 Output		32 35		32 35		51 51	Fig. 1	ns
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_3 Output		48 50		48 50		70 70	Fig. 1	ns
t_{PHL}	MS Input to Q_0 and Q_3 Outputs		30					Fig. 3	ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		40					Fig. 2	ns
t_{PHL}	MR Input to any Output		40		40		40	Fig. 2	ns

Figure1.



* The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

Figure 2.

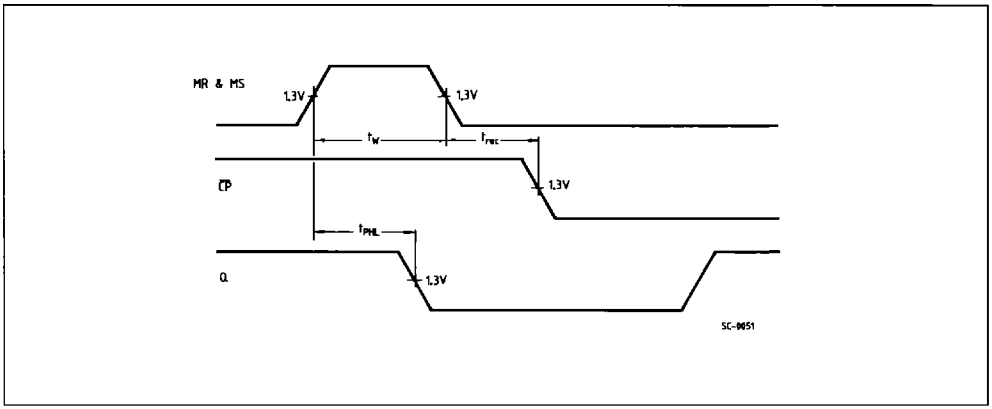


Figure 3.