HARRIS SEMICONDUCTOR

CD74LPT543

December 1996

Fast CMOS 3.3V 8-Bit Latched Transceiver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Active Bus-Hold Circuitry**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT543AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT543AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT543CM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT543CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT543M	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT543QM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

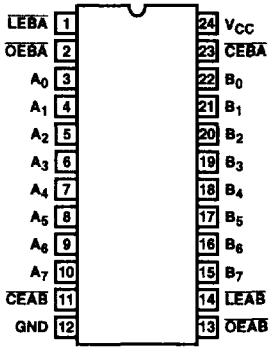
Description

The CD74LPT543 is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or to take data from B_0-B_7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The CD74LPT543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT543
(QSOP, SOIC)
TOP VIEW



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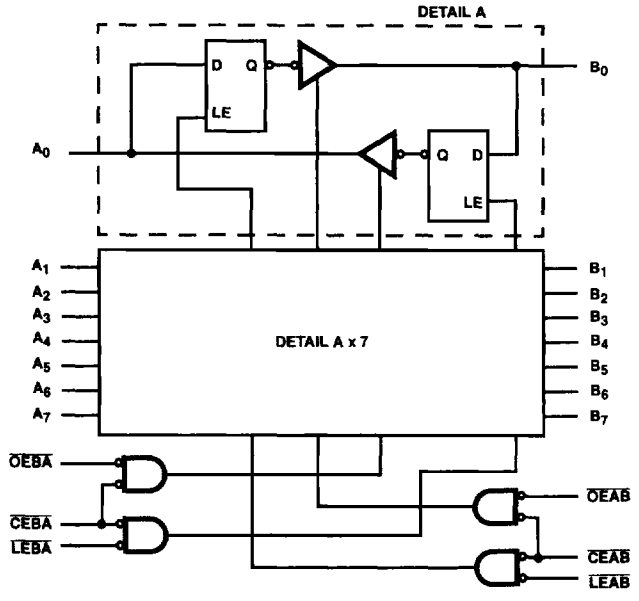
3.3V LPT

File Number **4256**

Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B_0 - B_7
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
2. Before $\overline{LEAB}$ LOW-to-HIGH Transition
3. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0 - A_7	A-to-B Data Inputs or B-to-A Three-State Outputs
B_0 - B_7	B-to-A Data Inputs or B-to-A Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA} = V_{CC}$ 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

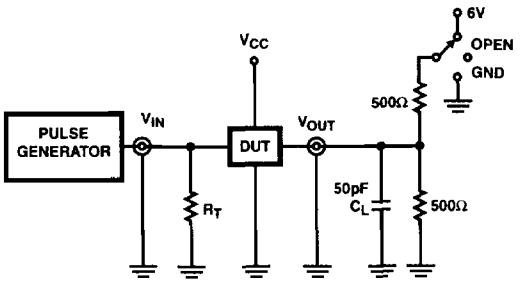
Switching Specifications Over Operating Range (NOTE 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT543		CD74LPT543A		CD74LPT543C		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	ns
Propagation Delay $\overline{LEBA}$ to A_N $\overline{LEAB}$ to B_N	t_{PLH}, t_{PHL}		2.5	12.5	2.5	8.0	2.5	7.0	ns
Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PZH}, t_{PZL}		2.0	12.0	2.0	9.0	2.0	8.0	ns
Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	7.5	2.0	6.5	ns
Setup Time HIGH or LOW, AN or B_N to $\overline{LEAB}$ or $\overline{LEBA}$	t_{SU}		3.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, A_N or B_N to $\overline{LEAB}$ or $\overline{LEBA}$	t_H		2.0	-	2.0	-	2.0	-	ns
$\overline{LEAB}$ or $\overline{LEBA}$ Pulse Width LOW	t_W		5.0	-	5.0	-	5.0	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V 0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

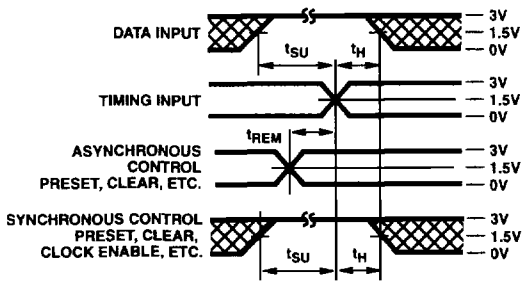


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

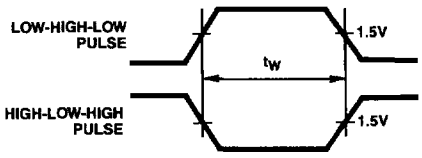


FIGURE 3. PULSE WIDTH

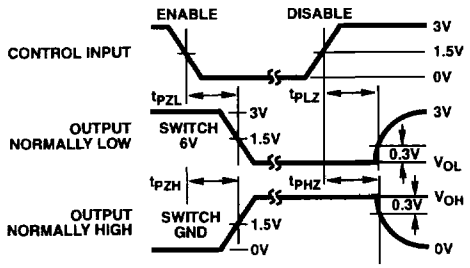


FIGURE 4. ENABLE AND DISABLE TIMING

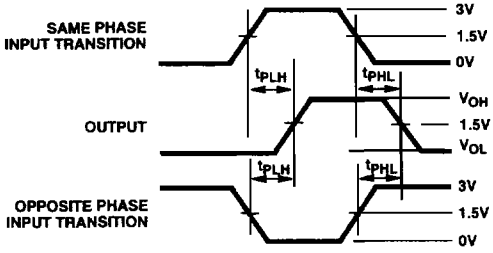


FIGURE 5. PROPAGATION DELAY