# ISL89166, ISL89167, ISL89168

## High Speed, Dual Channel, 6A, Power MOSFET Driver With Programmable Delays

FN7720
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The ISL89166, ISL89167, and ISL89168 are high-speed, 6A, dual channel MOSFET drivers. These parts are similar to the ISL89160, ISL89161, ISL89162 drivers but use the NC pins for programming the rising edge time delays of the outputs used for dead time control.

As an alternative to using external RC circuits for time delays, the programmable delays on the RDTA and RDTB pins allows the user to delay the rising edge of the respective outputs just by connecting an appropriate resistor value between these pins and ground. The accuracy and temperature characteristics of the time delays are specified freeing the user of the need to select appropriate external resistors and capacitors that traditionally are applied to the logic inputs to delay the output edges.

At high switching frequencies, these MOSFET drivers use very little internal bias currents. Separate, non-overlapping drive circuits are used to drive each CMOS output FET to prevent shoot-thru currents in the output stage.

The start-up sequence is design to prevent unexpected glitches when $V_{DD}$ is being turned on or turned off. When $V_{DD}$ < ~1V, an internal 10kΩ resistor between the output and ground helps to keep the output voltage low. When ~1V <$V_{DD}$ < UV, both outputs are driven low with very low resistance and the logic inputs are ignored. This insures that the driven FETs are off. When $V_{DD}$ > UVLO, and after a short delay, the outputs now respond to the logic inputs.

## Features

- Typical ON-resistance <1Ω
- Specified Miller plateau drive currents
- Very low thermal impedance ($\theta_{JC}$ = 3°C/W)
- Hysteretic Input logic levels for 3.3V CMOS, 5V CMOS, and TTL
- Precision threshold inputs for optional time delays with external RC components
- Instead of RC components for time delays, a resistor can be used to program delays
- 20ns rise and fall time driving a 10nF load.
- NC pins may be connected to ground or VDD for flexible PCB layout options

## Applications

- Synchronous Rectifier (SR) Driver
- Switch mode power supplies
- Motor Drives, Class D amplifiers, UPS, Inverters
- Pulse Transformer Driver
- Clock/Line Driver

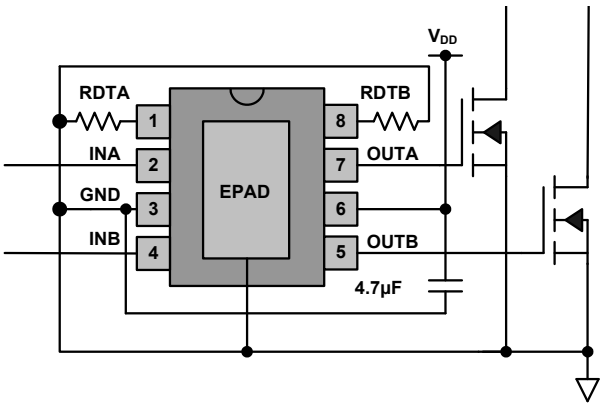



FIGURE 1. TYPICAL APPLICATION

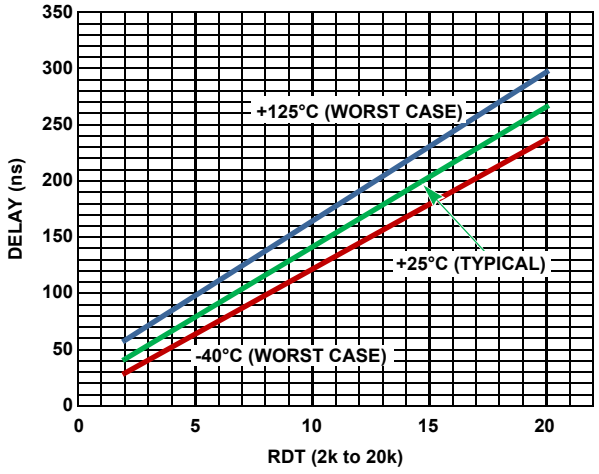
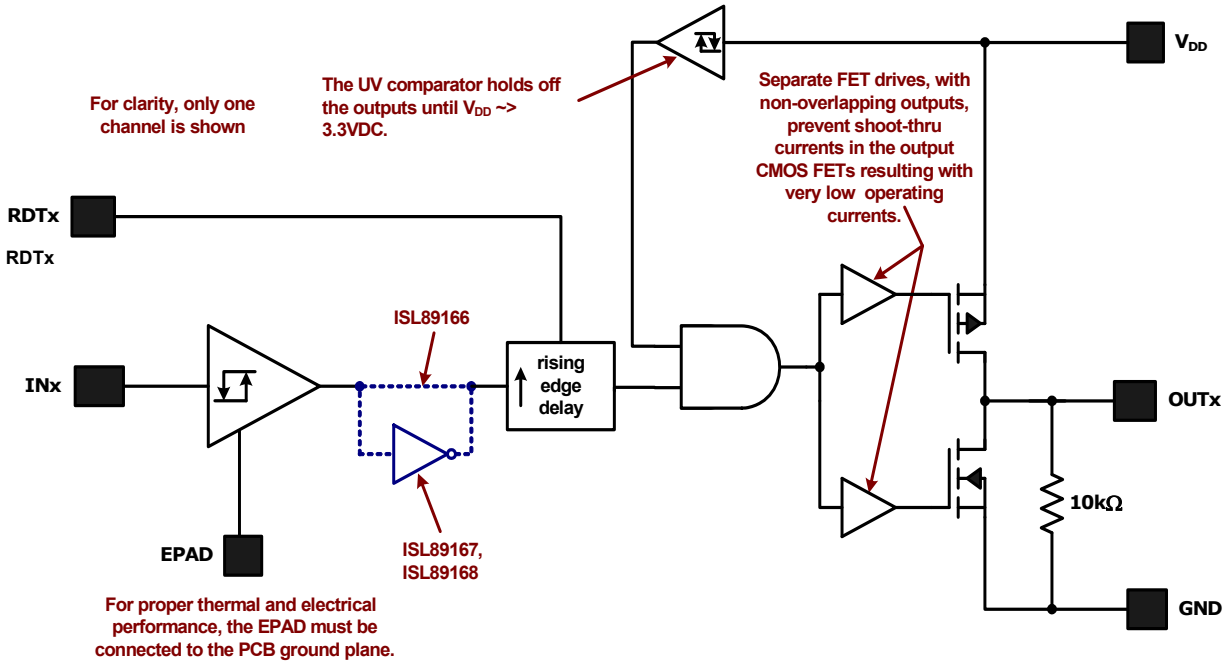


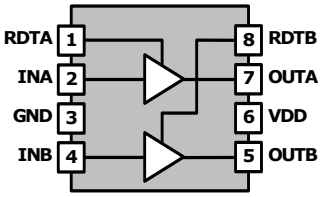

FIGURE 2. PROGRAMMABLE TIME DELAYS

# Block Diagram

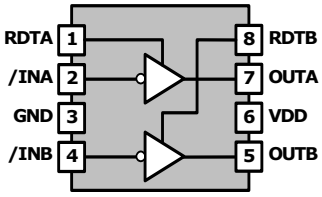



# Pin Configurations

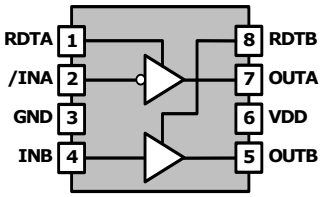
ISL89166FR, ISL89166FB
(8 LD TDFN, EPSOIC)
TOP VIEW




ISL89167FR, ISL89167FB
(8 LD TDFN, EPSOIC)
TOP VIEW




ISL89168FR, ISL89168FB
(8 LD TDFN, EPSOIC)
TOP VIEW




# Pin Descriptions

| PIN NUMBER | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | RDTA | Connect a resistor between this pin and ground to program the rising edge delay of OUTA, 0k to 20k |
| 2 | INA or /INA | Channel A input, 0V to VDD |
| 3 | GND | Power Ground, 0V |
| 4 | INB or /INB | Channel B enable, 0V to VDD |
| 5 | OUTB | Channel B output |
| 6 | VDD | Power input, 4.5V to 16V |
| 7 | OUTA | Channel A output, 0V to VDD |
| 8 | RDTB | Connect a resistor between this pin and ground to program the rising edge delay of OUTB, 0k to 20k |
| | EPAD | Power Ground, 0V |

# Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | TEMP RANGE (°C) | INPUT CONFIGURATION | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|---|
| ISL89166FRTAZ | 166A | -40 to +125 | non-inverting | 8 Ld 3x3 TDFN | L8.3x3I |
| ISL89167FRTAZ | 167A | -40 to +125 | inverting | 8 Ld 3x3 TDFN | L8.3x3I |
| ISL89168FRTAZ | 168A | -40 to +125 | inverting + non-inverting | 8 Ld 3x3 TDFN | L8.3x3I |
| ISL89166FBEAZ | 89166 FBEAZ | -40 to +125 | non-inverting | 8 Ld EPSOIC | M8.15D |
| ISL89167FBEAZ | 89167 FBEAZ | -40 to +125 | inverting | 8 Ld EPSOIC | M8.15D |
| ISL89168FBEAZ | 89168 FBEAZ | -40 to +125 | inverting + non-inverting | 8 Ld EPSOIC | M8.15D |

NOTES:

1. Add "-T*", suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL89166, ISL89167, ISL89168. For more information on MSL, please see Technical Brief TB363.

## Absolute Maximum Ratings

Supply Voltage, $V_{DD}$ Relative to GND . . . . . -0.3V to 18V
Logic Inputs (INA, INB) . . . . . GND - 0.3v to $V_{DD}$ + 0.3V
Outputs (OUTA, OUTB) . . . . . GND - 0.3v to $V_{DD}$ + 0.3V
Average Output Current (Note 6) . . . . . 150mA

**ESD Ratings**
Human Body Model Class 2 (Tested per JESD22-A114E) . . . . . 2000V
Machine Model Class B (Tested per JESD22-A115-A) . . . . . 200V
Charged Device Model Class IV. . . . . 1000V

**Latch-Up**
(Tested per JESD-78B; Class 2, Level A)
Output Current . . . . . 500mA

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 8 Ld TDFN Package (Notes 4, 5). . . . . | 44 | 3 |
| 8 Ld EPSOIC Package (Notes 4, 5). . . . . | 42 | 3 |

Max Power Dissipation at +25°C in Free Air . . . . . 2.27W
Max Power Dissipation at +25°C with Copper Plane . . . . . 33.3W
Storage Temperature Range. . . . . -65°C to +150°C
Operating Junction Temp Range . . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Maximum Recommended Operating Conditions

Junction Temperature . . . . . -40°C to +125°C
Supply Voltage, $V_{DD}$ Relative to GND. . . . . 4.5V to 16V
Logic Inputs (INA, INB). . . . . 0V to $V_{DD}$
Outputs (OUTA, OUTB) . . . . . 0V to $V_{DD}$

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379 for details.
5. For $\theta_{JC}$, the “case temp” location is the center of the exposed metal pad on the package underside.
6. The average output current, when driving a power MOSFET or similar capacitive load, is the average of the rectified output current. The peak output currents of this driver are self limiting by transconductance or $r_{DS(ON)}$ and do not required any external components to minimize the peaks. If the output is driving a non-capacitive load, such as an LED, maximum output current must be limited by external means to less than the specified absolute maximum.

## DC Electrical Specifications

$V_{DD}$ = 12V, GND = 0V, No load on OUTA or OUTB, RDTA = RDTB = 0kΩ unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C.**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = +25°C | | | $T_J$ = -40°C to +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN (Note 7) | MAX (Note 7) | |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | $V_{DD}$ | | - | - | - | **4.5** | **16** | V |
| $V_{DD}$ Quiescent Current | $I_{DD}$ | INx = GND | - | 5 | - | - | - | mA |
| | | INA = INB = 1MHz, square wave | - | 25 | - | - | - | mA |
| **UNDERVOLTAGE** | | | | | | | | |
| VDD Undervoltage Lock-out (Note 9) (Figure 9) | $V_{UV}$ | INA = INB = True (Note 10) | - | 3.3 | - | - | - | V |
| Hysteresis | | | - | ~25 | - | - | - | mV |
| **INPUTs** | | | | | | | | |
| Input Range for INA, INB | $V_{IN}$ | | - | - | - | **GND** | **$V_{DD}$** | V |
| Logic 0 Threshold for INA, INB | $V_{IL}$ | Nominally 37% x 3.3V | - | 1.22 | - | **1.12** | **1.32** | V |
| Logic 1 Threshold for INA, INB | $V_{IH}$ | Nominally 63% x 3.3V | - | 2.08 | - | **1.98** | **2.18** | V |
| Input Capacitance of INA, INB (Note 8) | $C_{IN}$ | | - | 2 | - | - | - | pF |

## DC Electrical Specifications

$V_{DD}$ = 12V, GND = 0V, No load on OUTA or OUTB, RDTA = RDTB = 0kΩ unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C. (Continued)**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = +25°C | | | $T_J$ = -40°C to +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN (Note 7) | MAX (Note 7) | |
| Input Bias Current for INA, INB | $I_{IN}$ | GND < $V_{IN}$ < $V_{DD}$ | - | - | - | **-10** | **+10** | µA |
| **OUTPUTS** | | | | | | | | |
| High Level Output Voltage | $V_{OHA}$ $V_{OHB}$ | | - | - | - | **$V_{DD}$ - 0.1** | **$V_{DD}$** | V |
| Low Level Output Voltage | $V_{OLA}$ $V_{OLB}$ | | - | - | - | **GND** | **GND + 0.1** | V |
| Peak Output Source Current | $I_O$ | $V_O$ (initial) = 0V, $C_{LOAD}$ = 10nF | - | -6 | - | - | - | A |
| Peak Output Sink Current | $I_O$ | $V_O$ (initial) = 12V, $C_{LOAD}$ = 10nF | - | +6 | - | - | - | A |

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. This parameter is taken from the simulation models for the input FET. The actual capacitance on this input will be dominated by the PCB parasitic capacitance.
9. A 400µs delay further inhibits the release of the output state when the UV positive going threshold is crossed. See Figure 9
10. The true state of a specific part number is defined by the input logic symbol.

## AC Electrical Specifications

$V_{DD}$ = 12V, GND = 0V, No Load on OUTA or OUTB, RDTA = RDTB = 0kΩ unless Otherwise Specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C.**

| PARAMETERS | SYMBOL | TEST CONDITIONS /NOTES | $T_J$ = +25°C | | | $T_J$ = -40°C to +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN (Note 7) | MAX (Note 7) | |
| Output Rise Time (see Figure 4) | $t_R$ | $C_{LOAD}$ = 10nF, 10% to 90% | - | 20 | - | - | **40** | ns |
| Output Fall Time (see Figure 4) | $t_F$ | $C_{LOAD}$ = 10nF, 90% to 10% | - | 20 | - | - | **40** | ns |
| Output Rising Edge Propagation Delay (see Figure 3) | $t_{RDLY}$ | RDTx = 0kΩ | - | 25 | - | - | **50** | ns |
| Output Falling Edge Propagation Delay (see Figure 3) (Note 12) | $t_{FDLY}$ | RDTx = 0kΩ | - | 25 | - | - | **50** | ns |
| Rising Propagation Matching (see Figure 3) | $t_{RM}$ | RDTx = 0kΩ | - | <1ns | - | - | - | ns |
| Falling Propagation Matching (see Figure 3) | $t_{FM}$ | RDTx = 0kΩ | - | <1ns | - | - | - | ns |
| Rising edge timer delay (Note 11) | $t_{RTDLY20}$ | RTx = 20kΩ, No load | - | 266 | - | **237** | **297** | ns |
| | $t_{RTDLY2}$ | RTx = 2.0kΩ, No load | - | 42 | - | **29** | **58** | ns |
| Miller Plateau Sink Current (See Test Circuit Figure 5) | $-I_{MP}$ | $V_{DD}$ = 10V, $V_{MILLER}$ = 5V | - | 6 | - | - | - | A |
| | $-I_{MP}$ | $V_{DD}$ = 10V, $V_{MILLER}$ = 3V | - | 4.7 | - | - | - | A |
| | $-I_{MP}$ | $V_{DD}$ = 10V, $V_{MILLER}$ = 2V | - | 3.7 | - | - | - | A |

**AC Electrical Specifications** $V_{DD}$ = 12V, GND = 0V, No Load on OUTA or OUTB, RDTA = RDTB = 0kΩ unless Otherwise Specified. **Boldface limits apply over the operating junction temperature range, -40°C to +125°C. (Continued)**

| PARAMETERS | SYMBOL | TEST CONDITIONS /NOTES | $T_J$ = +25°C | | | $T_J$ = -40°C to +125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN (Note 7) | MAX (Note 7) | |
| Miller Plateau Source Current (See Test Circuit Figure 6) | $I_{MP}$ | $V_{DD}$ = 10V, $V_{MILLER}$ = 5V | - | 5.2 | - | - | - | A |
| | $I_{MP}$ | $V_{DD}$ = 10V, $V_{MILLER}$ = 3V | - | 5.8 | - | - | - | A |
| | $I_{MP}$ | $V_{DD}$ = 10V, $V_{MILLER}$ = 2V | - | 6.9 | - | - | - | A |

NOTE:

11. The rising edge delay timer increases the propagation delay for values of RDTx > 2.0kΩ. Time delays for RDTx < 2.0kΩ and RDTx > 20kΩ are not specified and are not recommended. The resistors tolerances (including the boundary values of 2.0kΩ and 20.0kΩ) are recommended to be 1% or better.
12. The falling edge propagation delays are independent of the RDT value.

# Test Waveforms and Circuits

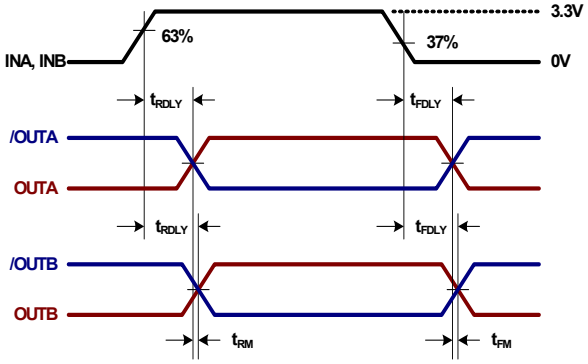



FIGURE 3. PROP DELAYS AND MATCHING

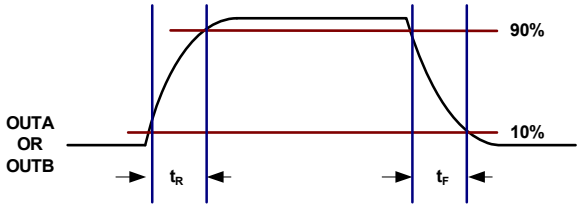



FIGURE 4. RISE/FALL TIMES

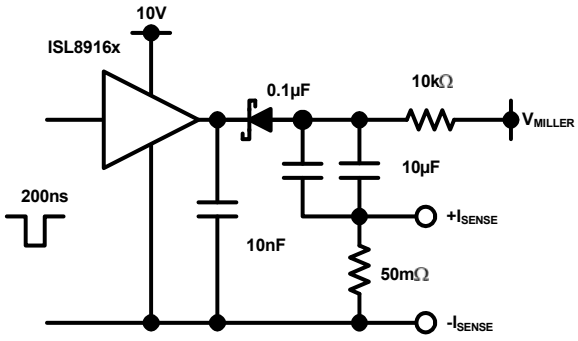



FIGURE 5. MILLER PLATEAU SINK CURRENT TEST CIRCUIT

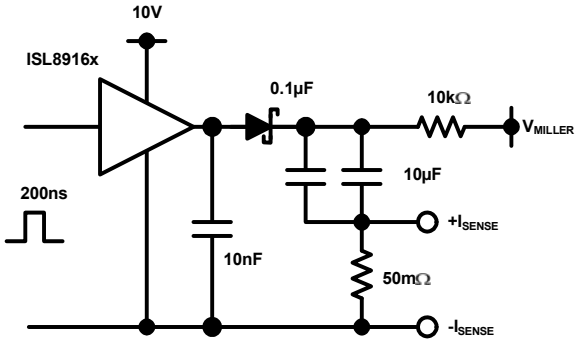



FIGURE 6. MILLER PLATEAU SOURCE CURRENT TEST CIRCUIT

## Test Waveforms and Circuits (Continued)

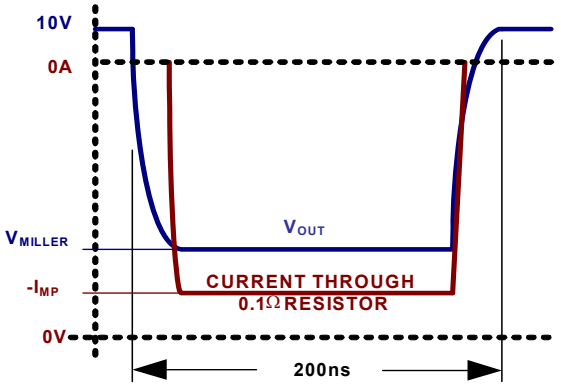



FIGURE 7. MILLER PLATEAU SINK CURRENT

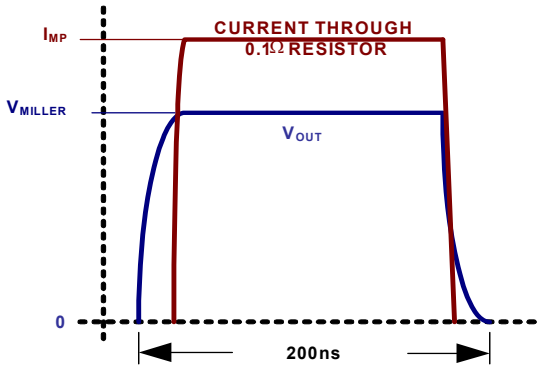



FIGURE 8. MILLER PLATEAU SOURCE CURRENT

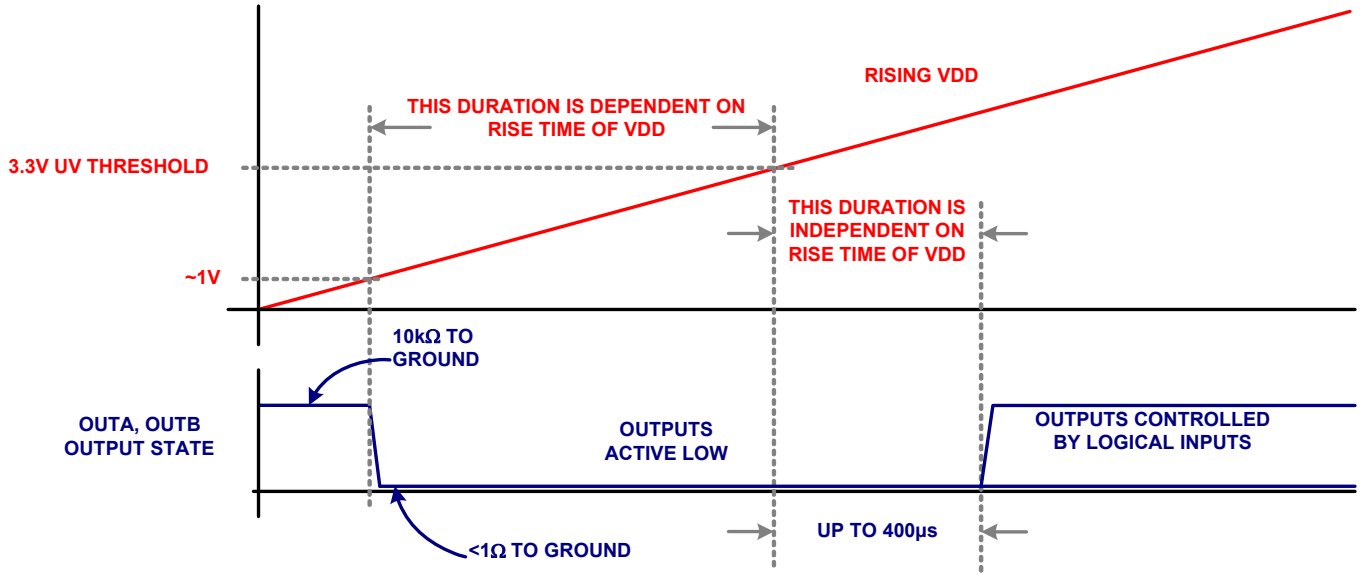



FIGURE 9. START-UP SEQUENCE

## Typical Performance Curves

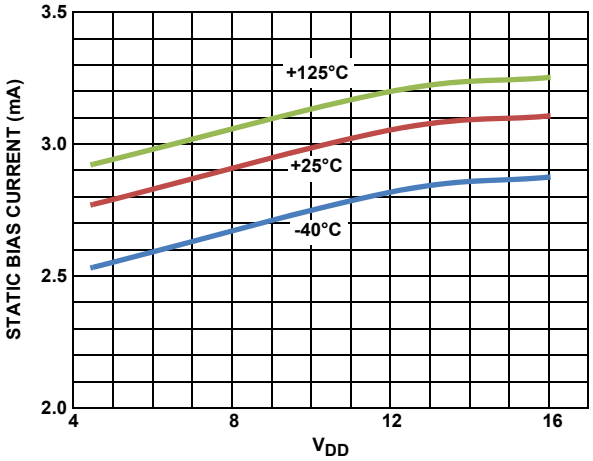



FIGURE 10. $I_{DD}$ vs $V_{DD}$ (STATIC)

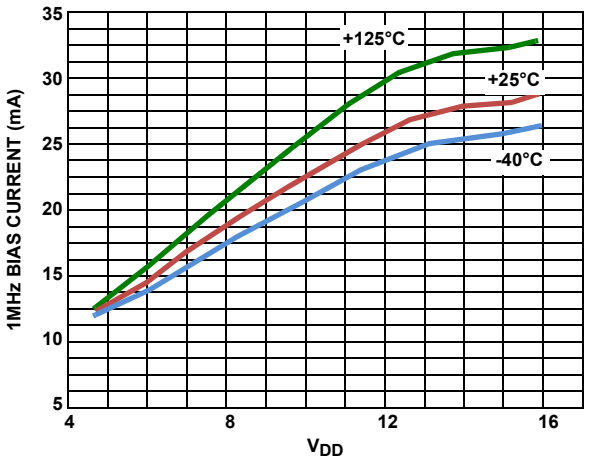



FIGURE 11. $I_{DD}$ vs $V_{DD}$ (1MHz)

## Typical Performance Curves (Continued)

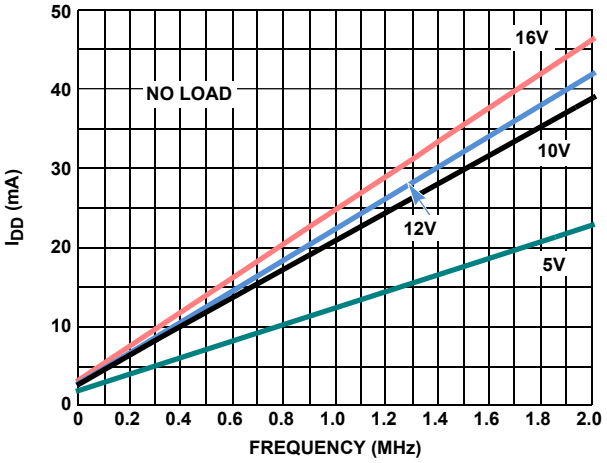



FIGURE 12. $I_{DD}$ vs FREQUENCY (+25°C)

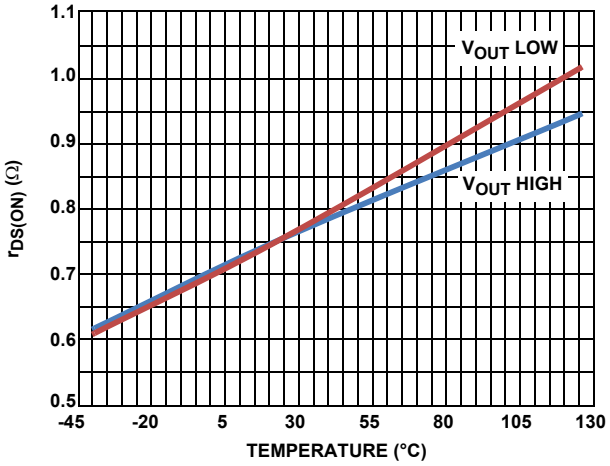



FIGURE 13. $r_{DS(ON)}$ vs TEMPERATURE

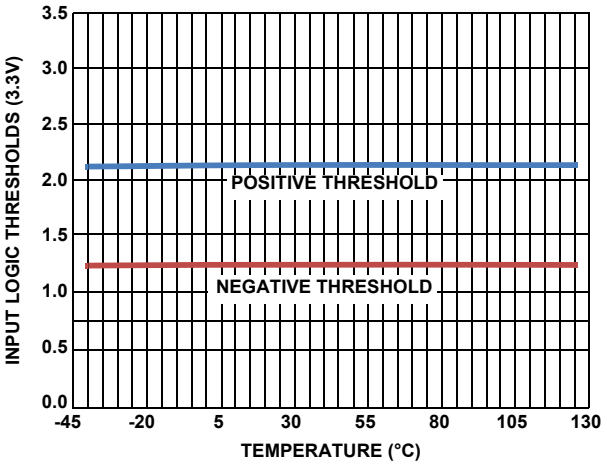



FIGURE 14. INPUT THRESHOLDS

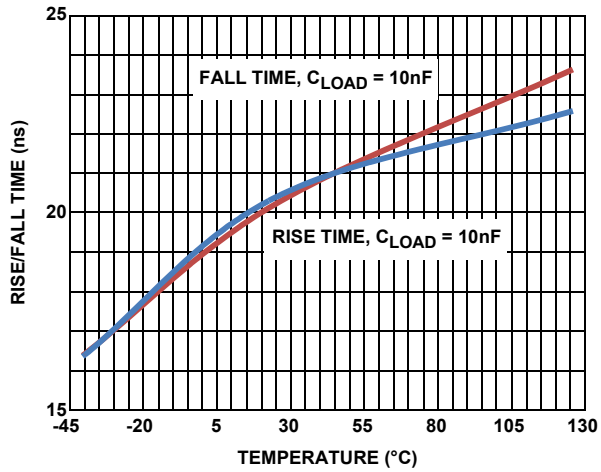



FIGURE 15. OUTPUT RISE/FALL TIME

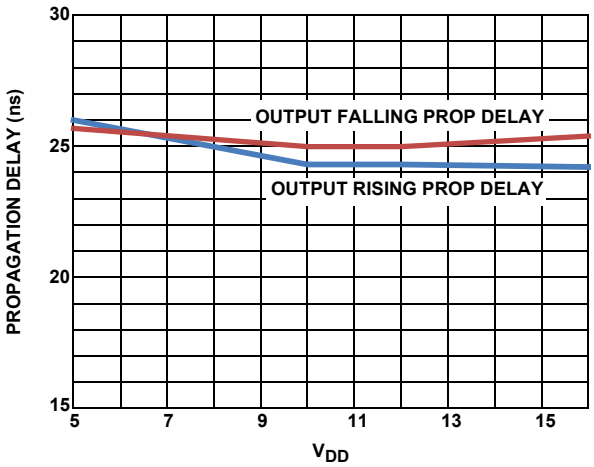



FIGURE 16. PROPAGATION DELAY vs $V_{DD}$

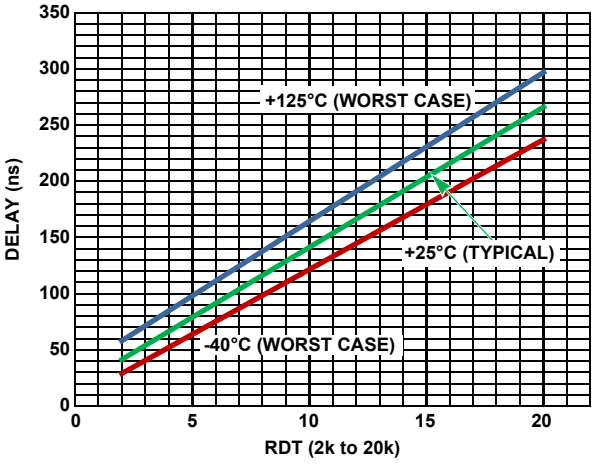



FIGURE 17. PROPAGATION DELAY vs RDT

# Functional Description

## Overview

The ISL89166, ISL89167, ISL89168 drivers incorporate several features including precision input logic thresholds, undervoltage lock-out, fast rising high output drive currents and programmable rising edge output delays.

The programmable delays require only a resistor connecter between the RDTA or RDTB pins and ground. This is a useful feature to create dead times for bridge applications to prevent shoot-through or for synchronous rectifier applications to adjust the timing.

Fast rising (or falling) output drive current of the ISL89166, ISL89167, ISL89168 minimizes the turn-on (off) delay due to the input capacitance of the driven FET. The switching transition period at the Miller plateau is also minimized by the high drive currents. (See the specified Miller plateau currents in the AC Electrical Specifications on page 5).

The start-up sequence for is designed to prevent unexpected glitches when $V_{DD}$ is being turned on or turned off. When $V_{DD}$ < ~1V, an internal 10kΩ resistor connected between the output and ground, help to keep the gate voltage close to ground. When ~1V<$V_{DD}$ < UV, both outputs are driven low while ignoring the logic inputs. This low state has the same current sinking capacity as during normal operation. This insures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates via the Miller capacitance. When $V_{DD}$ > UVLO, and after a 400µs delay, the outputs now respond to the logic inputs. See Figure 9 for complete details.

For the negative transition of $V_{DD}$ through the UV lockout voltage, the outputs are active low when $V_{DD}$ < ~3.2$V_{DC}$ regardless of the input logic states.

# Application Information

## Programming Rising Edge Delays

As compared to setting the output delays of a driver using an resistor, capacitor and diode on the logic inputs, programming the rising edge output delays of the ISL89166, ISL89167, ISL89168 is almost trivial.

All that is necessary is to select the required resistor value from the Propagation Delay vs RDT graph, Figure 17. Unlike using an RCD network, the operating tolerances over temperature are specified. If a traditional RCD network (Figure 19) is used on the input logic, then it is necessary to account for the tolerance of the logic input threshold, the tolerances of R and C, and their temperature sensitivity.

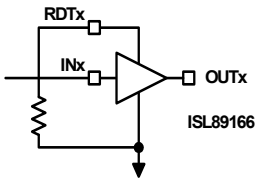



FIGURE 18. SETTING DELAYS WITH A RESISTOR

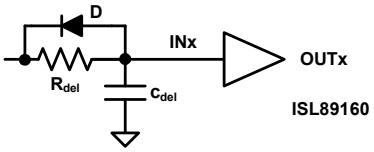



FIGURE 19. SETTING DELAYS WITH A RCD NETWORK

## Paralleling Outputs to Double the Peak Drive Currents

The typical propagation matching of the ISL89166 and ISL89167 is less than 1ns. **Note that the propagation matching is only valid when RTDA and RTDB = 0kΩ.** The matching is so precise that carefully matched and calibrated scopes probes and scope channels must be used to make this measurement. Because of this excellent performance, these driver outputs can be safely paralleled to double the current drive capacity. It is important that the INA and INB inputs be connected together on the PCB with the shortest possible trace. This is also required of OUTA and OUTB. Note that the ISL89168 cannot be paralleled because of the complementary logic.

## Power Dissipation of the Driver

The power dissipation of the ISL89166, ISL89167, ISL89168 is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant as compared to the gate charge losses.

Figure 20 illustrates how the gate charge varies with the gate voltage in a typical power MOSFET. In this example, the total gate charge for $V_{gs}$ = 10V is 21.5nC when $V_{DS}$ = 40V. This is the charge that a driver must source to turn-on the MOSFET and must sink to turn-off the MOSFET.

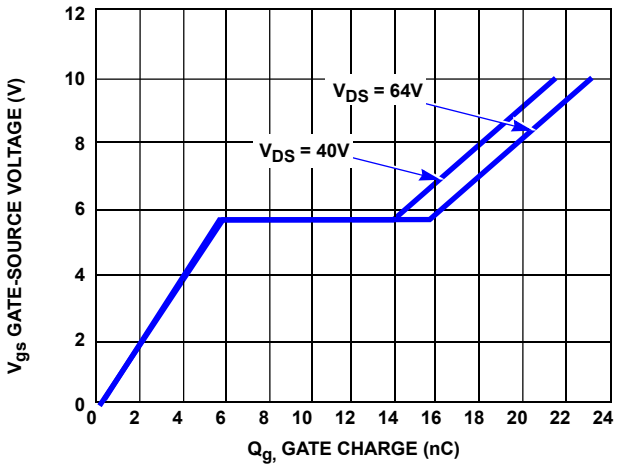



FIGURE 20. MOSFET GATE CHARGE vs GATE VOLTAGE

Equation 1 shows calculating the power dissipation of the driver:

$$P_D = 2 \bullet Q_c \bullet freq \bullet V_{GS} \bullet \frac{R_{gate}}{R_{gate} + r_{DS(ON)}} + I_{DD}(freq) \bullet V_{DD} \quad \text{(EQ. 1)}$$

Where:

freq = Switching frequency,

$V_{GS} = V_{DD}$ bias of the ISL89166, ISL89167, ISL89168

$Q_c$ = Gate charge for $V_{GS}$

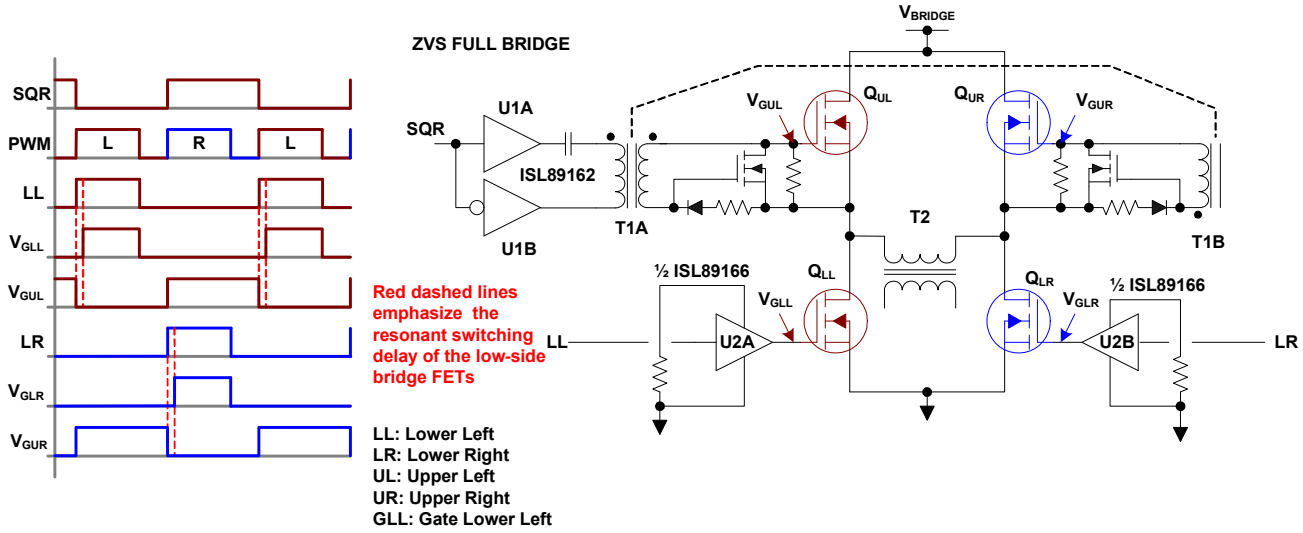
$I_{DD}$(freq) = Bias current at the switching frequency (see Figure 10 on page 7)

$r_{DS(ON)}$ = ON-resistance of the driver

$R_{gate}$ = External gate resistance (if any).

Note that the gate power dissipation is proportionally shared with the external gate resistor. When sizing an external gate resistor, do not overlook the power dissipated by this resistor.

# Typical Application Circuit



The Typical Application Circuit is an example of how the ISL89166, ISL89167, ISL89168, MOSFET drivers can be applied in a zero voltage switching full bridge. Two main signals are required: a 50% duty cycle square wave (SQR) and a PWM signal synchronized to the edges of the SQR input. An ISL89162 is used to drive T1 with alternating half cycles driving $Q_{UL}$ and $Q_{UR}$. An ISL89166 is used to drive $Q_{LL}$ and $Q_{LR}$ also with alternating half cycles. Unlike the two high side bridge FETs, the two low-side bridge FETs are turned on with a rising edge delay. The delay is setup by resistors connected to RDTA and RDTB pins of the ISL89166. The duration of the delay is chosen to turn on the low-side FETs when the voltage on their respective drains is at the resonant valley.

# General PCB Layout Guidelines

The AC performance of the ISL89166, ISL89167, ISL89168 depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET.
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they are usually more effective than parallel traces.
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt will induce currents and consequently, noise voltages in the low level signal lines.
- When practical, minimize impedances in low level signal circuits. The noise, magnetically induced on a 10k resistor, is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling.
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductance in the VDD and GND leads. To be effective, these caps must also have the shortest possible conduction paths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits especially on OUTA and OUTB. If an external gate resistor is unacceptable, then the layout must be improved to minimize lead inductance.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL89166, ISL89167, ISL89168.
- Avoid having a signal ground plane under a high amplitude dv/dt circuit. This will inject di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Many PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic caps, power resistors, etc.) will have internal parasitic inductance which cannot be eliminated.
  This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components especially parasitic inductance.

# General EPAD Heatsinking Considerations

The thermal pad is electrically connected to the GND supply through the IC substrate. The epad of the ISL89166, ISL89167, ISL89168 has two main functions: to provide a quiet GND for the input threshold comparators and to provide heat sinking for the IC. The EPAD must be connected to a ground plane and no switching currents from the driven FET should pass through the ground plane under the IC.

Figure 21 is a PCB layout example of how to use vias to remove heat from the IC through the epad.

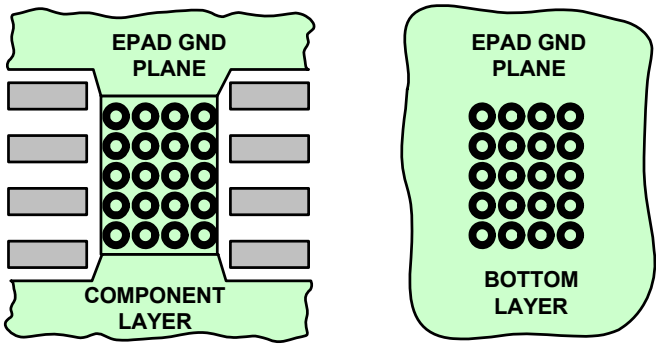



FIGURE 21. TYPICAL PCB PATTERN FOR THERMAL VIAS

For maximum heatsinking, it is recommended that a ground plane, connected to the EPAD, be added to both sides of the PCB. A via array, within the area of the EPAD, will conduct heat from the EPAD to the GND plane on the bottom layer. The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the ISL89166, ISL89167, ISL89168, the air flow and the maximum temperature of the air around the IC.

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

| DATE | REVISION | CHANGE |
|---|---|---|
| December 21, 2012 | FN7720.2 | Removed retired parts ISL8916xFRTBZ, ISL8916xFRTCZ, ISL8916xFBEBZ, ISL8916xFBECZ from “Ordering Information” on page 3.<br>(page 4) Abs Max Ratings ESD Ratings Charged Device Model changed from "1500" to "1000" |
| January 31, 2012 | FN7720.1 | (page 1) Figure 1 illustration improved.<br>(page 1) Last paragraph of the product description is changed to better describe the improved turn on characteristics.<br>(page 1) Features list is revised to improve readability and to add new product specific features.<br>(page 3) Updated Ordering information with new parts.<br>(page 4) Abs Max Ratings ESD Ratings Charged Device Model changed from "1000" to "1500"<br>(page 4) Note and figure references are added to the VDD Under-voltage lock-out parameter.<br>(page 5) Note 9 is revised to more clearly describe the turn-on characteristics. Changed "200µs" to "400µs"<br>(page 6) Wording of Note 11 is revised to correctly label the RDT resistors.<br>(page 7) Figure 9 added to clearly define the startup characteristics.<br>(page 9) The paragraphs of the Functional Description Overview describing the turn-on sequence is replaced by 3 paragraphs to more clearly describe the under voltage and turn-on and turn-off characteristics.<br>(page 9) A new section is added to the application information describing how the drivers outputs can be paralleled.<br>(pages 1..12) Various minor corrections to text for grammar and spelling.<br>M8.15D POD on page 14 - Converted to new POD format. Removed table of dimensions and moved dimensions onto drawing. Added land pattern. |
| January 14, 2011 | FN7720.0 | Initial Release |

# About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the fastest growing markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil or to find out how to become a member of our winning team, visit our website and career page at www.intersil.com.

For a complete listing of Applications, Related Documentation and Related Parts, please see the respective product information page. Also, please check the product information page to ensure that you have the most updated datasheet: ISL89166, ISL89167, ISL89168

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

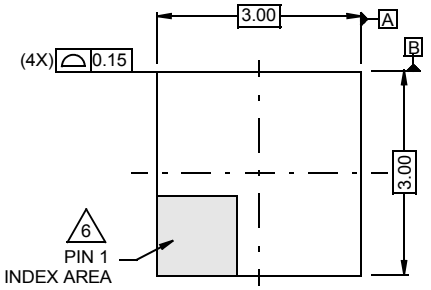
Reliability reports are available from our website at: http://rel.intersil.com/reports/search.php

# Package Outline Drawing

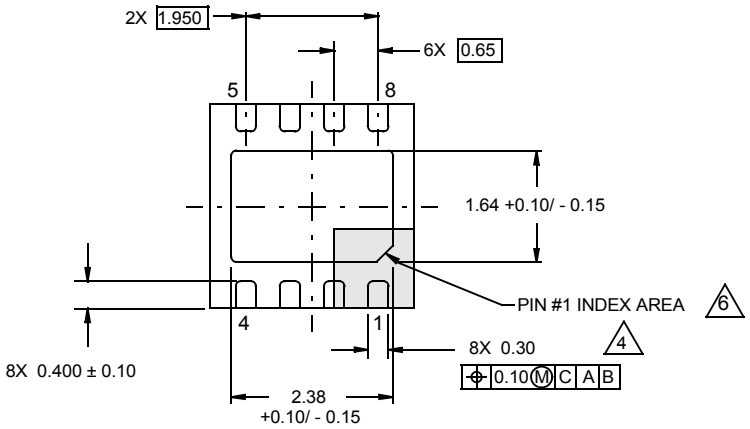
## L8.3x3I

**8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE**

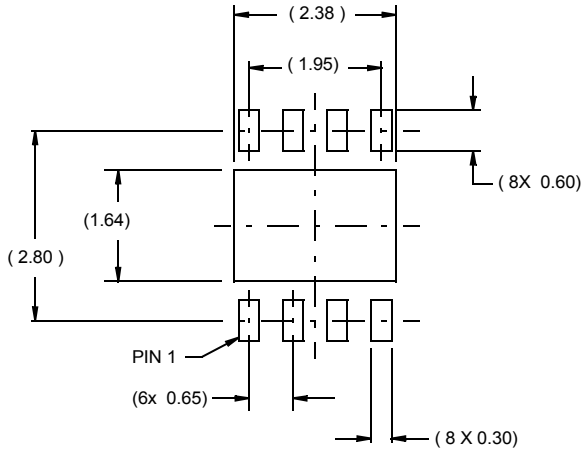
**Rev 1 6/09**



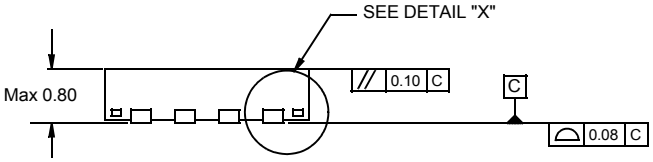

**TOP VIEW**



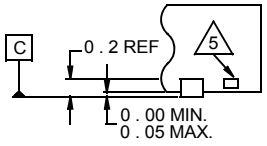

**BOTTOM VIEW**




**TYPICAL RECOMMENDED LAND PATTERN**




**SIDE VIEW**




**DETAIL "X"**

NOTES:

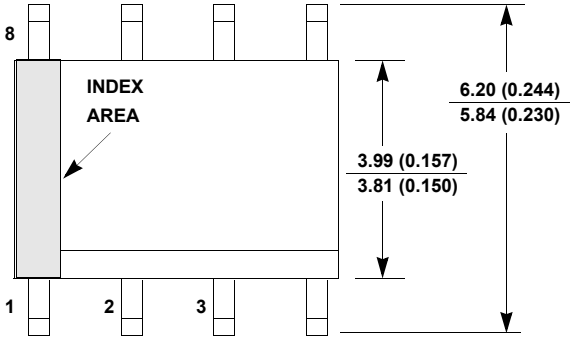
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

# Package Outline Drawing

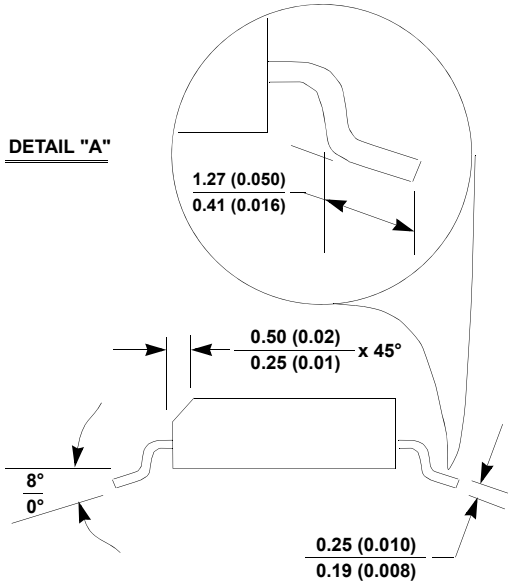
## M8.15D

**8 LEAD NARROW BODY SMALL OUTLINE EXPOSED PAD PLASTIC PACKAGE**

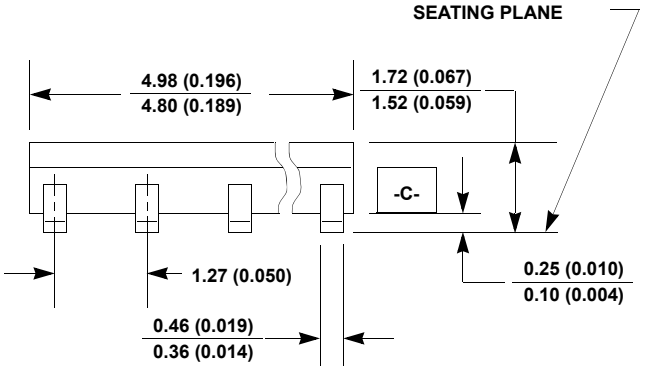
**Rev 1, 3/11**



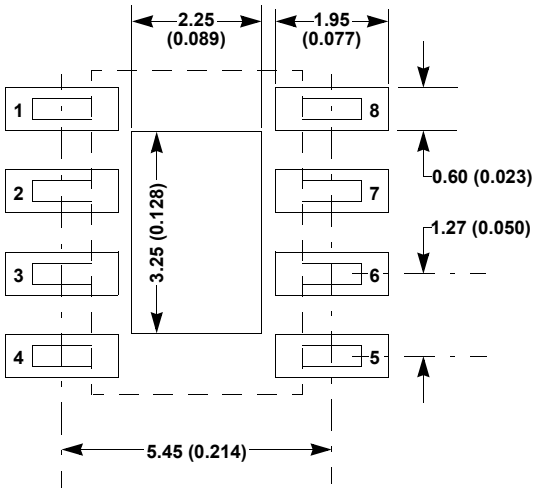

TOP VIEW



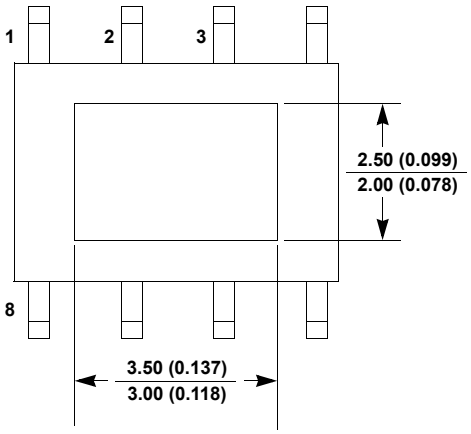

SIDE VIEW "B"




SIDE VIEW "A




TYPICAL RECOMMENDED LAND PATTERN




BOTTOM VIEW

**NOTES:**

1. Dimensions are in millimeters. Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing per ASME-Y14.5M-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The Pin 1 identifier may be either a mold or a mark feature.
6. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.