Signetics

Military Logic Products

54S253
Multiplexer

Dual 4-Input Multiplexer (3-State)

Product Specification

FEATURES

- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

DESCRIPTION

The 54S253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are High, the outputs are forced to a High impedance (Hi-Z) state.

The 54S253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot + I_{3a} \cdot S_1 S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 S_0)$$

All but one device must be in the High impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

ORDERING INFORMATION

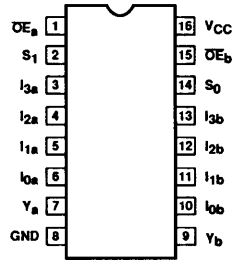
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S253/BEA
16-Pin Ceramic FlatPack	54S253/BFA
20-Pin Ceramic LLCC	54S253/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
All	Inputs	1SUL
All	Outputs	10SUL

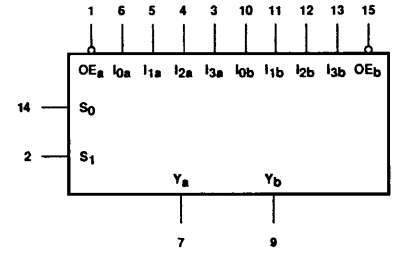
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



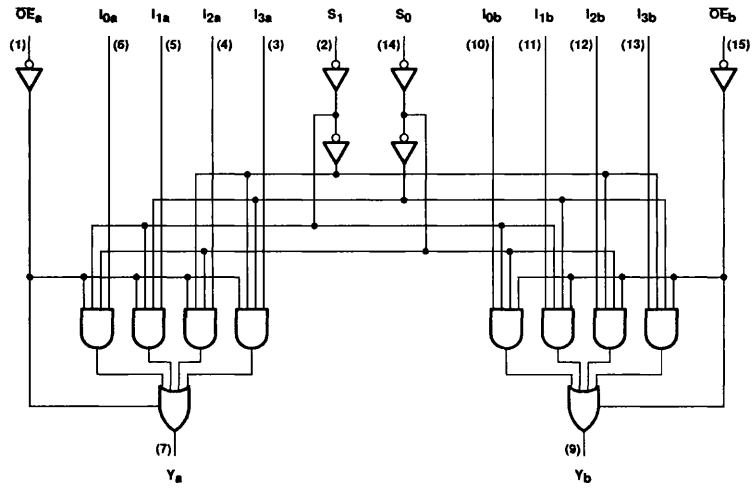
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC Pin Assignment, See JEDEC Standard No. 2

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			+0.8	V
	+125°C			+0.7	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-2.0	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max,				0.5	V
		I_{OL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{OZH}	Off-state output current, High-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 2.4V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied	V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V				-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CCH}	Supply current[4] (total)	V_{CC} = Max	Condition 1			70	mA
I_{CCL}	Supply current[4] (total)	V_{CC} = Max	Condition 2			80	mA
I_{CCZ}	Supply current[4] (total)	V_{CC} = Max	Condition 3			100	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 15pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		18 18	ns ns
t_{PZH}	Output enable to High level	Waveform 2		13	ns
t_{PZL}	Output enable to Low level	Waveform 3		14	ns
t_{PHZ}	Output disable from High level	Waveform 2 – C_L = 5pF[5]		8.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – C_L = 5pF[5]		14	ns
t_{PHZ}	Output disable from High level	Waveform 2 – C_L = 50pF		13.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – C_L = 50pF		15.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		11.5 11.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		20.5 20.5	ns ns
t_{PZH}	Output enable to High level	Waveform 2		15.5	ns
t_{PZL}	Output enable to Low level	Waveform 3		16.5	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 5pF$[5]		8.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 5pF$[5]		14	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 50pF$		13.5	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 50pF$		15.5	ns

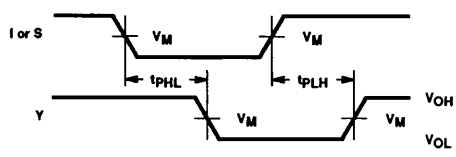
AC ELECTRICAL CHARACTERISTICS $T_A = -55°C$ and $+125°C$, $V_{CC} = 5.0V$[6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		27 27	ns ns
t_{PZH}	Output enable to High level	Waveform 2		20	ns
t_{PZL}	Output enable to Low level	Waveform 3		21	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 5pF$[5]		11	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 5pF$[5]		18	ns
t_{PHZ}	Output disable from High level	Waveform 2 – $C_L = 50pF$		18	ns
t_{PLZ}	Output disable from Low level	Waveform 3 – $C_L = 50pF$		20	ns

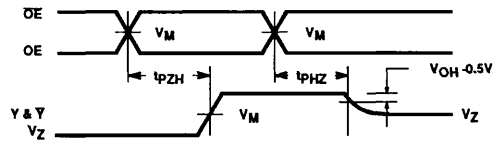
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured under the following conditions with the outputs open: *Condition* 1: All inputs grounded. *Condition* 2: All inputs at $\geq 4.0V$ except $\overline{OE}$ which is grounded. *Condition* 3: $\overline{OE} \geq 4.0V$ all inputs grounded.
5. Guaranteed by the 50pF limits, but not tested.
6. These parameters are guaranteed, but not tested.

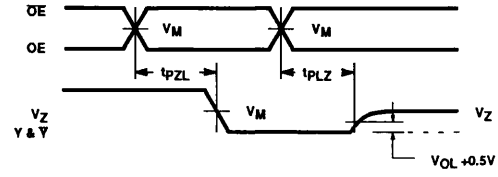
AC WAVEFORMS



Waveform 1. Waveform for Non-Inverting Outputs



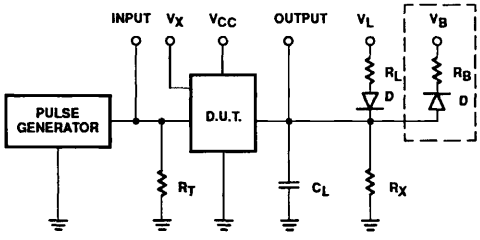
Waveform 2. 3-State Enable Time to High Level and Disable Time from High Level



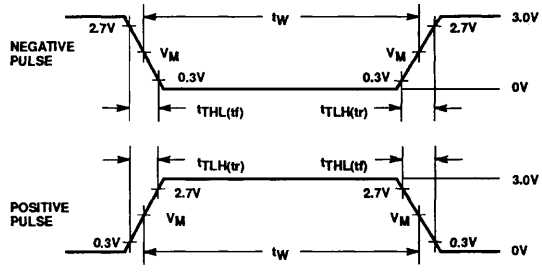
Waveform 3. 3-State Enable Time to Low Level and Disable Time from Low Level

FAMILY	V_M	V_{MZL}	V_{MZH}	V_Z
54SXXX	1.5V	0.7V	2.0V	1.65V

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 3-State Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS							
	R_L	R_X	V_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	82Ω	560Ω	2.5V	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

Optional load for 54LSXXX only: R_B = 631Ω; V_B = 5.5V for all tests except T_{PHZ}; V_B = -0.6V for T_{PHZ} test.

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.