National Semiconductor

PRELIMINARY

DM54AS253/DM74AS253 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and a non-inverting Tri-state output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS253	−55°C to 125°C
DM74AS253	0° to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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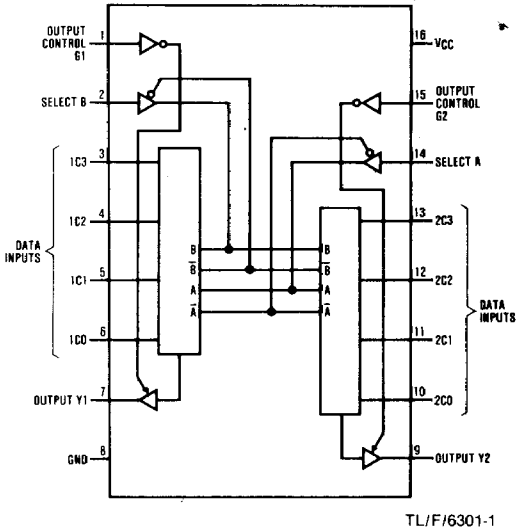
Connection Diagram

Dual-In-Line Package



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54AS253 (J) 74AS253 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Recommended Operating Conditions

Parameter	DM54AS253			DM74AS253			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range.

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_{IN} = -18mA$				−1.2	V
V_{OH}	High Level Output Voltage	$V_{CC} = 4.5V$, I_{OH} = Max		2.4	3.2		V
		$I_{OH} = -2mA$, $V_{OC} = 4.5V$ to 5.5V		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, I_{OL} = Max			0.35	0.5	V
I_I	Input Current at Max Input Voltage	$V_{CC} = 5.5V$, $V_{IN} = 7V$	A, B			0.2	mA
			All Others			0.1	
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 2.7V$	A, B			40	μA
			All Others			20	
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$	A, B		−0.6	−1	mA
			All others		−0.3	−0.5	
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_{OUT} = 2.25V$		−30		−112	mA
I_{OZH}	Off-State Output Current, High Bias	$V_{CC} = 5.5V$, $V_{OUT} = 2.7V$				50	μA
I_{OZL}	Off-State Output Current, Low Bias	$V_{CC} = 5.5V$, $V_{OUT} = 0.4V$				−50	μA
I_{CC}	Supply Current	$V_{CC} = 5.5V$	Outputs high		17	29	mA
			Outputs low		20	32	
			Outputs disabled		21	33	

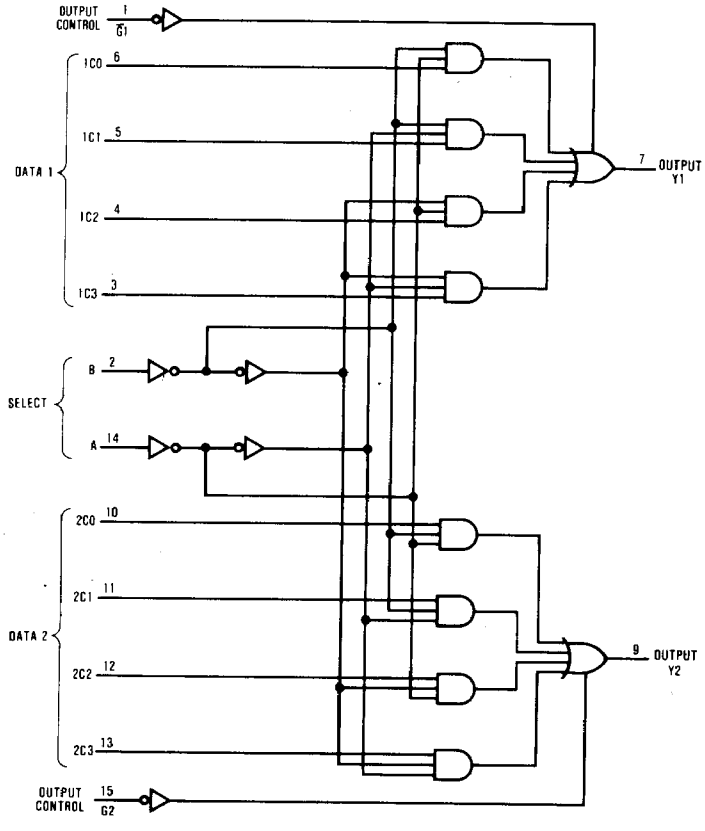
Switching Characteristics over recommended operating free air temperature range (Note 1).

All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$.

Parameter	From	To	Conditions	DM54AS253			DM74AS253			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	4		14.5	4		13.5	ns
t_{PHL}, High to low Level Output				4		12	4		11.5	ns
t_{PLH}, Low to high Level Output	Data			3		8.5	3		7.5	ns
t_{PHL}, High to low Level Output				3		8.5	3		7.5	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y		4		13	4		12.5	ns
t_{ZL}, Output Enable Time to Low Level				4		12	4		11.5	ns
t_{HZ}, Output Disable Time From High Level				2		6.5	2		6	ns
t_{LZ}, Output Disable Time From Low Level				2		8	2		7	ns

Note 1: See Section 1 for test waveforms and output load.

Logic Diagram



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