M5M418165BJ,TP-6,-7,-8,-6S,-7S,-8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418165BXX-6,6S	60	15	30	15	110	850
M5M418165BXX-7,7S	70	20	35	20	130	750
M5M418165BXX-8,8S	80	20	40	20	150	650

XX=J,TP

- Standard 42 pin SOJ,50 pin TSOP
- Single 5.5V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ····· CMOS Input level
- Low operating power dissipation
  M5M418165Bxx- 6,6S ---------- 940.0mW (Max)
  M5M418165Bxx- 7,7S ---------- 830.0mW (Max)
  M5M418165Bxx- 8,8S ---------- 720.0mW (Max)
- Hyper-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~A_9)

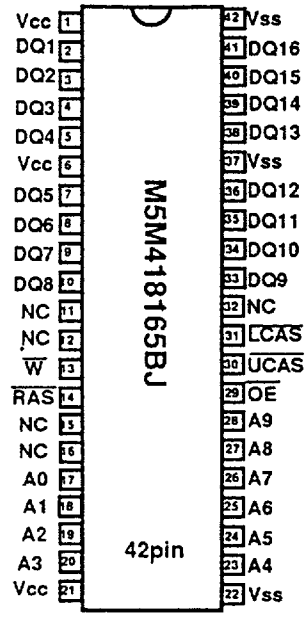
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

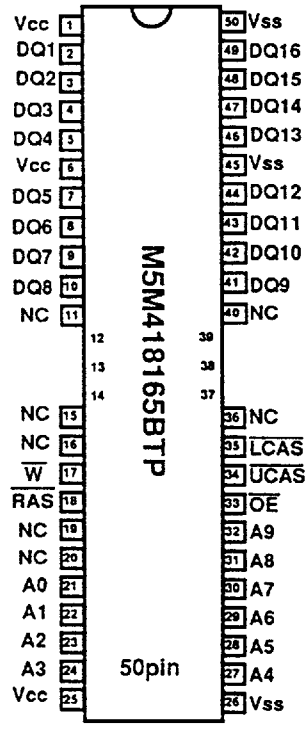
PIN DESCRIPTION

Pin Name	Function
A_0-A_9	Address Inputs
DQ_1-DQ_{16}	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{UCAS}$	Upper Bite Control Column Address Strobe Input
$\overline{LCAS}$	Lower Bite Control Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0K (400mil SOJ)



Outline 50P3W-L (400mil TSOP Normal Bend)

MITSUBISHI ELECTRIC

Apr. 1995

M5M418165BJ,TP-6,-7,-8,-6S,-7S,-8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

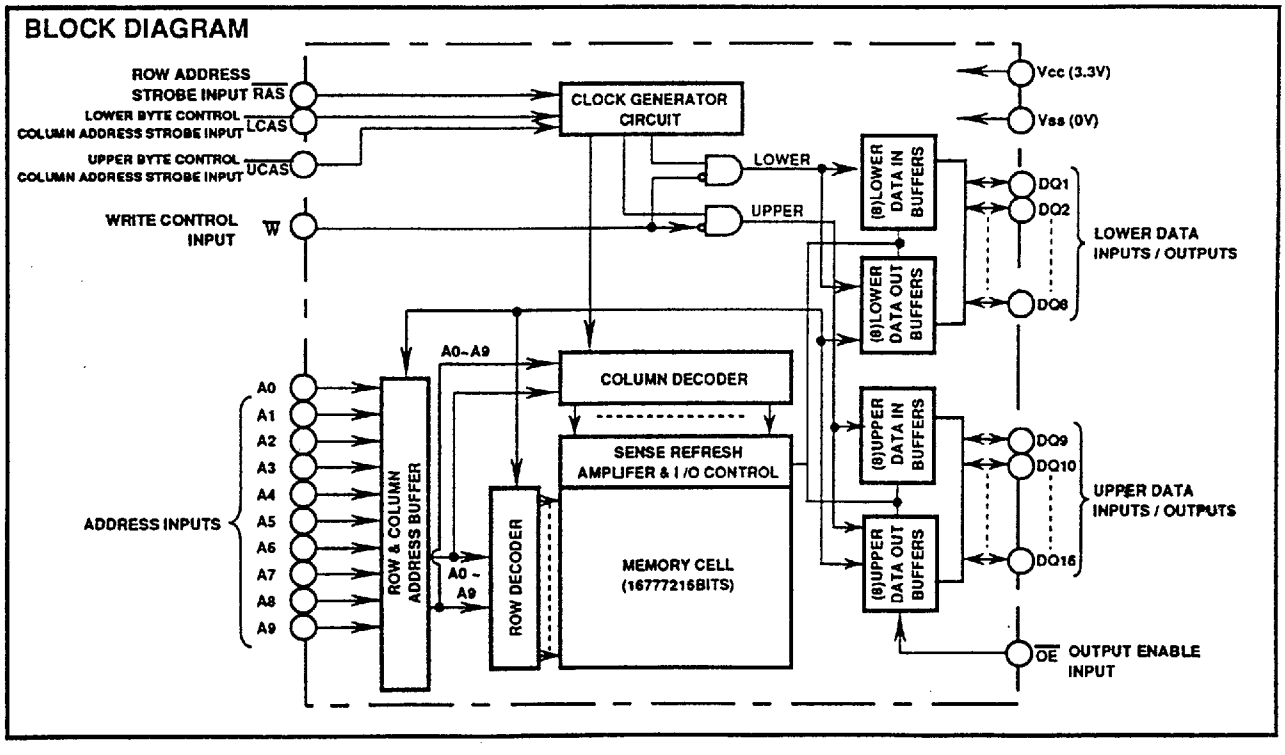
The M5M418165BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$ only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1~7	V
VI	Input voltage		-1~7	V
VO	Output voltage		-1~7	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.4		6.0	V
VIL	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH=-5.0mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL=4.2mA	0		0.4	V
IOZ	Off-state output current		Q floating 0V≦VOUT≦5.5V	-5		5	μA
II	Input current		0V≦VIN≦6V, Other inputs pins=0V	-5		5	μA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M418165B-6,6S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC=tWC=min. output open			170	mA
		M5M418165B-7,7S				150	
		M5M418165B-8,8S				130	
ICC2	Supply current from Vcc , stand-by (Note 6)		$\overline{RAS}$= $\overline{CAS}$ =VIH, output open			2	mA
			$\overline{RAS}$= $\overline{CAS}$ ≧Vcc -0.2 V			1	
ICC3 (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M418165B-6,6S	$\overline{RAS}$ cycling, $\overline{CAS}$= VIH tRC=min. output open			170	mA
		M5M418165B-7,7S				150	
		M5M418165B-8,8S				130	
ICC4(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M418165B-6,6S	$\overline{RAS}$=VIL, $\overline{CAS}$ cycling tPC=min. output open			135	mA
		M5M418165B-7,7S				115	
		M5M418165B-8,8S				95	
ICC6(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M418165B-6,6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC=min. output open			170	mA
		M5M418165B-7,7S				150	
		M5M418165B-8,8S				130	

Note 2: Current flowing into an IC is positive, out is negative.
3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.
5: Column Address can be changed once or less while RAS=VIL and $\overline{LCAS}$/$\overline{UCAS}$=VIH .

M5M418165BJ,TP-6,-7,-8,-6S,-7S,-8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0 ~ 70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M418165BJ, TP	VI=Vss f=1MHz VI=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input					7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
$C_{I/O}$	Input/Output capacitance, data ports					8	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc = 5V ±10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		15		20		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		60		70		80	ns
tAA	Column address access time	(Note 7,10)		30		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40		45	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20		20	ns
tOHC	Output hold time from $\overline{CAS}$		5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		15		20		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		15		20		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		15		20		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		15		20		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-5mA) / VOL=0.4V(IOL=-4.2mA) load 100pF.

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ(max)}$, $t_{WEZ(max)}$, $t_{OFF(max)}$ and $t_{REZ(max)}$ defines the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 10$ uA) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write ,Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~70°C, Vcc = 5V ±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		16.4		16.4		16.4	ms
tRP	$\overline{RAS}$ high pulse width	40		50		60		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note16)	20	38	20	42	20	42	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
tCPN	$\overline{CAS}$ high pulse width	10		13		13		ns
tRAD	Column address delay time from $\overline{RAS}$ low (Note17)	15	30	15	35	15	40	ns
tASR	Row address setup time before $\overline{RAS}$ low	0		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low (Note18)	0	13	0	13	0	13	ns
tRAH	Row address hold time after $\overline{RAS}$ low	10		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low	10		10		10		ns
tDZC	Delay time, data to $\overline{CAS}$ low (Note19)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low (Note19)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data (Note20)	15		20		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data (Note20)	15		20		20		ns
tODD	Delay time, $\overline{OE}$ high to data (Note20)	15		20		20		ns
tT	Transition time (Note21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are assumed tT =2ns.

15: $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

16: $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is controlled exclusively by t_{CAC} or t_{AA}.

17: $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$, access time is controlled exclusively by t_{AA}.

18: $t_{ASC(max)}$ is specified as a reference point only. If $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$, access time is controlled exclusively by t_{CAC}.

19: Either t_{DZC} or t_{DZO} must be satisfied.

20: Either t_{RDD} or t_{CDD} or t_{ODD} must be satisfied.

21: t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width	10	10000	13	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		62		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		ns
tRCS	Read Setup time before $\overline{CAS}$ low	0		0		0		ns
tRCH	Read hold time after $\overline{CAS}$ high (Note 22)	0		0		0		ns
tRRH	Read hold time after $\overline{RAS}$ high (Note 22)	10		10		10		ns
tRAL	Column address to $\overline{RAS}$ hold time	30		35		40		ns
tCAL	Column address to $\overline{CAS}$ hold time	18		23		23		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low	15		20		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low	15		20		20		ns

Note 22: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tWC	Write cycle time	110		130		150		ns
tRAS	$\overline{RAS}$ low pulse width	60	10000	70	10000	80	10000	ns
tCAS	$\overline{CAS}$ low pulse width	10	10000	13	10000	13	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	48		55		63		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	15		20		20		ns
tWCS	Write setup time before $\overline{CAS}$ low (Note 24)	0		0		0		ns
tWCH	Write hold time after $\overline{CAS}$ low	10		13		15		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low	10		13		15		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low	10		13		15		ns
tWP	Write pulse width	10		13		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low	0		0		0		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low	10		13		15		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time (Note23)	133		161		183		ns
tRAS	$\overline{RAS}$ low pulse width	89	10000	107	10000	126	10000	ns
tCAS	$\overline{CAS}$ low pulse width	44	10000	57	10000	66	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low	82		99		116		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low	44		57		66		ns
tRCS	Read setup time before $\overline{CAS}$ low	0		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Note24)	32		42		44		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Note24)	77		92		107		ns
tAWD	Delay time, address to $\overline{W}$ low (Note24)	47		57		62		ns
tOEH	OE hold time after $\overline{W}$ low	15		20		20		ns

Note 23: t_{RWC} is specified as $t_{RWC(min)}=t_{RAC(max)}+t_{ODD(min)}+t_{RWL(min)}+t_{RP(min)}+4t_T$.

24: t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} and, t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS(min)}$ the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD(min)}$, $t_{RWD} \geq t_{RWD(min)}$, $t_{AWD} \geq t_{AWD(min)}$ and $t_{CPWD} \geq t_{CPWD(min)}$ (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to V_{IH}) is indeterminate.

Hyper page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle, , Read Write Mix Cycle, HI-Z control by $\overline{OE}$ or $\overline{W}$) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
		Min	Max	Min	Max	Min	Max	
t_{HPC}	Hyper page mode read/write cycle time	25		30		30		ns
t_{HPRWC}	Hyper Page Mode read write / read modify write cycle time	66		79		88		ns
t_{DOH}	Output hold time from $\overline{CAS}$ low	5		5		5		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read write cycle (Note26)	77	100000	92	100000	107	100000	ns
t_{CP}	$\overline{CAS}$ high pulse width (Note27)	10	18	13	18	13	18	ns
t_{CPRH}	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge	35		40		40		ns
t_{CPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	52		62		62		ns
t_{CHOL}	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
t_{OEPE}	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{WPE}	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
t_{HCWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	32		42		52		ns
t_{HAWD}	Delay time, Address to $\overline{W}$ low after read	62		72		82		ns
t_{HPWD}	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	72		82		92		ns
t_{HCOD}	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	15		20		20		ns
t_{HAOD}	Delay time, Address to $\overline{OE}$ high after read	30		35		35		ns
t_{HPOD}	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	35		40		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26: $t_{RAS(min)}$ is specified as two cycles of $\overline{CAS}$ input are performed.

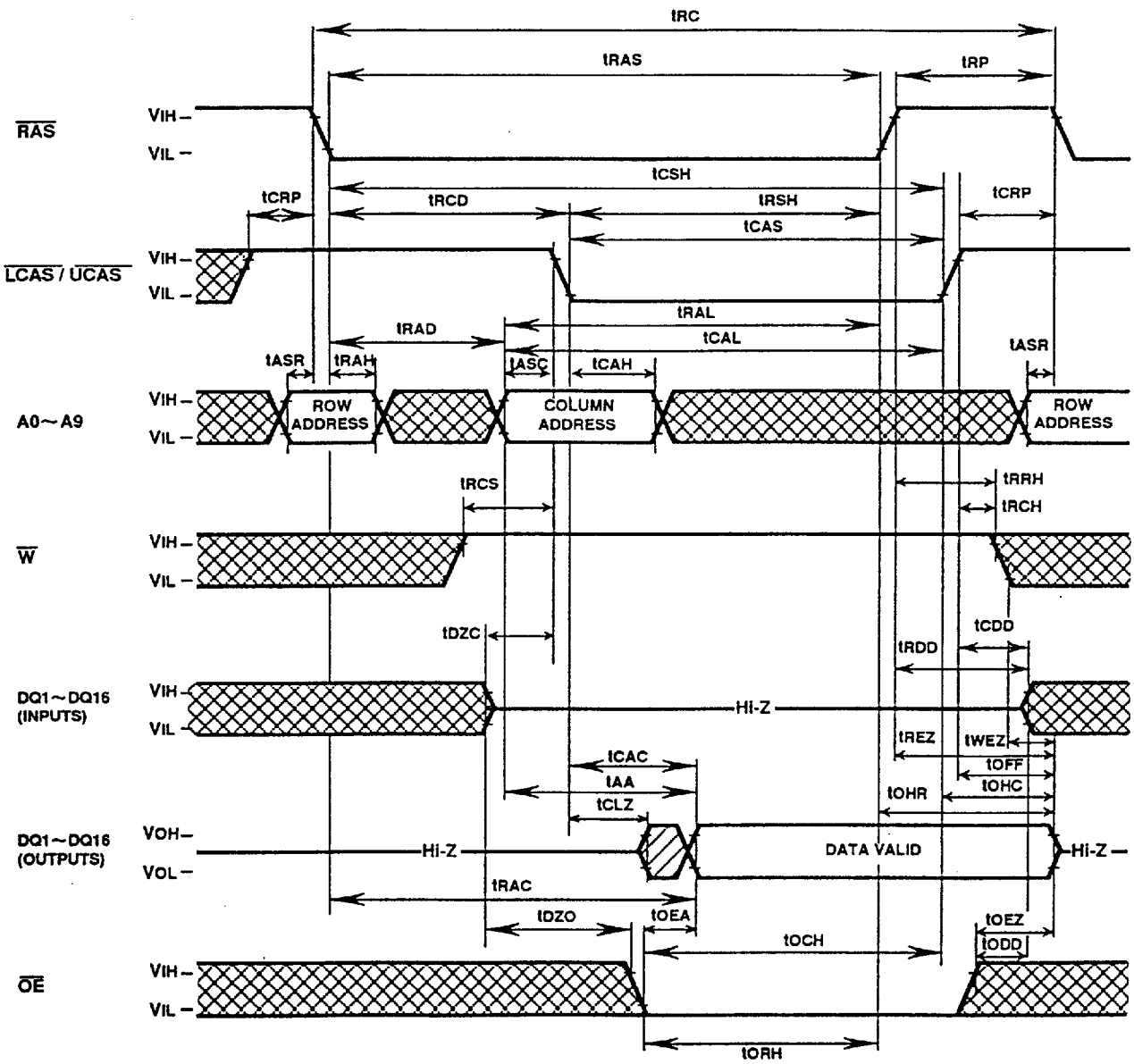
27: $t_{CP(max)}$ is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

Symbol	Parameter	Limits						Unit
		M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns

Note 28: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 29)
Read Cycle

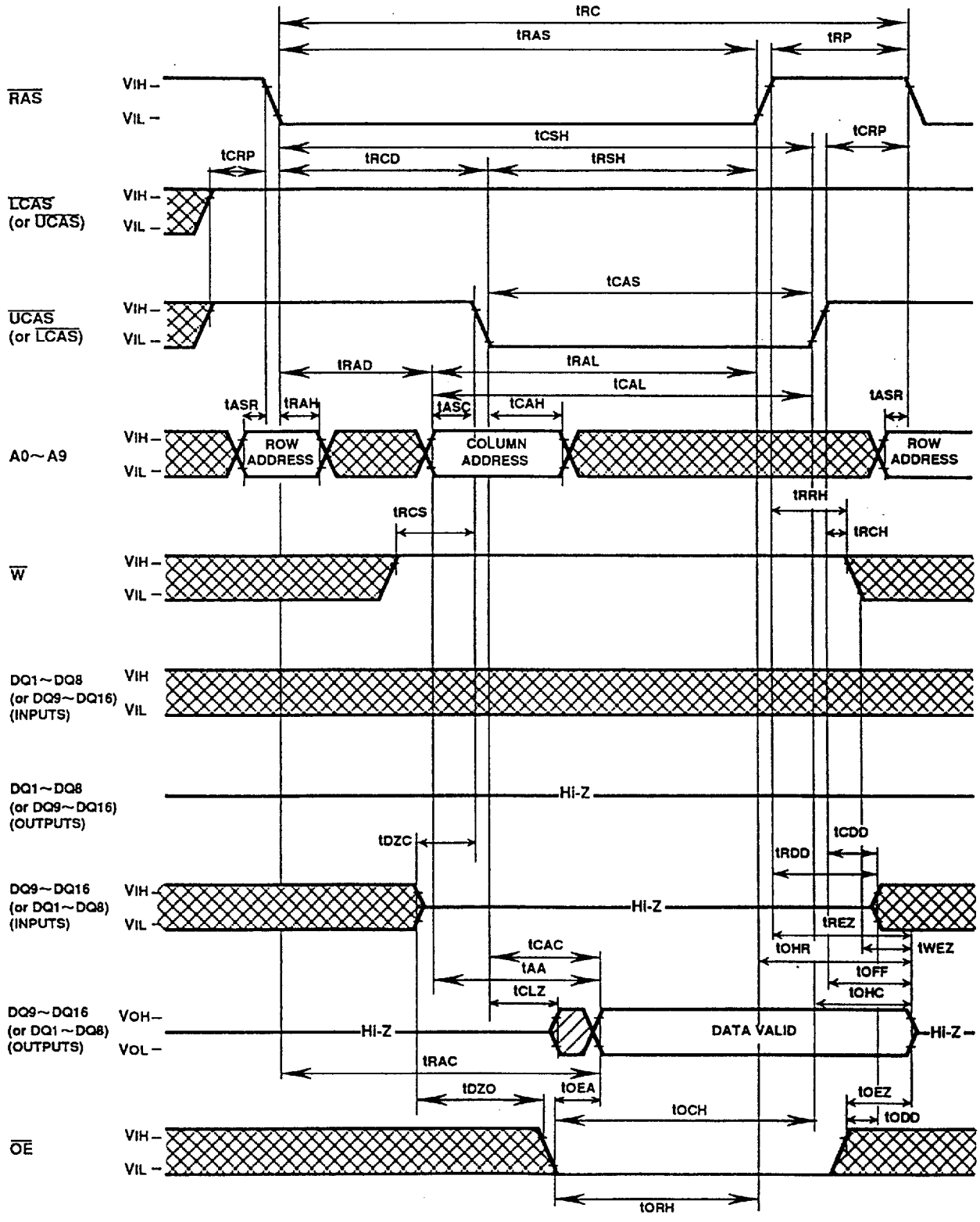


Note 29

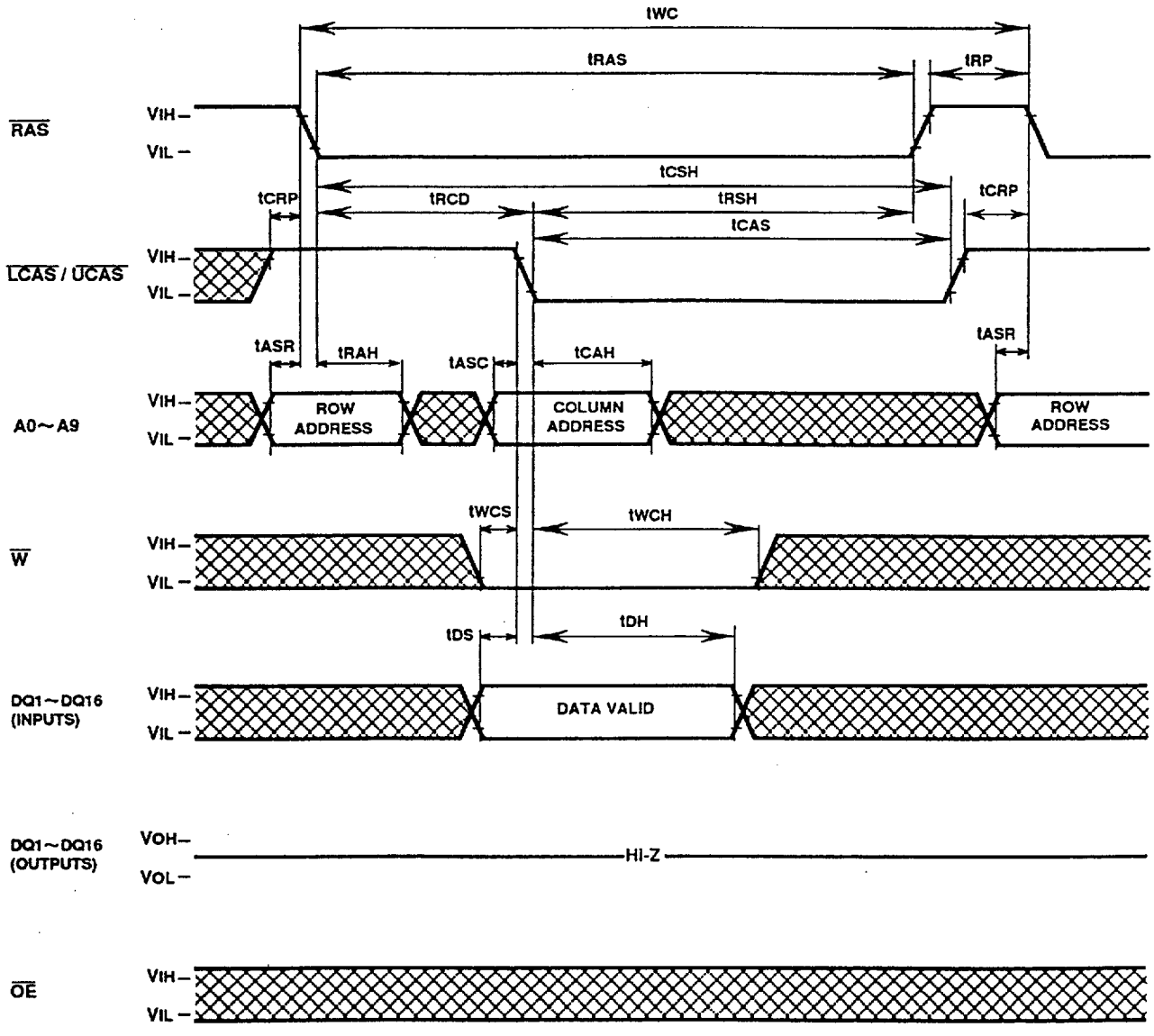
Indicates the don't care input.
$V_{IH(min)} \leqq V_{IN} \leqq V_{IH(max)}$ or $V_{IL(min)} \leqq V_{IN} \leqq V_{IL(max)}$

Indicates the invalid output.

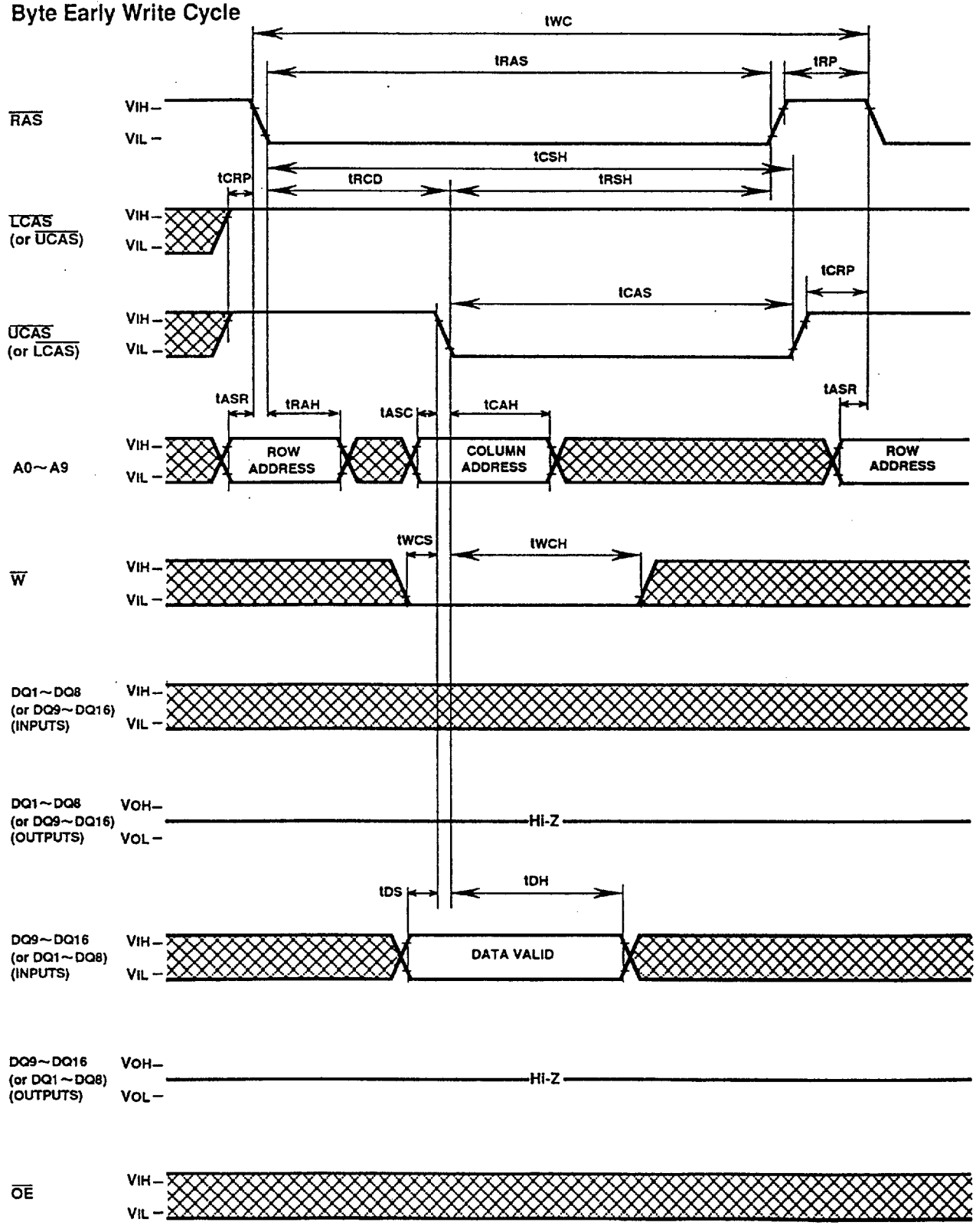
Byte Read Cycle



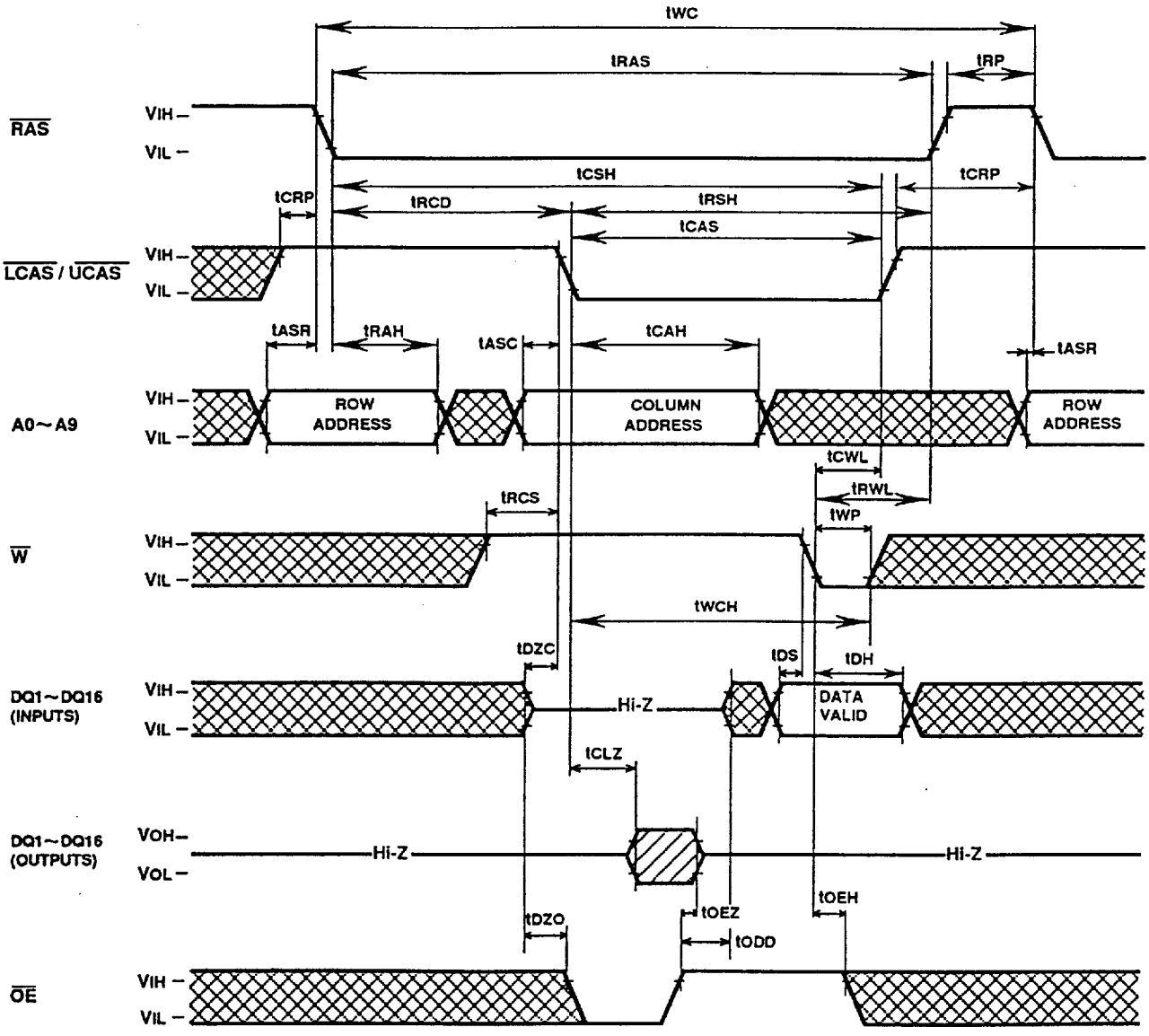
Early Write Cycle



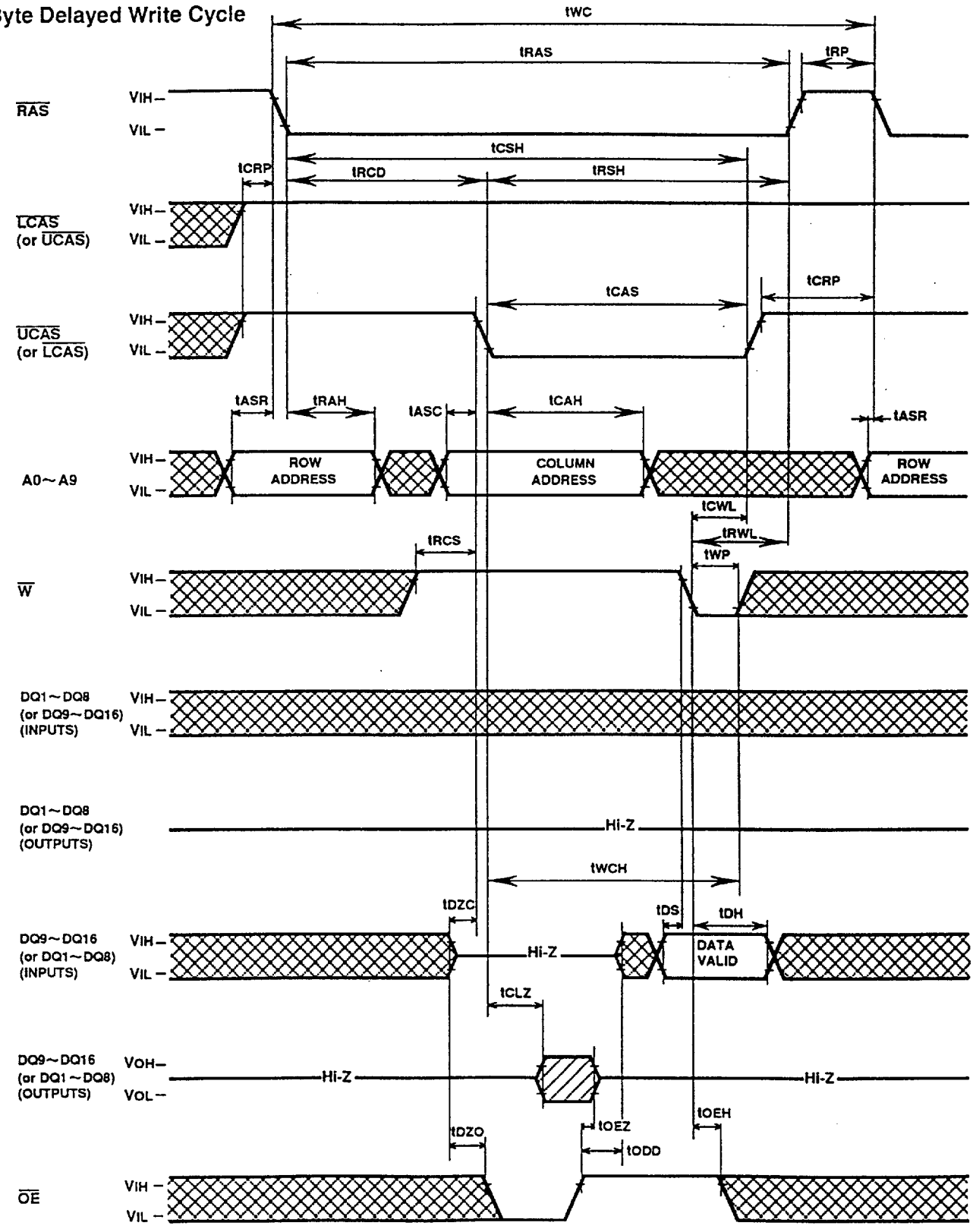
Byte Early Write Cycle



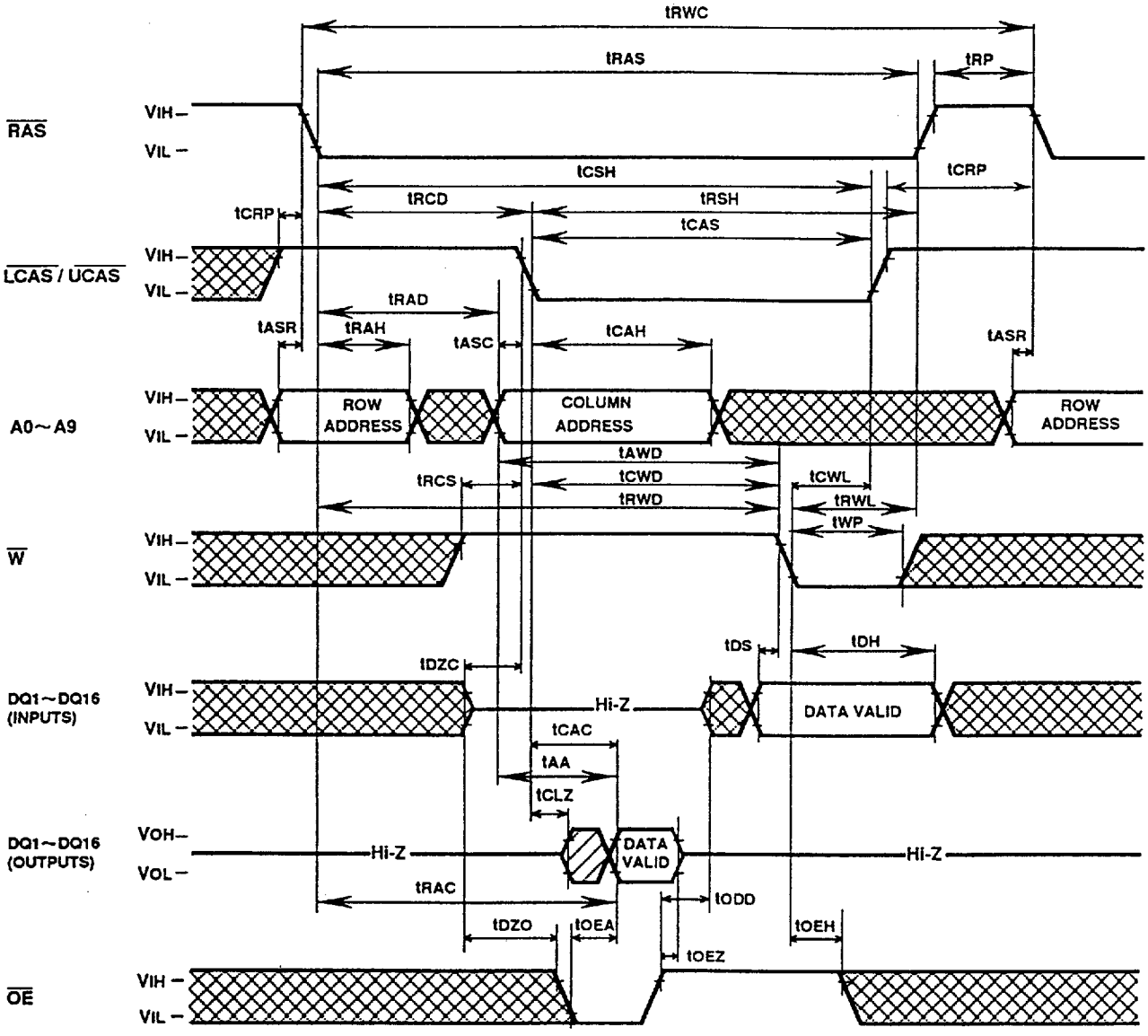
Delayed Write Cycle



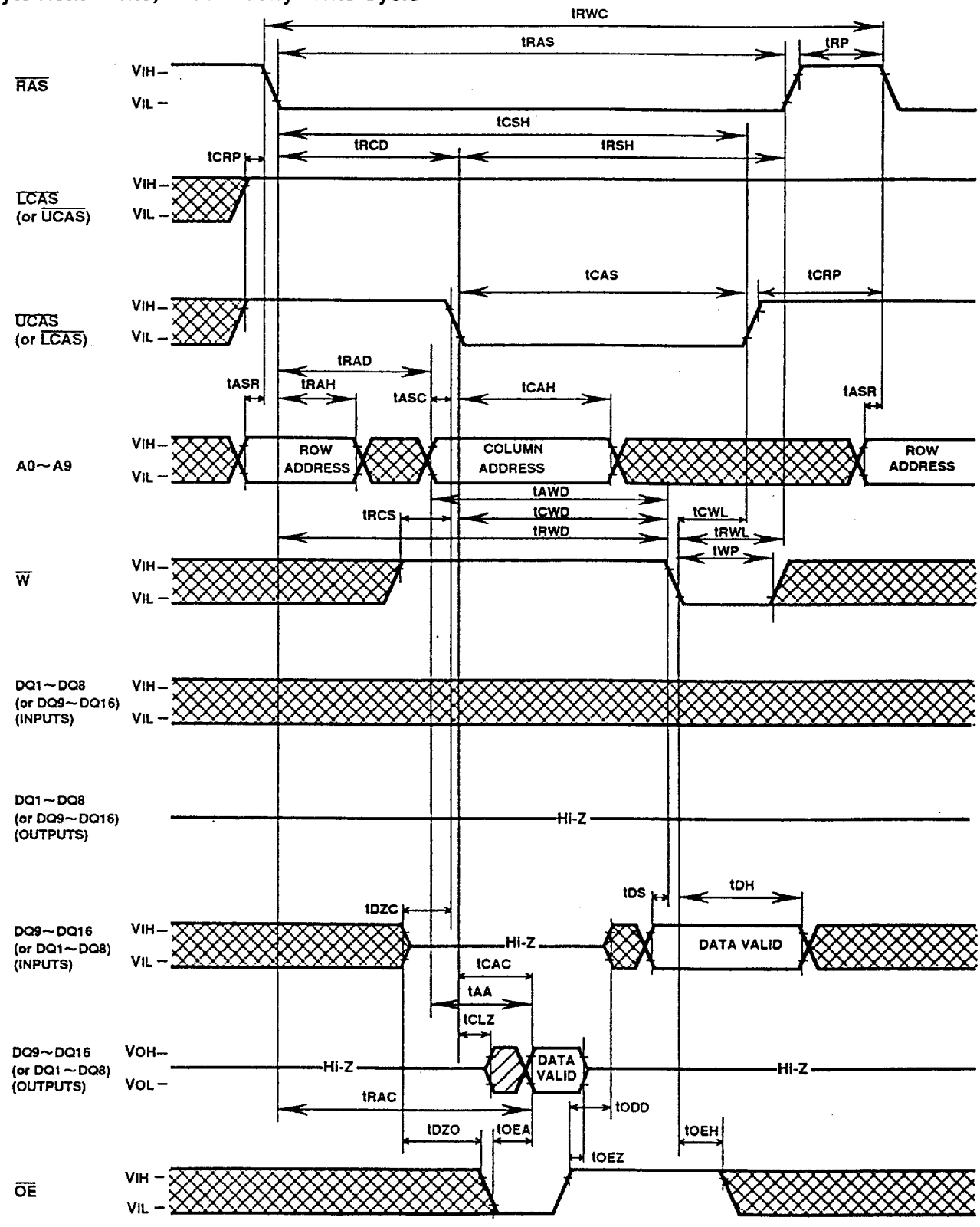
Byte Delayed Write Cycle



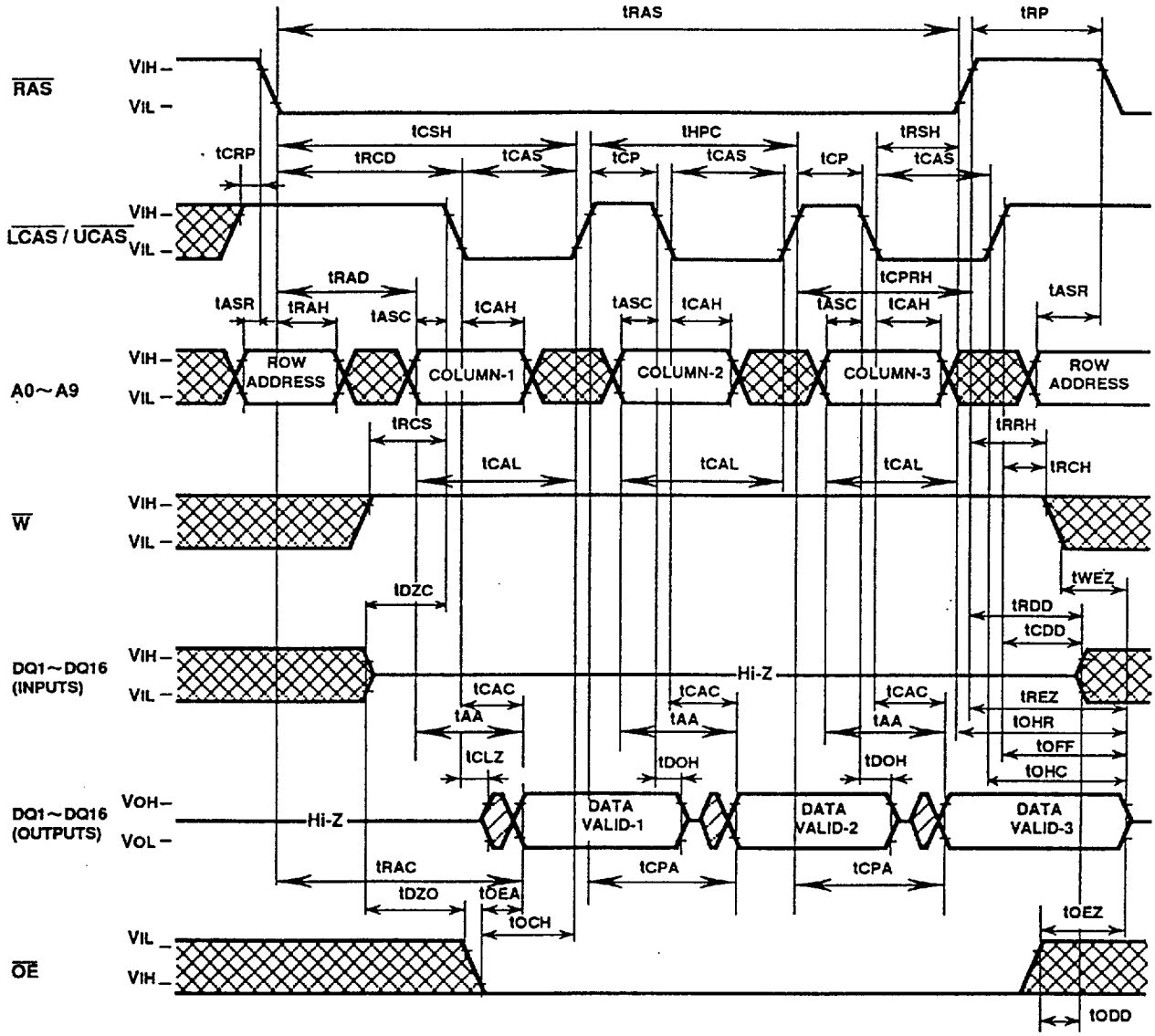
Read-Write, Read-Modify-Write Cycle



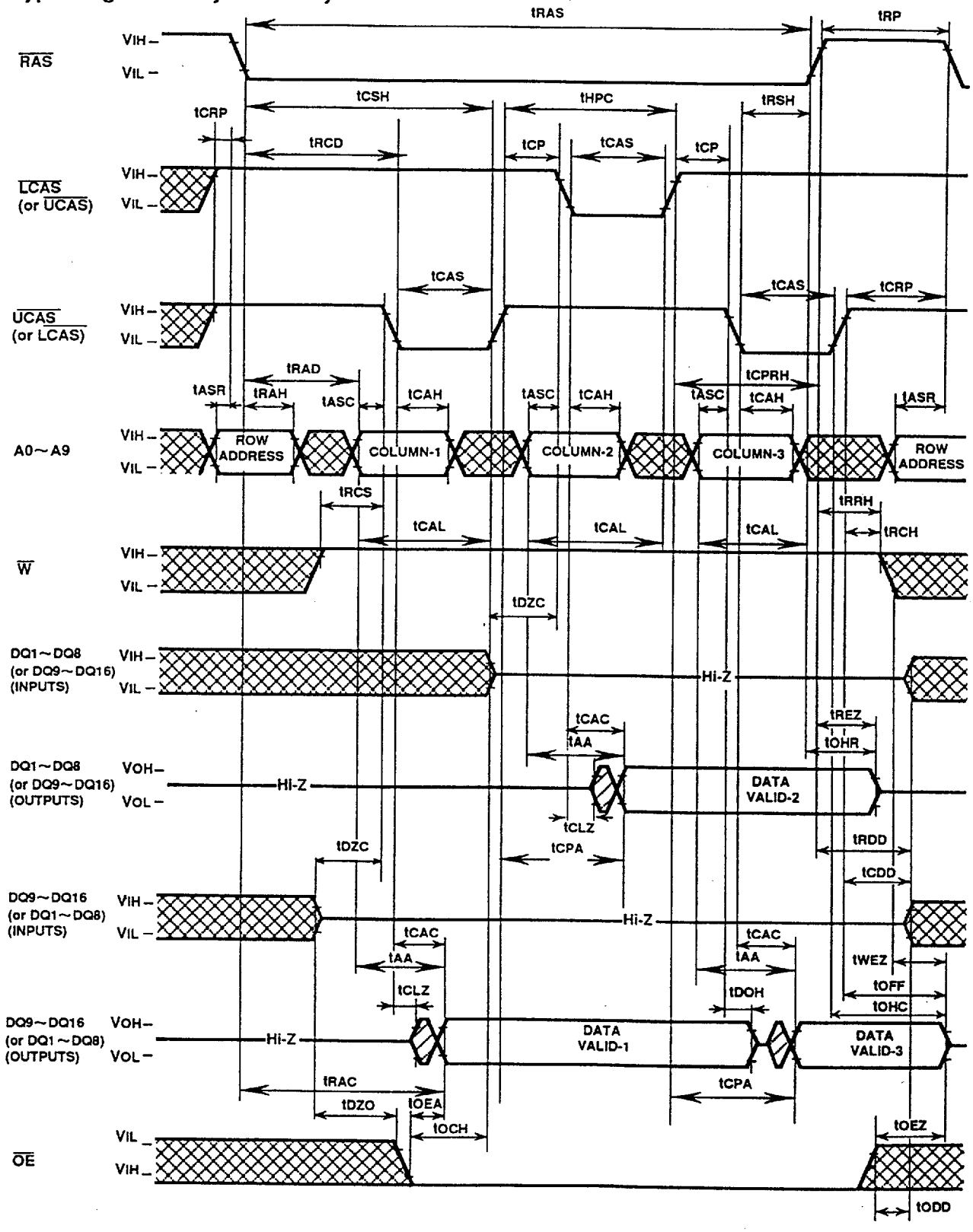
Byte Read-Write, Read-Modify-Write Cycle



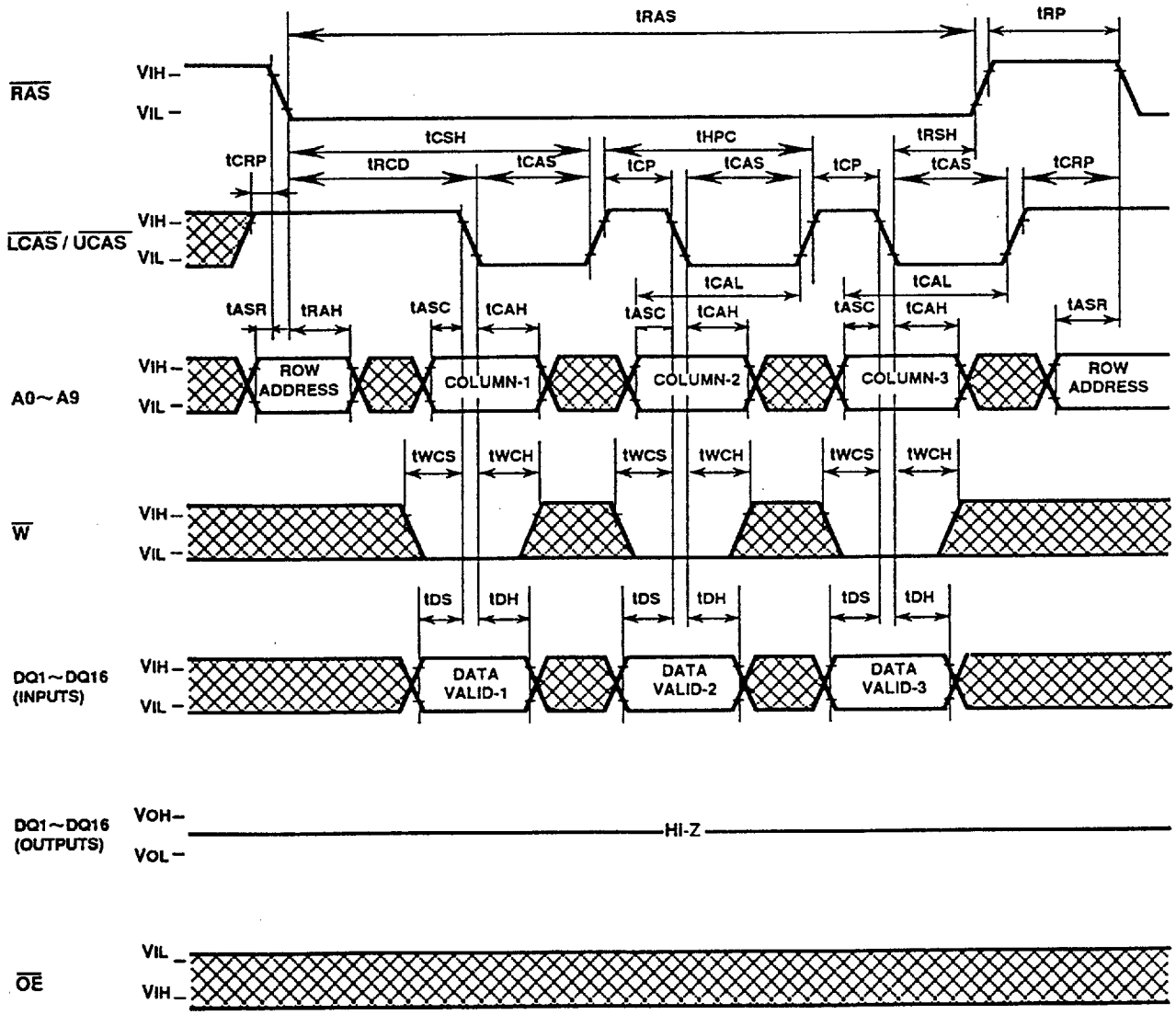
Hyper Page Mode Read Cycle



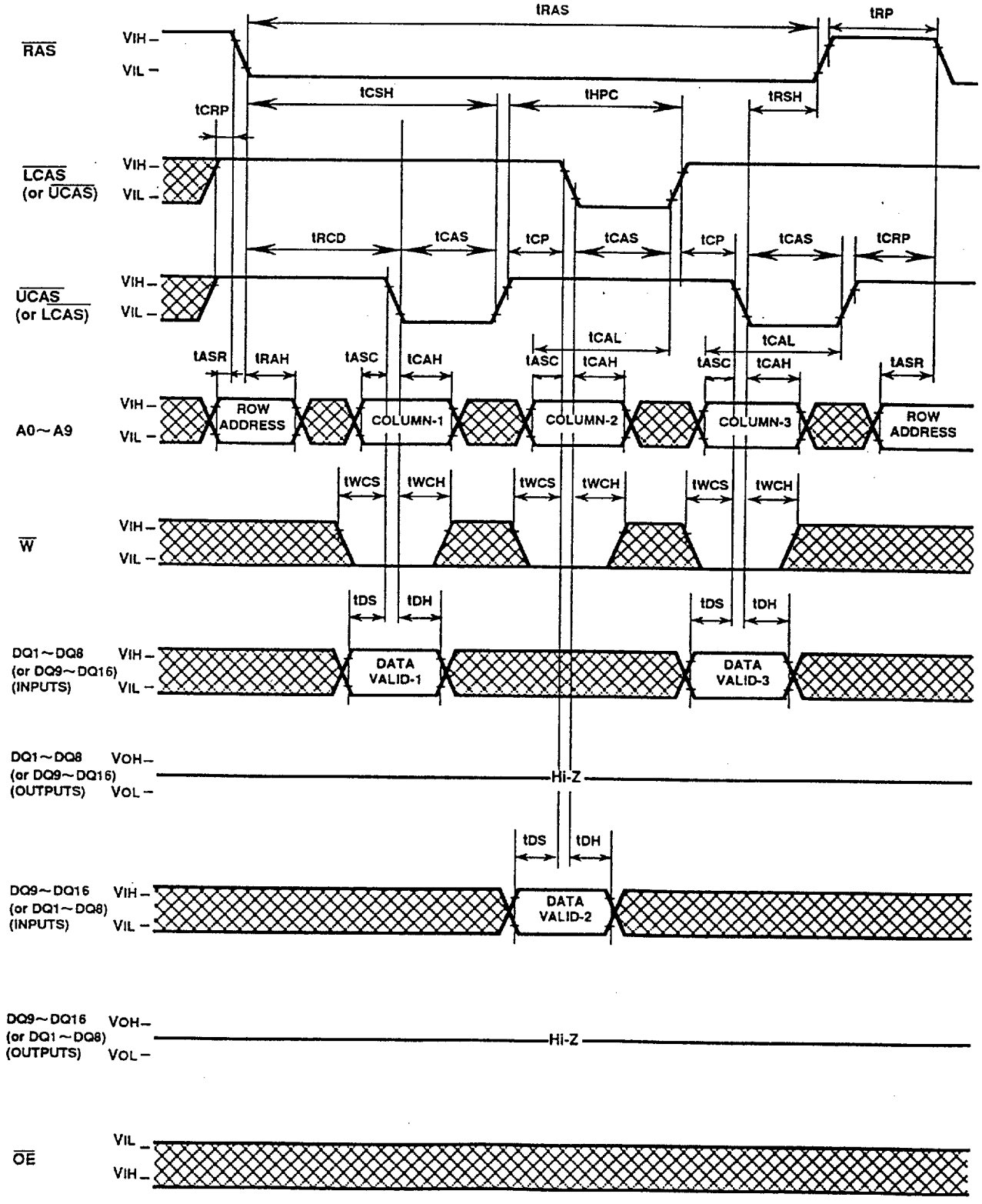
Hyper Page Mode Byte Read Cycle



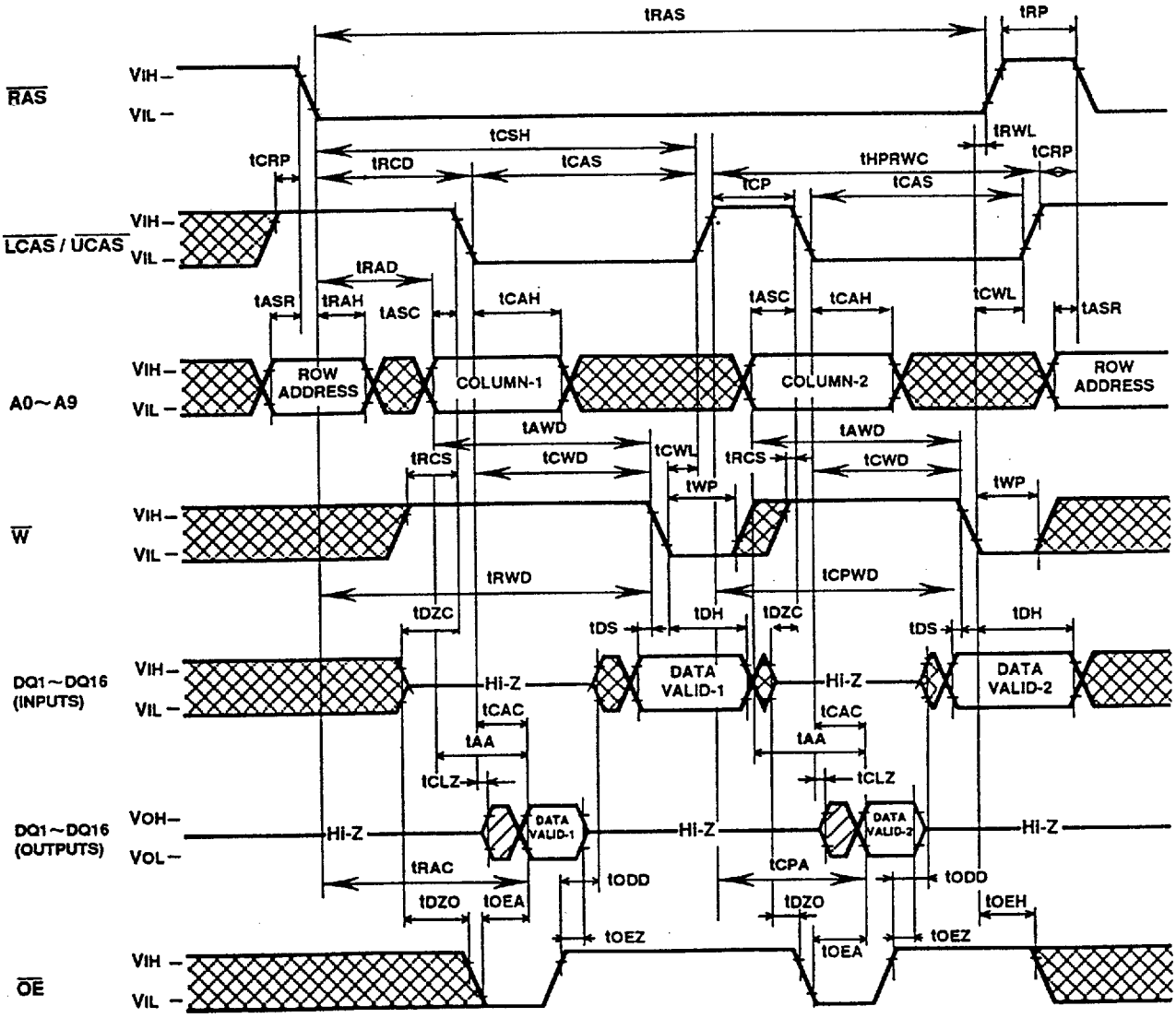
Hyper Page Mode Early Write Cycle



Hyper Page Mode Byte Early Write Cycle



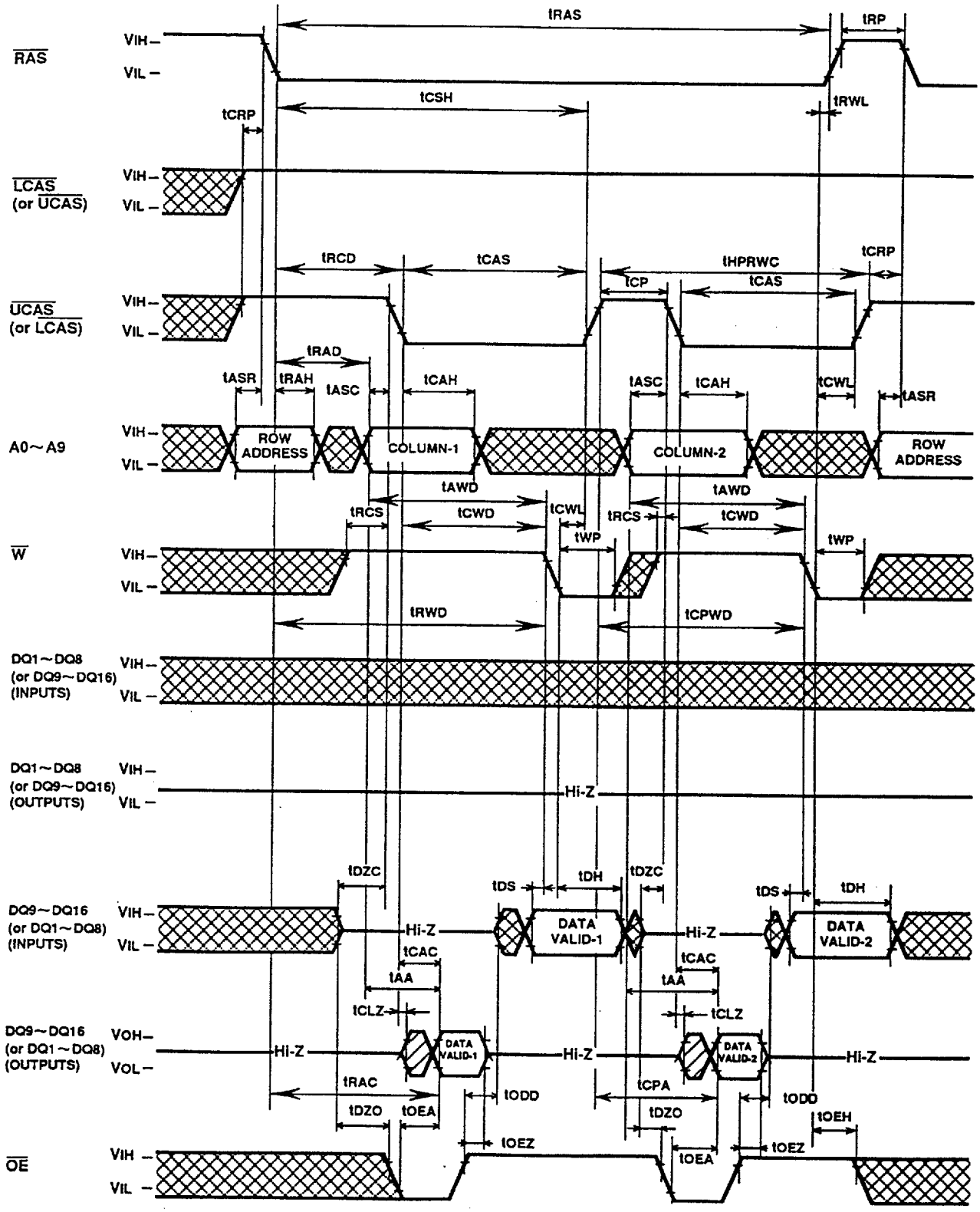
Hyper Page Mode Read-Write,Read-Modify-Write Cycle



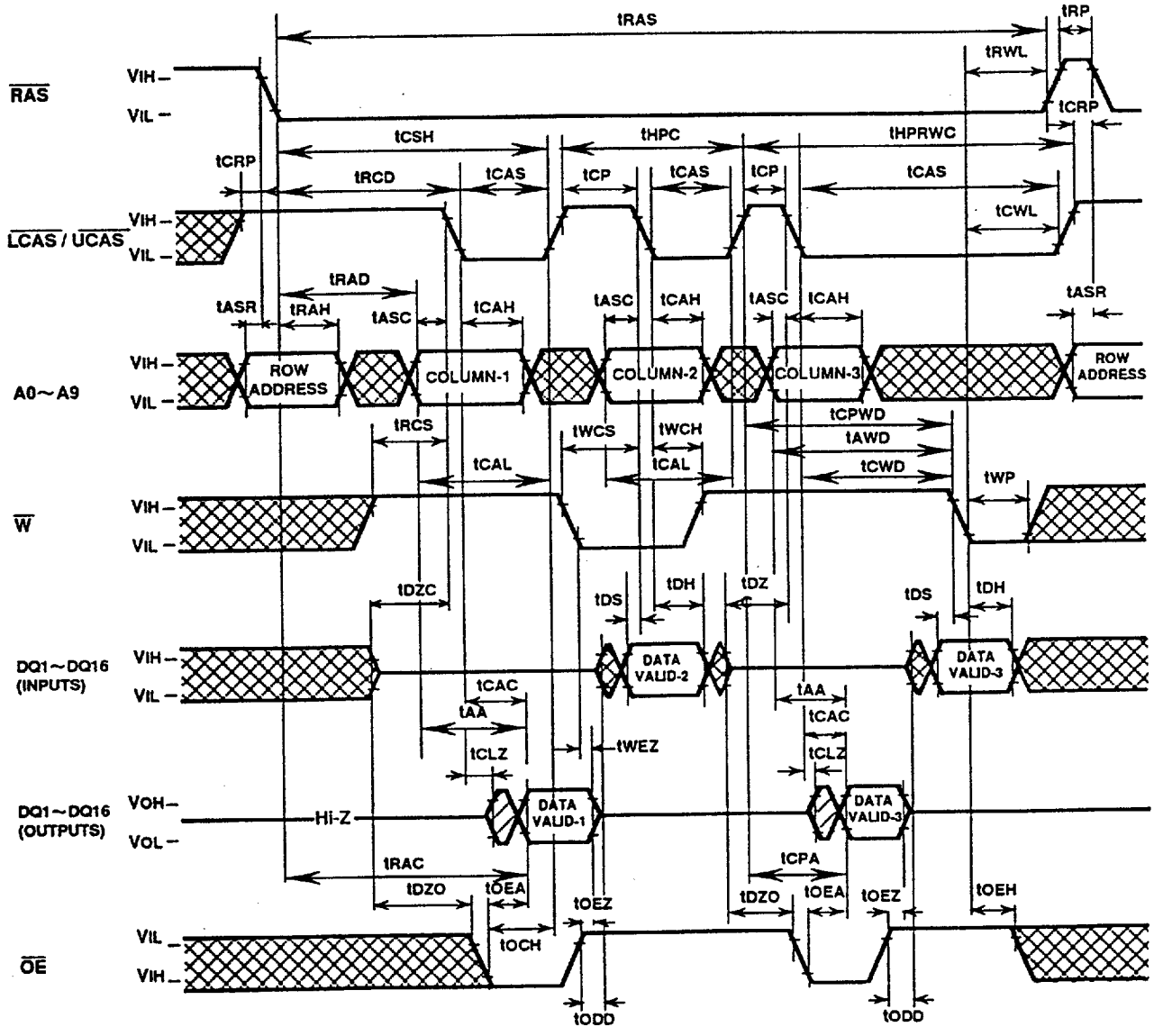
M5M418165BJ,TP-5,-6,-7,-5S,-6S,-7S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

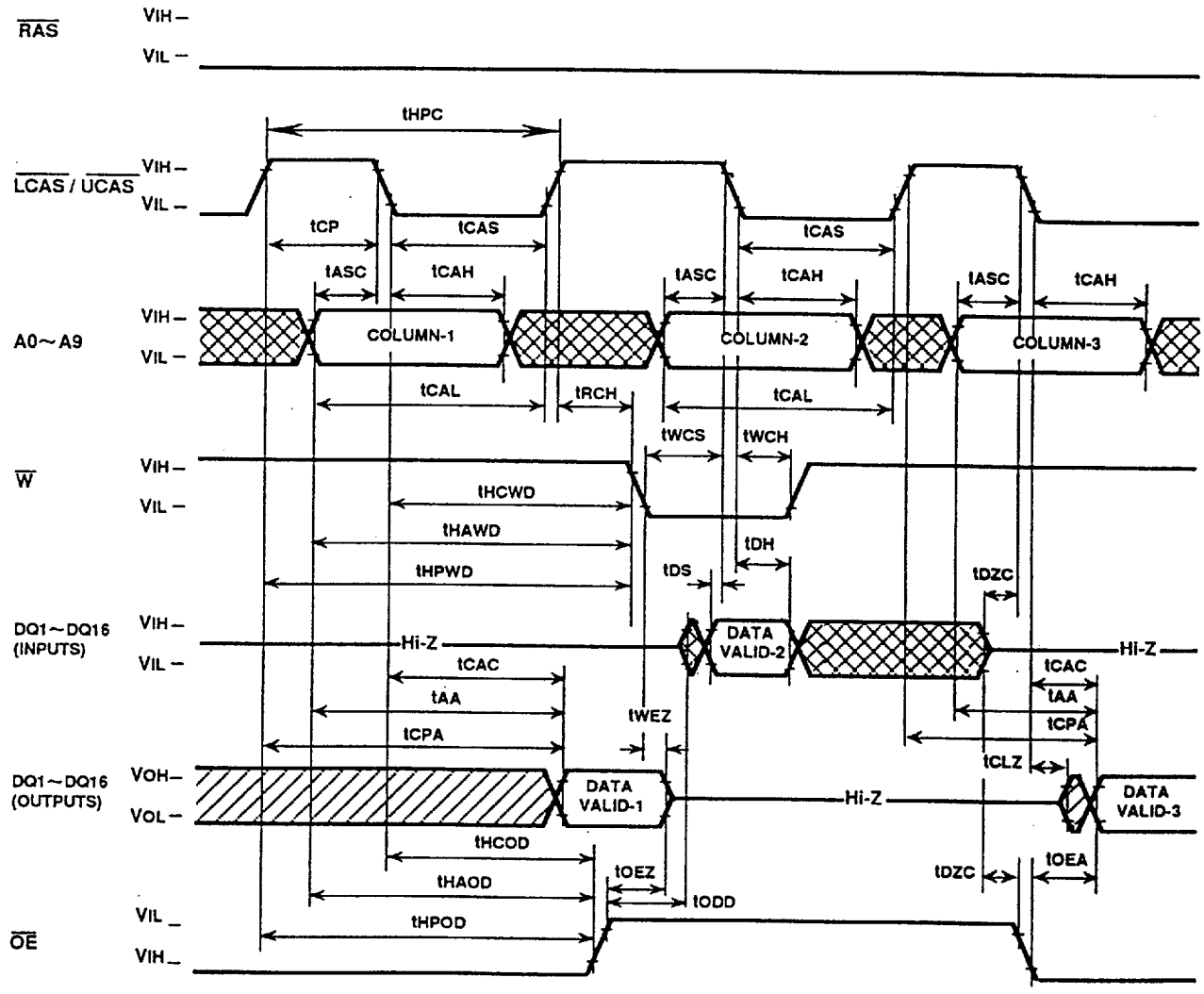
Hyper Page Mode Byte Read-Write,Read-Modify-Write Cycle



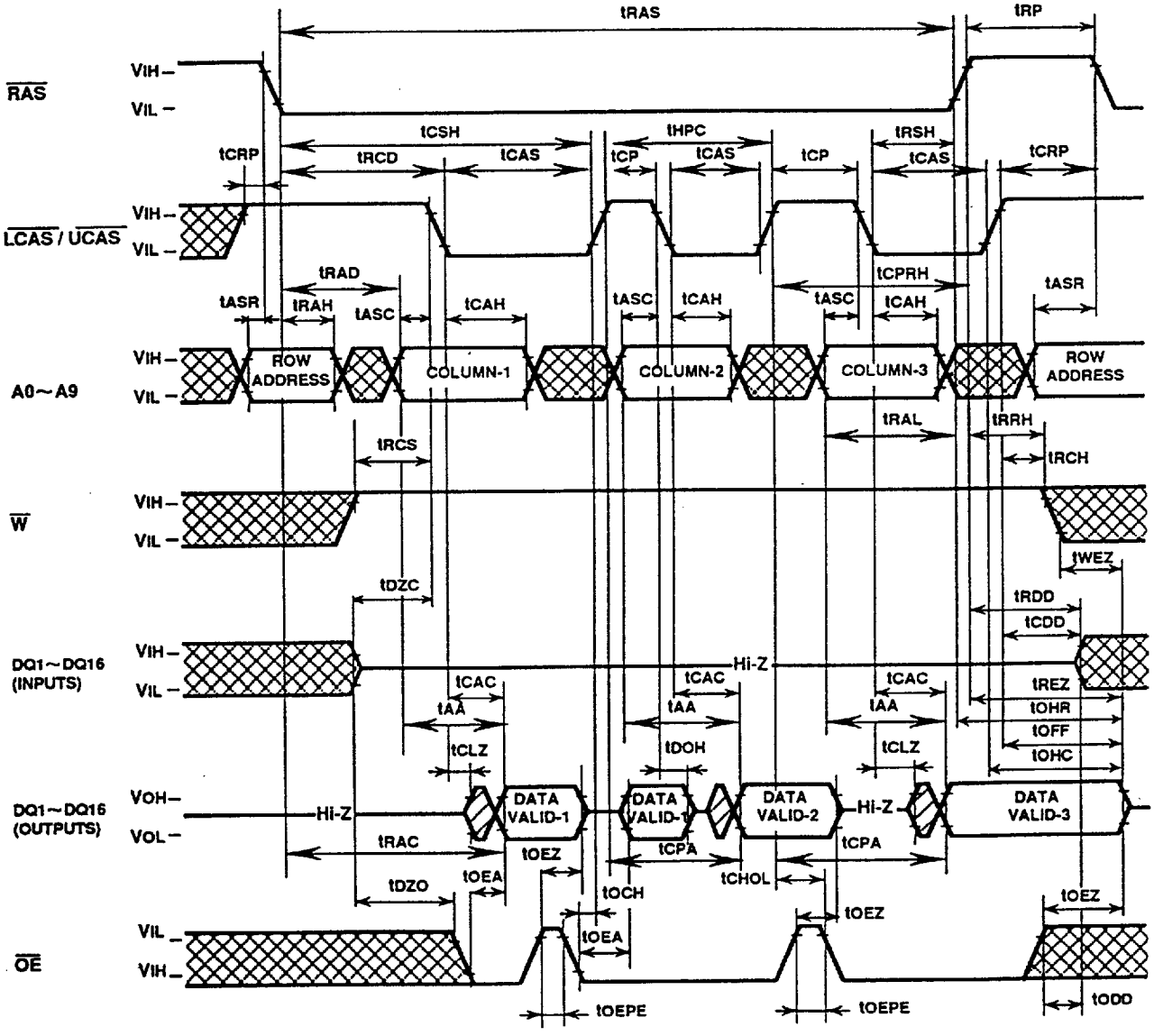
Hyper Page Mode Mix Cycle (1)



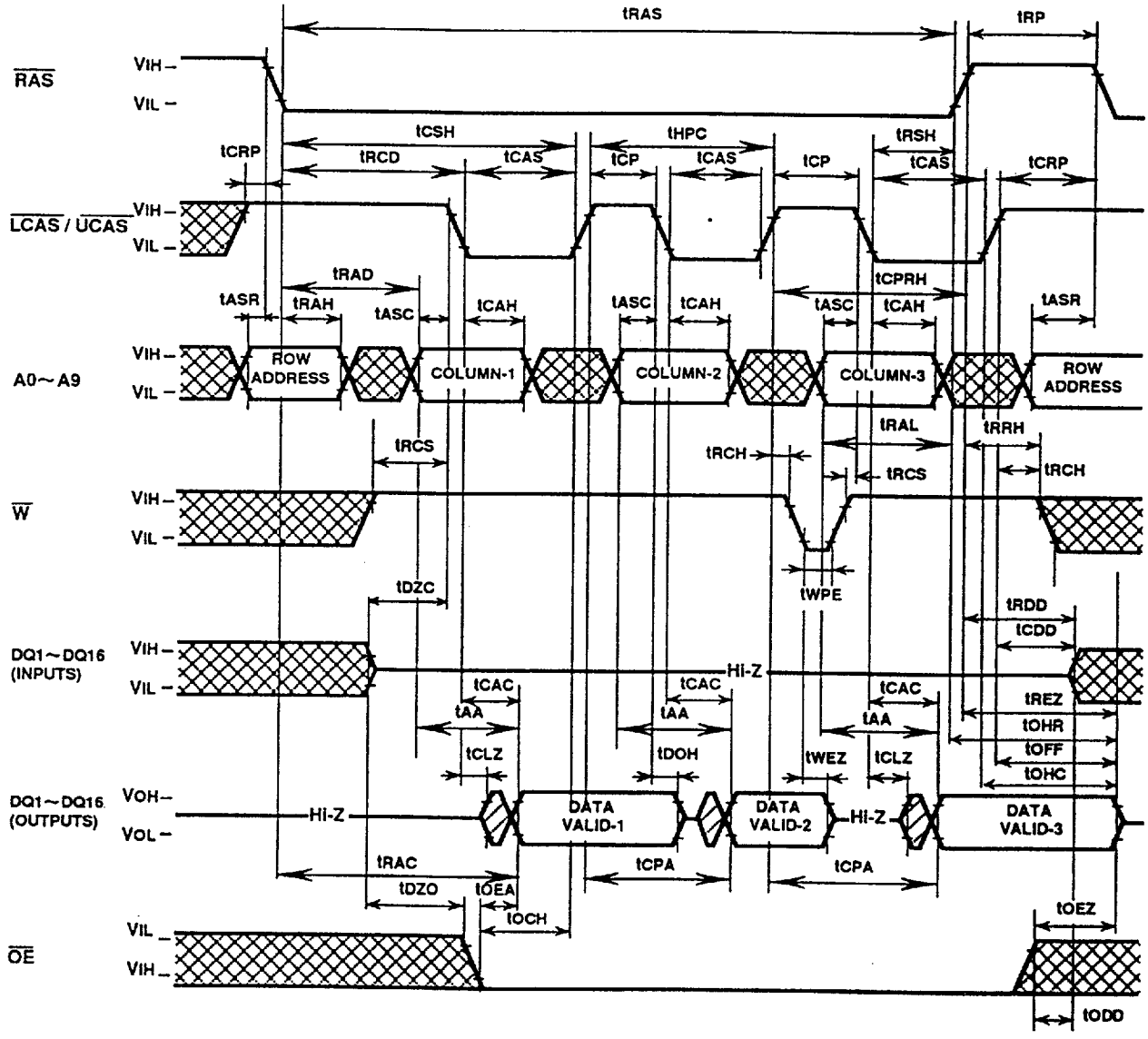
Hyper Page Mode Mix Cycle (2)



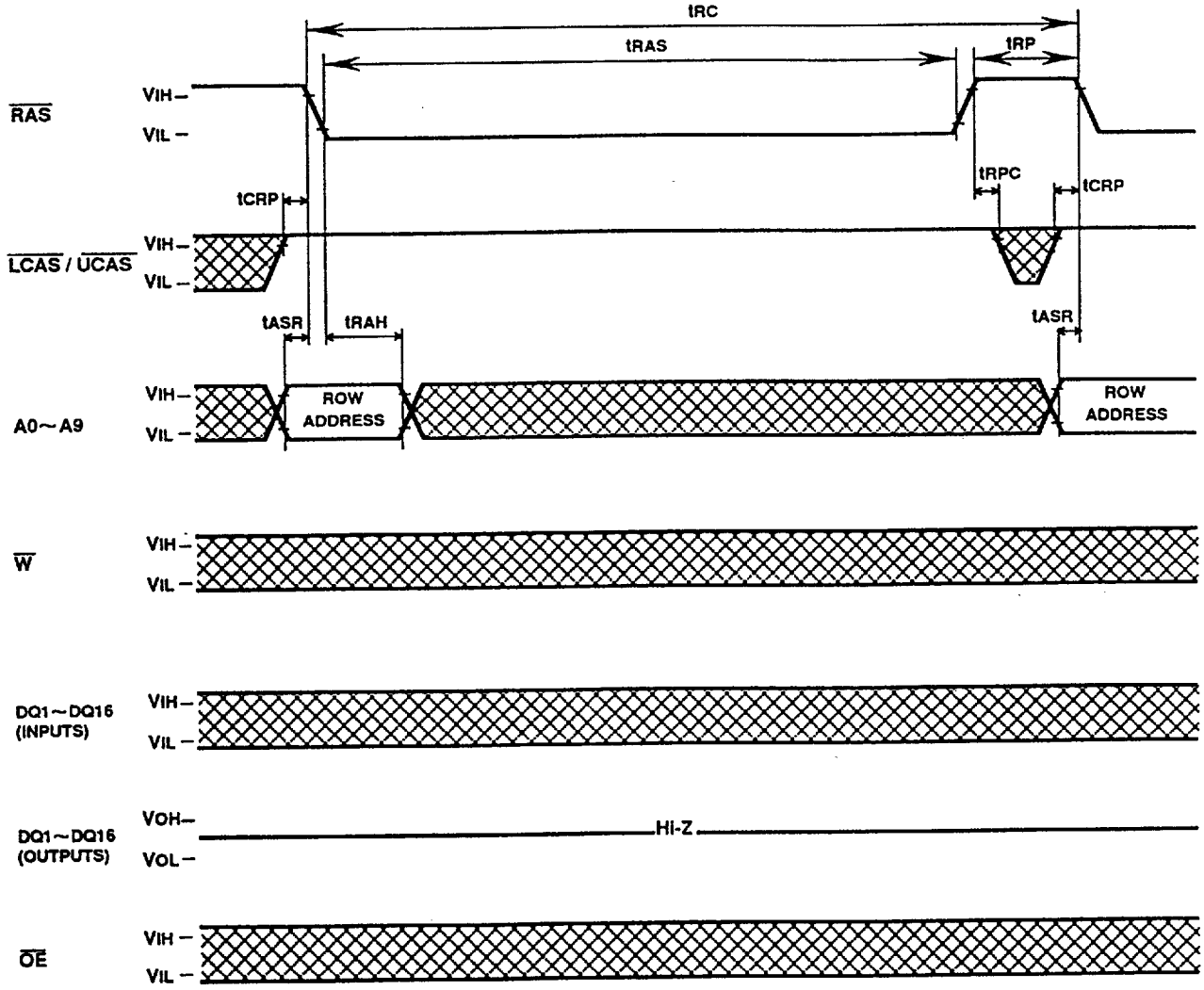
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{OE}$)



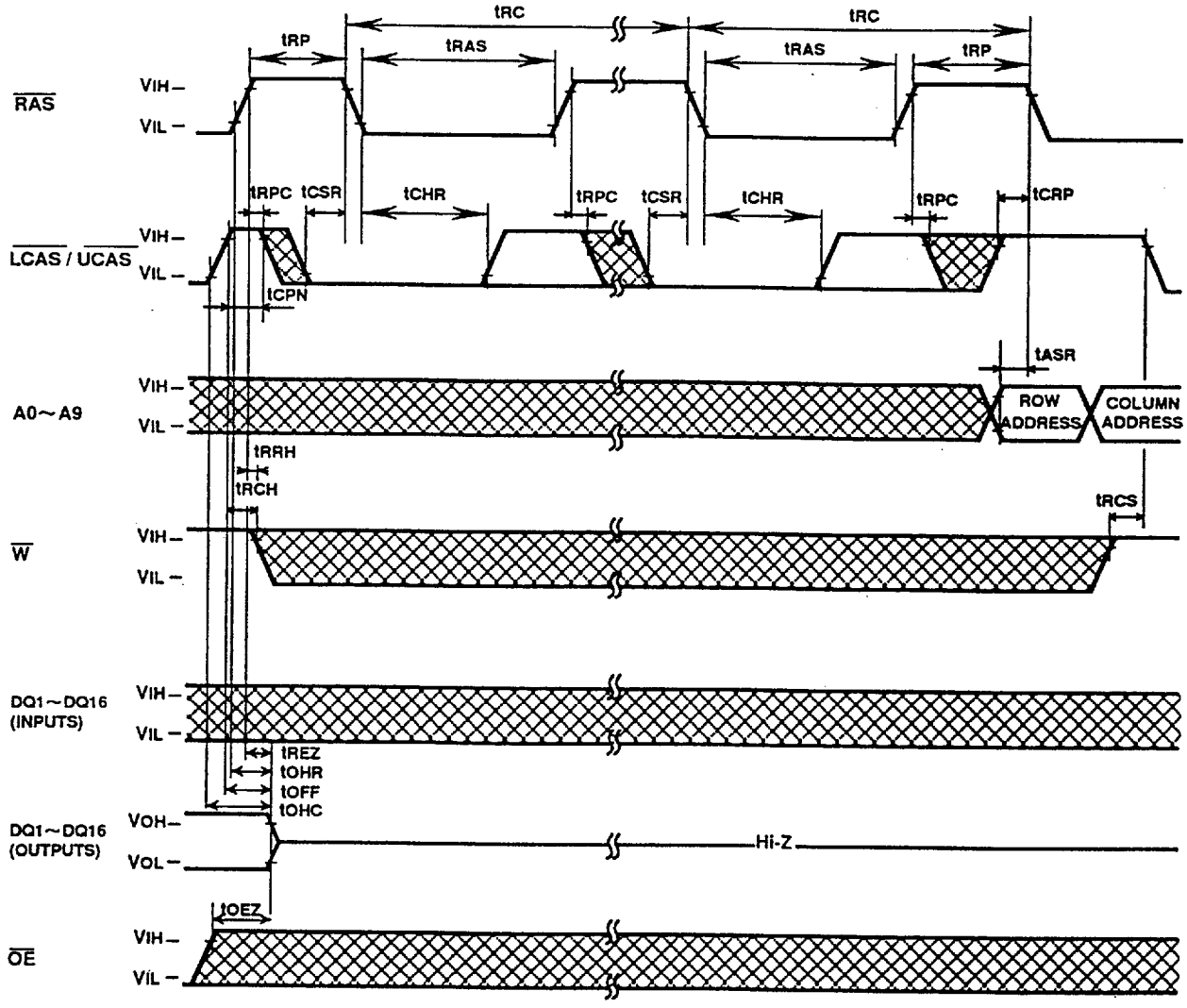
Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$)



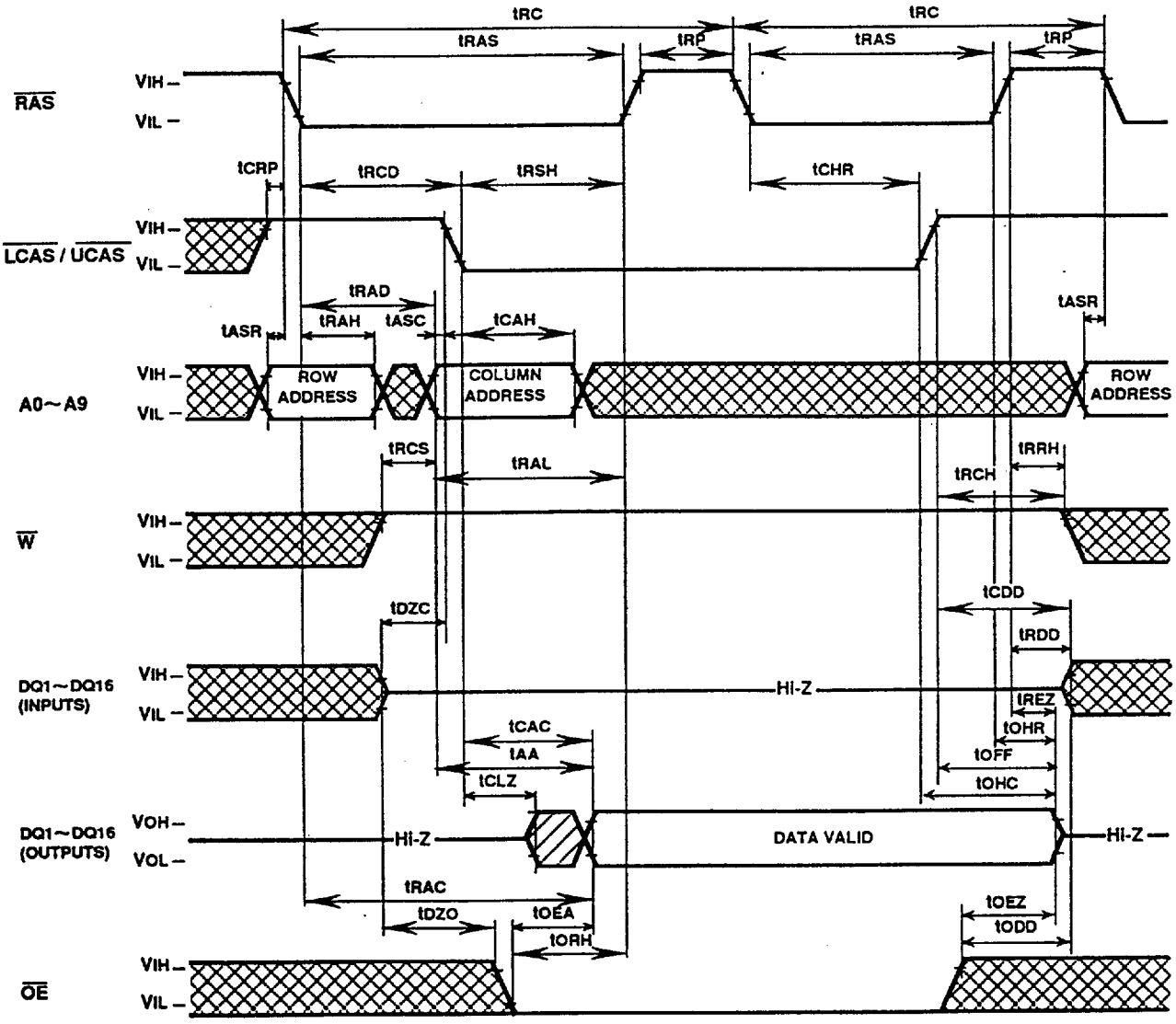
$\overline{RAS}$-only Refresh Cycle



$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle*

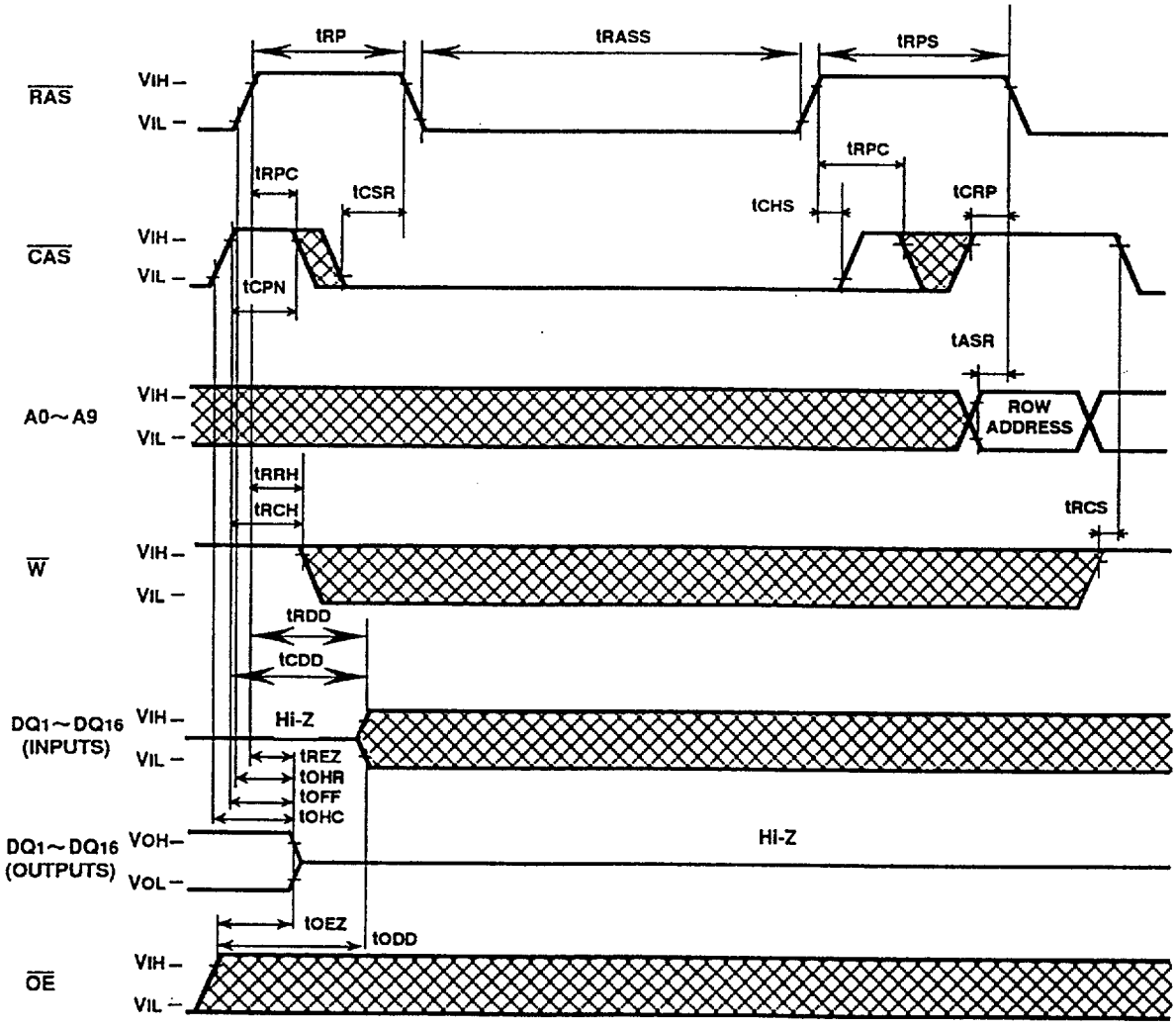


Hidden Refresh Cycle (Read) (Note 30)



Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

Self Refresh Cycle* (31)



SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S / -8S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
I_{CC2}	Supply current from Vcc, stand-by	M5M418165B (S)	$\overline{RAS}$ = $\overline{CAS}$ ≧ Vcc-0.2V			300	μA
$I_{CC8\ (AV)}$	Average supply current from Vcc Self - Refresh cycle	M5M418165B (S)	$\overline{RAS}$ = $\overline{CAS}$ ≦ 0.2V			400	μA

TIMING REQUIREMENTS (Ta=0 ~ 70°C, Vcc=5.0V ± 10%, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M418165B-6S		M5M418165B-7S		M5M418165B-8S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	110		130		150		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	- 50		- 50		- 50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS ≦ 16.4 ms and tSN ≦ 16.4 ms.

(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within tNS / tSN before / after self refresh, on the condition of tNS + tSN ≦ 16.4 ms.