SM72501

SM72501 SolarMagic Precision, CMOS Input, RRIO, Wide Supply Range Amplifier

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National Semiconductor

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General Description

The SM72501 is a low offset voltage, rail-to-rail input and output precision amplifier with a CMOS input stage and a wide supply voltage range. The SM72501 is ideal for sensor interface and other instrumentation applications.

The guaranteed low offset voltage of less than ±200 μV along with the guaranteed low input bias current of less than ±1 pA makes the SM72501 ideal for precision applications. The SM72501 is built utilizing VIP50 technology, which allows the combination of a CMOS input stage and a 12V common mode and supply voltage range. This makes the SM72501 a great choice in many applications where conventional CMOS parts cannot operate under the desired voltage conditions.

The SM72501 has a rail-to-rail input stage that significantly reduces the CMRR glitch commonly associated with rail-to-rail input amplifiers. This is achieved by trimming both sides of the complimentary input stage, thereby reducing the difference between the NMOS and PMOS offsets. The output of the SM72501 swings within 40 mV of either rail to maximize the signal dynamic range in applications requiring low supply voltage.

The SM72501 is offered in the space saving 5-Pin SOT23. This small package is an ideal solution for area constrained PC boards and portable electronics.

Features

- Renewable Energy Grade

Unless otherwise noted, typical values at $V_S = 5V$

■ Input offset voltage	±200 μV (max)
■ Input bias current	±200 fA
■ Input voltage noise	9 nV/√Hz
■ CMRR	130 dB
■ Open loop gain	130 dB
■ Temperature range	−40°C to 125°C
■ Unity gain bandwidth	2.5 MHz
■ Supply current (SM72501)	715 μA
■ Supply voltage range	2.7V to 12V
■ Rail-to-rail input and output	

Applications

- High impedance sensor interface
- Battery powered instrumentation
- High gain amplifiers
- DAC buffer
- Instrumentation amplifier
- Active filters

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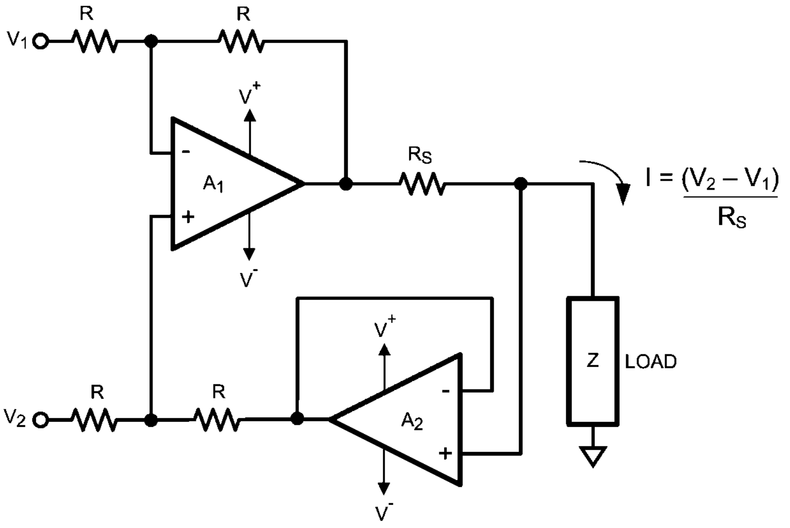
Typical Application



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Precision Current Source

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Charge-Device Model	1000V
V_{IN} Differential	±300 mV
Supply Voltage ($V_S = V^+ - V^-$)	13.2V
Voltage at Input/Output Pins	$V^+ + 0.3V$, $V^- - 0.3V$
Input Current	10 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40°C to +125°C
Supply Voltage ($V_S = V^+ - V^-$)	2.7V to 12V
Package Thermal Resistance (θ_{JA} (Note 3))	
5-Pin SOT23	265°C/W

3V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for $T_A = 25°C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V^+/2$, and $R_L > 10\ k\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±37	±200 **±500**	μV
TCV_{OS}	Input Offset Voltage Temperature Drift	(Note 7)		±1	**±5**	μV/°C
I_B	Input Bias Current	(Note 7, Note 8) $-40°C \leq T_A \leq 85°C$		±0.2	±1 **±50**	pA
		(Note 7, Note 8) $-40°C \leq T_A \leq 125°C$		±0.2	±1 **±400**	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	$0V \leq V_{CM} \leq 3V$	86 **80**	130		dB
PSRR	Power Supply Rejection Ratio	$2.7V \leq V^+ \leq 12V$, $V_o = V^+/2$	86 **82**	98		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 77 dB	−0.2 **−0.2**		3.2 **3.2**	V
A_{VOL}	Open Loop Voltage Gain	$R_L = 2\ k\Omega$ $V_O = 0.3V$ to $2.7V$	100 **96**	114		dB
		$R_L = 10\ k\Omega$ $V_O = 0.2V$ to $2.8V$	100 **96**	124		
V_{OUT}	Output Voltage Swing High	$R_L = 2\ k\Omega$ to $V^+/2$		40	80 **120**	mV from V+
		$R_L = 10\ k\Omega$ to $V^+/2$		30	40 **60**	
	Output Voltage Swing Low	$R_L = 2\ k\Omega$ to $V^+/2$		40	60 **80**	mV
		$R_L = 10\ k\Omega$ to $V^+/2$		20	40 **50**	
I_{OUT}	Output Current (Note 3, Note 9)	Sourcing $V_O = V^+/2$ $V_{IN} = 100$ mV	25 **15**	42		mA
		Sinking $V_O = V^+/2$ $V_{IN} = -100$ mV	25 **20**	42		
I_S	Supply Current			0.670	1.0 **1.2**	mA
SR	Slew Rate (Note 10)	$A_V = +1$, $V_O = 2\ V_{PP}$ 10% to 90%		0.9		V/μs

Symbol	Parameter	Conditions	Min (*Note 6*)	Typ (*Note 5*)	Max (*Note 6*)	Units
GBW	Gain Bandwidth			2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, $A_V = 1$, $R._L = 10$ kΩ		0.02		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		$\text{nV}/\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise Density	f = 100 kHz		1		$\text{fA}/\sqrt{\text{Hz}}$

5V Electrical Characteristics (*Note 4*)

Unless otherwise specified, all limits are guaranteed for $T_A = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V^+/2$, and $R_L > 10$ kΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (*Note 6*)	Typ (*Note 5*)	Max (*Note 6*)	Units
V_{OS}	Input Offset Voltage			±37	±200 **±500**	μV
TCV_{OS}	Input Offset Voltage Temperature Drift	(*Note 7*)		±1	**±5**	μV/°C
I_B	Input Bias Current	(*Note 7*, *Note 8*) $-40°C \le T_A \le 85°C$		±0.2	±1 **±50**	pA
		(*Note 7*, *Note 8*) $-40°C \le T_A \le 125°C$		±0.2	±1 **±400**	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 5V$	88 **83**	130		dB
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 12V$, $V_O = V^+/2$	86 **82**	100		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	–0.2 **–0.2**		5.2 **5.2**	V
A_{VOL}	Open Loop Voltage Gain	$R_L = 2$ kΩ $V_O = 0.3V$ to $4.7V$	100 **96**	119		dB
		$R_L = 10$ kΩ $V_O = 0.2V$ to $4.8V$	100 **96**	130		
V_{OUT}	Output Voltage Swing High	$R_L = 2$ kΩ to $V^+/2$		60	110 **130**	mV from V^+
		$R_L = 10$ kΩ to $V^+/2$		40	50 **70**	
	Output Voltage Swing Low	$R_L = 2$ kΩ to $V^+/2$		50	80 **90**	mV
		$R_L = 10$ kΩ to $V^+/2$		30	40 **50**	
I_{OUT}	Output Current (*Note 3*, *Note 9*)	Sourcing $V_O = V^+/2$ $V_{IN} = 100$ mV	40 **28**	66		mA
		Sinking $V_O = V^+/2$ $V_{IN} = -100$ mV	40 **28**	76		
I_S	Supply Current			0.715	1.0 **1.2**	mA
SR	Slew Rate (*Note 10*)	$A_V = +1$, $V_O = 4\ V_{PP}$ 10% to 90%		1.0		V/μs
GBW	Gain Bandwidth			2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, $A_V = 1$, $R_L = 10$ kΩ		0.02		%

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 100 kHz		1		$fA/\sqrt{Hz}$

±5V Electrical Characteristics (Note 4)

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 5V, V^- = –5V, V_{CM} = 0V, and R_L > 10 kΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			±37	±200 **±500**	μV
TCV_{OS}	Input Offset Voltage Temperature Drift	(Note 7)		±1	**±5**	μV/°C
I_B	Input Bias Current	(Note 7, Note 8) –40°C ≤ T_A ≤ 85°C		±0.2	1 **±50**	pA
		(Note 7, Note 8) –40°C ≤ T_A ≤ 125°C		±0.2	1 **±400**	
I_{OS}	Input Offset Current			40		fA
CMRR	Common Mode Rejection Ratio	–5V ≤ V_{CM} ≤ 5V	92 **88**	138		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 12V, V_O = 0V	86 **82**	98		dB
CMVR	Common Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB	–5.2 **–5.2**		5.2 **5.2**	V
A_{VOL}	Open Loop Voltage Gain	R_L = 2 kΩ V_O = –4.7V to 4.7V	100 **98**	121		dB
		R_L = 10 kΩ V_O = –4.8V to 4.8V	100 **98**	134		
V_{OUT}	Output Voltage Swing High	R_L = 2 kΩ to 0V		90	150 **170**	mV from V^+
		R_L = 10 kΩ to 0V		40	80 **100**	
	Output Voltage Swing Low	R_L = 2 kΩ to 0V		90	130 **150**	mV from V^-
		R_L = 10 kΩ to 0V		40	50 **60**	
I_{OUT}	Output Current (Note 3, Note 9)	Sourcing V_O = 0V V_{IN} = 100 mV	50 **35**	86		mA
		Sinking V_O = 0V V_{IN} = –100 mV	50 **35**	84		
I_S	Supply Current			0.790	1.1 **1.3**	mA
SR	Slew Rate (Note 10)	A_V = +1, V_O = 9 V_{PP} 10% to 90%		1.1		V/μs
GBW	Gain Bandwidth			2.5		MHz
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 1, R_L = 10 kΩ		0.02		%
e_n	Input Referred Voltage Noise Density	f = 1 kHz		9		$nV/\sqrt{Hz}$
i_n	Input Referred Current Noise Density	f = 100 kHz		1		$fA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

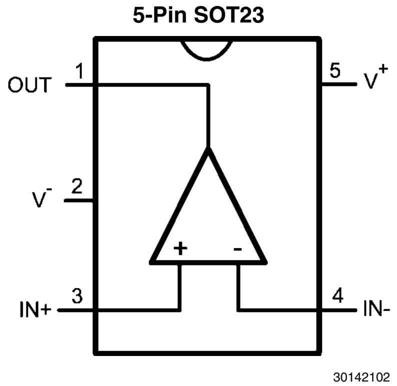
Note 7: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 8: Positive current corresponds to current flowing into the device.

Note 9: The short circuit test is a momentary test.

Note 10: The number specified is the slower of positive and negative slew rates.

Connection Diagram



Top View

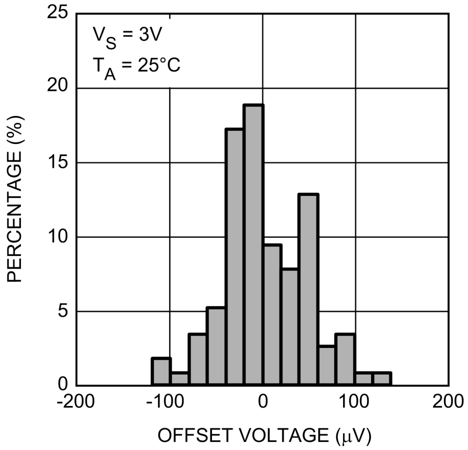
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT23	SM72501MFE	S501	250 Units Tape and Reel	MF05A
5-Pin SOT23	SM72501MF	S501	1000 Units Tape and Reel	MF05A
5-Pin SOT23	SM72501MFX	S501	3000 Units Tape and Reel	MF05A

Typical Performance Characteristics

Unless otherwise noted: $T_A = 25°C$, $V_{CM} = V_S/2$, $R_L > 10\ k\Omega$.

Offset Voltage Distribution



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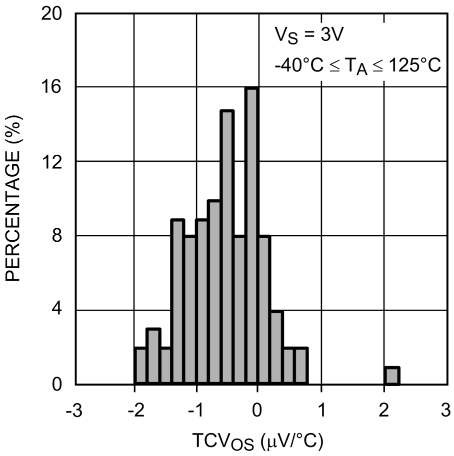
TCV_{OS} Distribution



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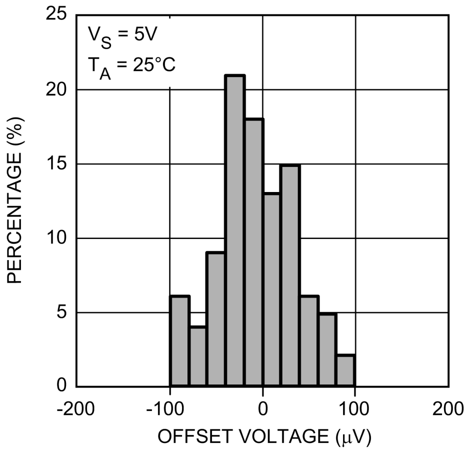
Offset Voltage Distribution



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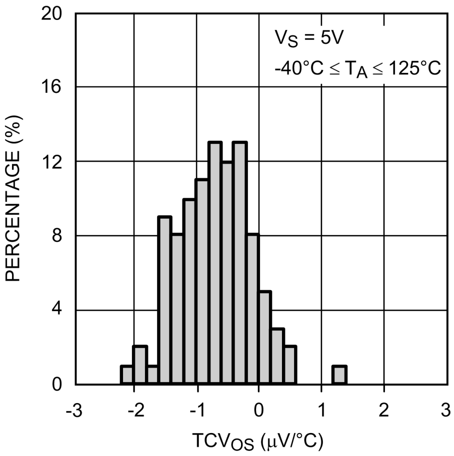
TCV_{OS} Distribution



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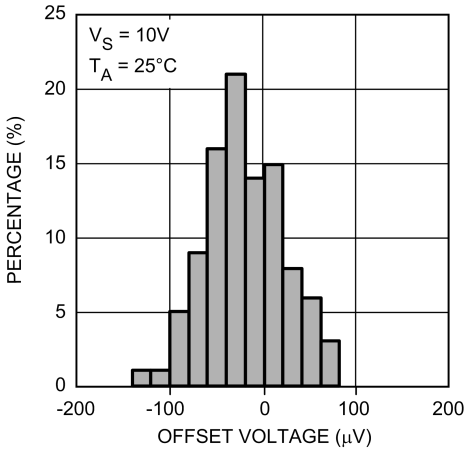
Offset Voltage Distribution



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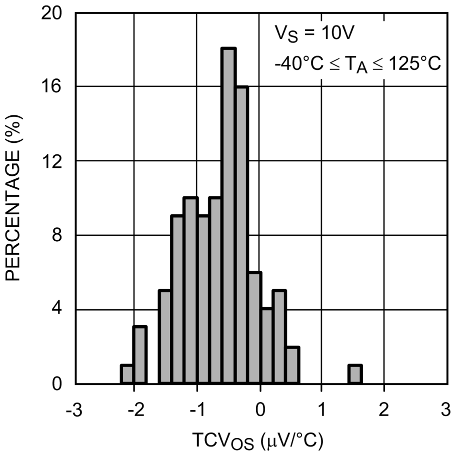
TCV_{OS} Distribution



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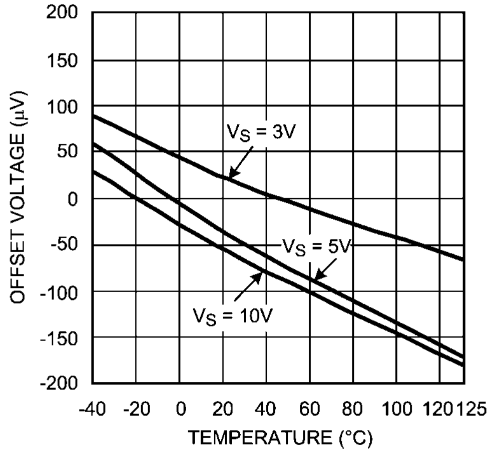

Offset Voltage vs. Temperature

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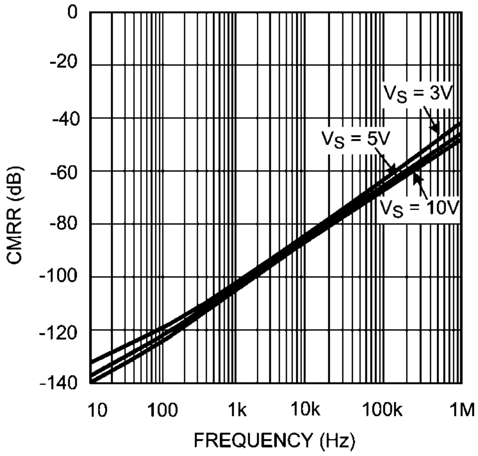

CMRR vs. Frequency

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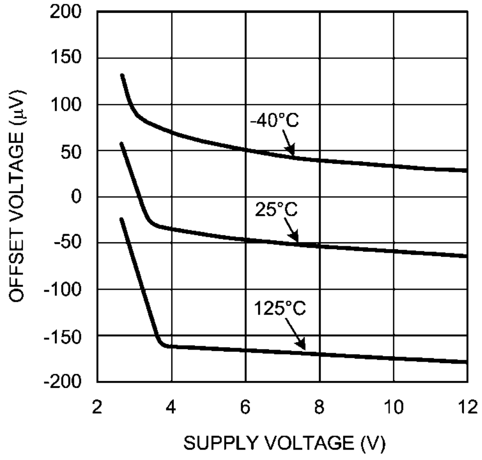

Offset Voltage vs. Supply Voltage

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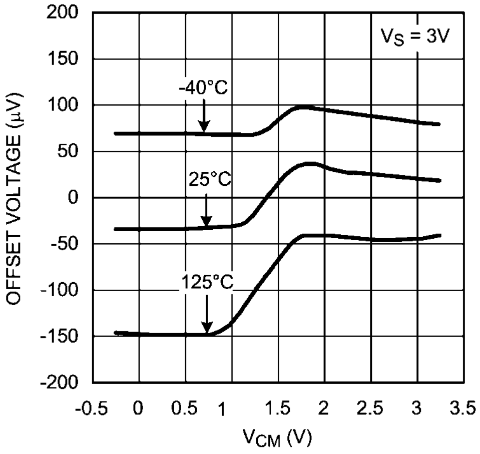

Offset Voltage vs. V_{CM}

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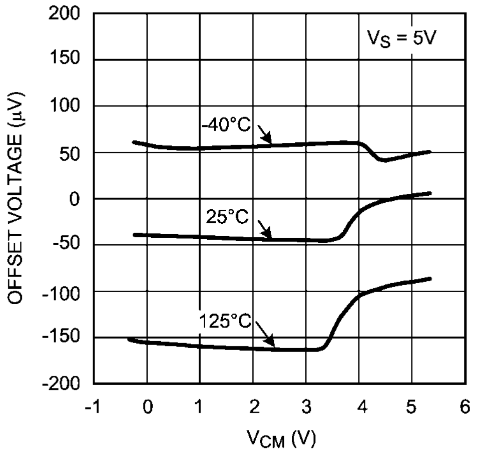

Offset Voltage vs. V_{CM}

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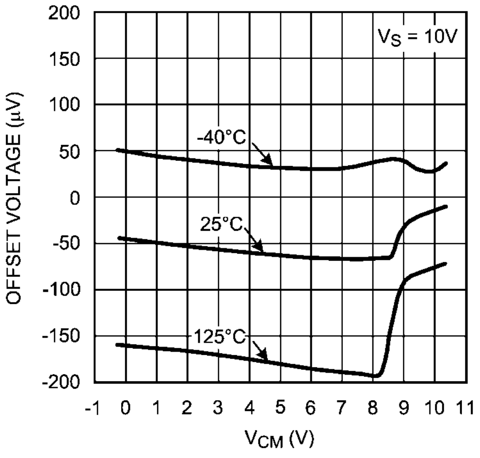

Offset Voltage vs. V_{CM}

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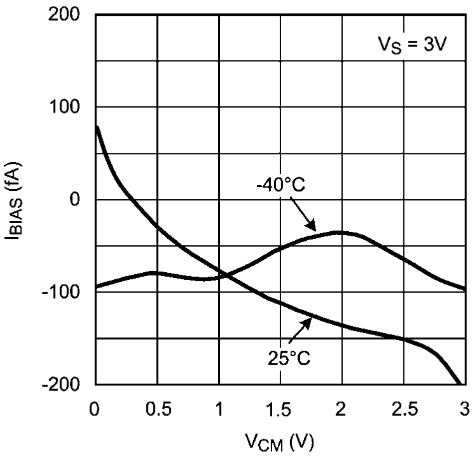
Input Bias Current vs. V_{CM}



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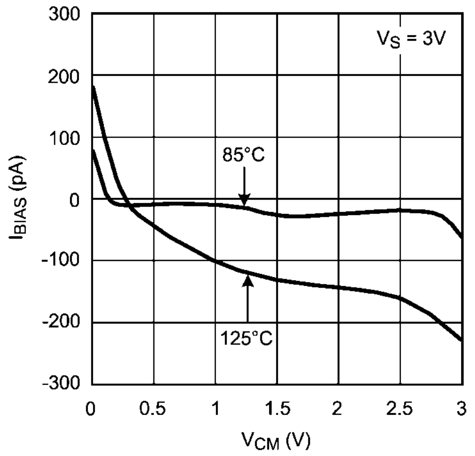
Input Bias Current vs. V_{CM}



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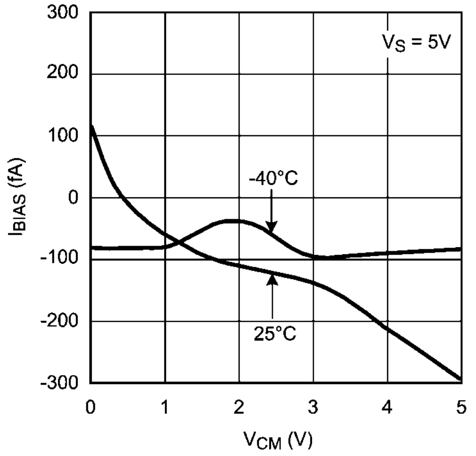
Input Bias Current vs. V_{CM}



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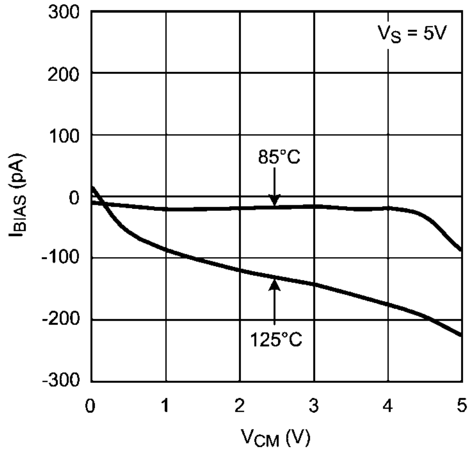
Input Bias Current vs. V_{CM}



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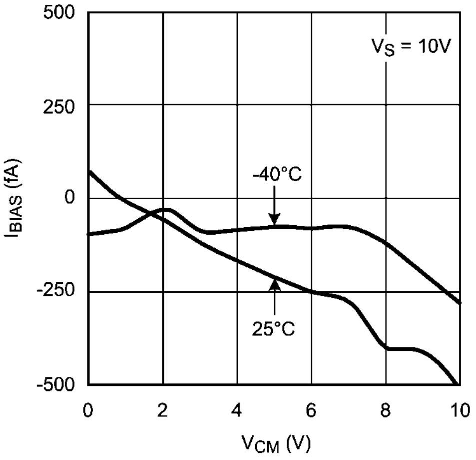
Input Bias Current vs. V_{CM}



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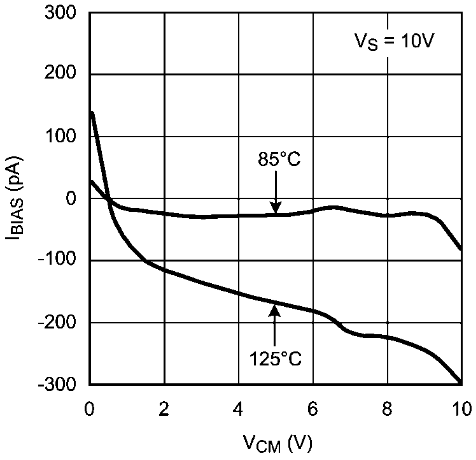
Input Bias Current vs. V_{CM}



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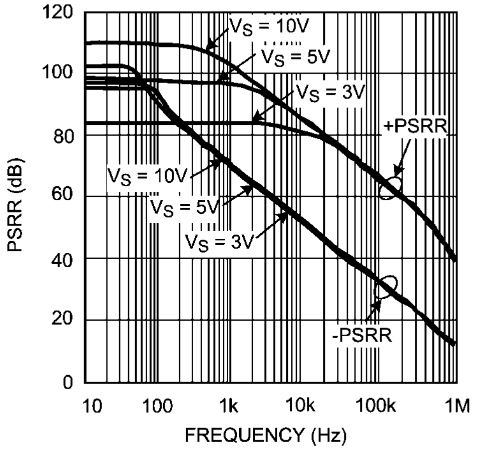
PSRR vs. Frequency



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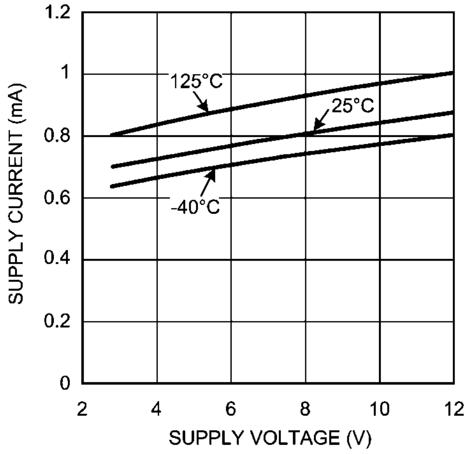
Supply Current vs. Supply Voltage (Per Channel)



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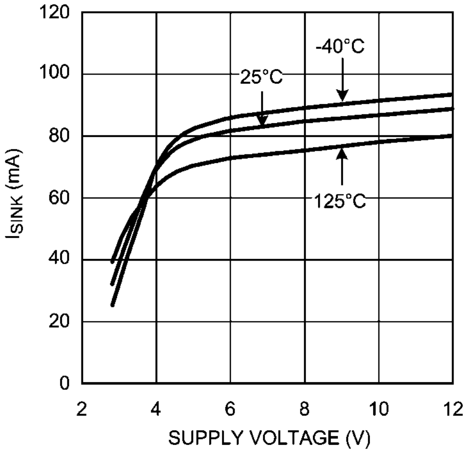
Sinking Current vs. Supply Voltage



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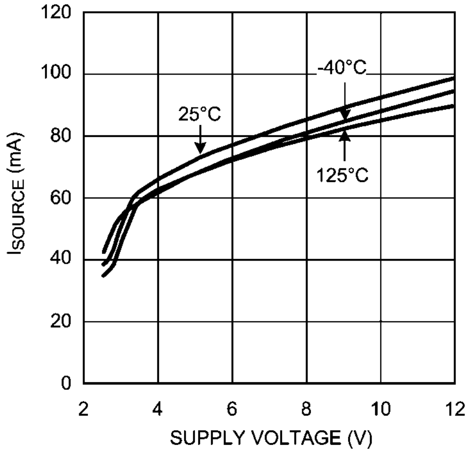
Sourcing Current vs. Supply Voltage



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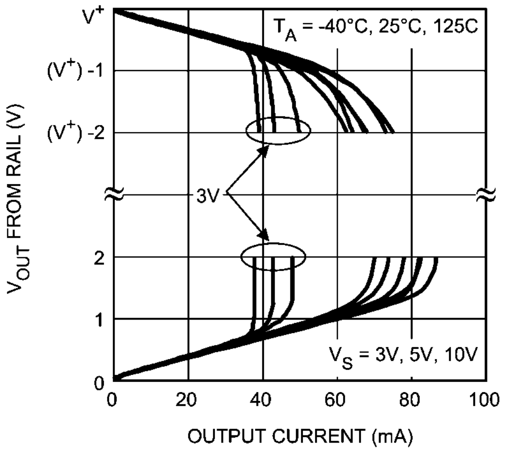
Output Voltage vs. Output Current



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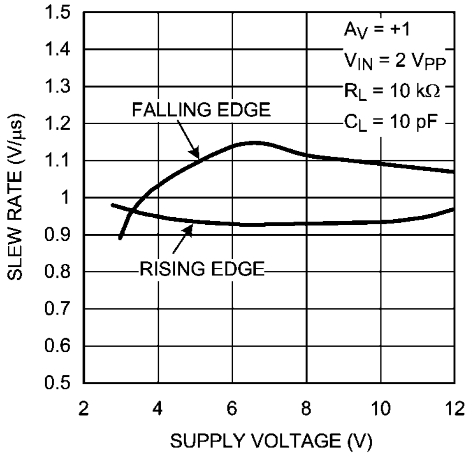
Slew Rate vs. Supply Voltage



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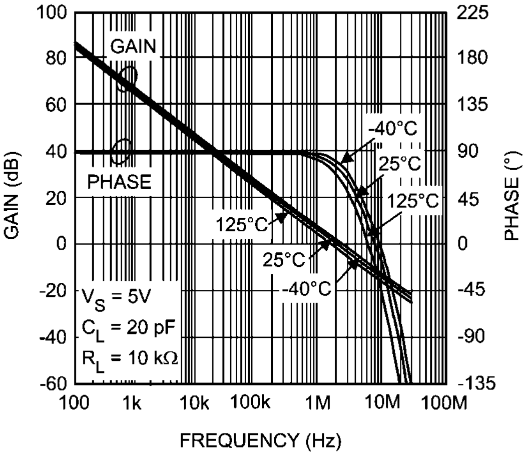
Open Loop Frequency Response



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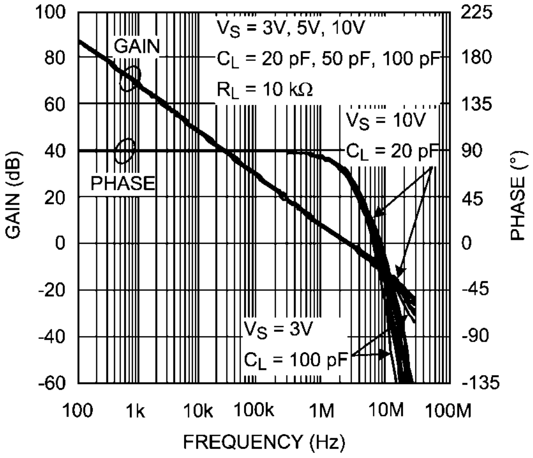
Open Loop Frequency Response



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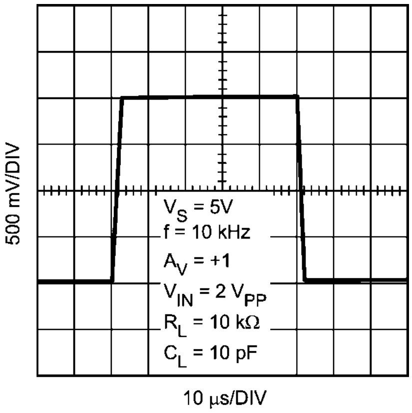
Large Signal Step Response



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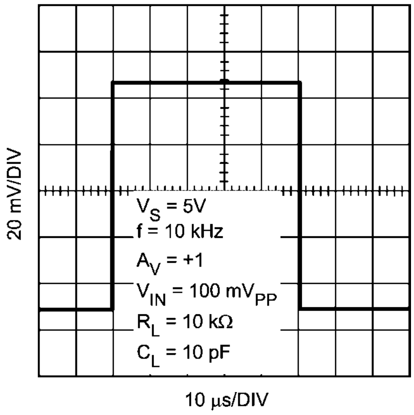
Small Signal Step Response



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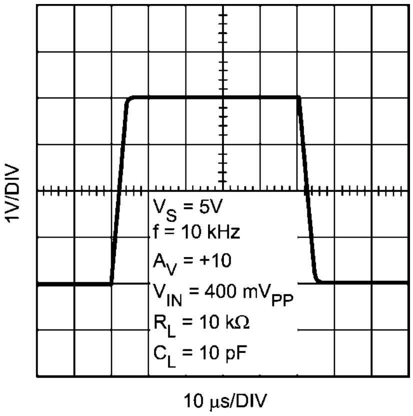
Large Signal Step Response



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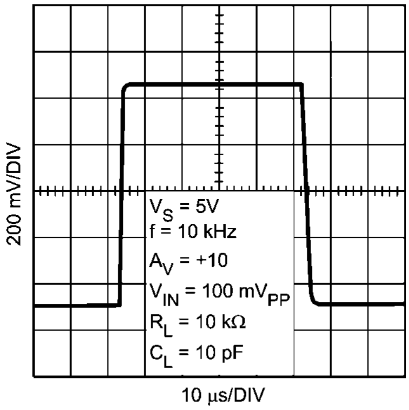
Small Signal Step Response



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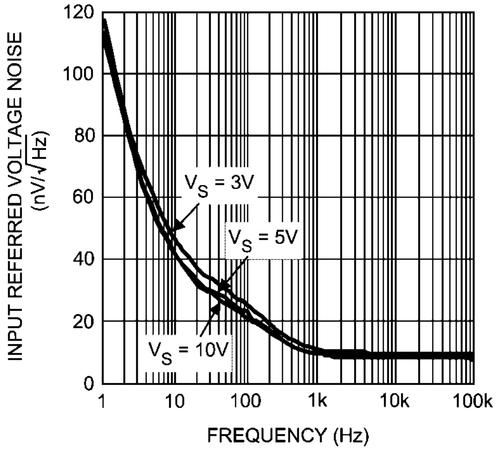
Input Voltage Noise vs. Frequency



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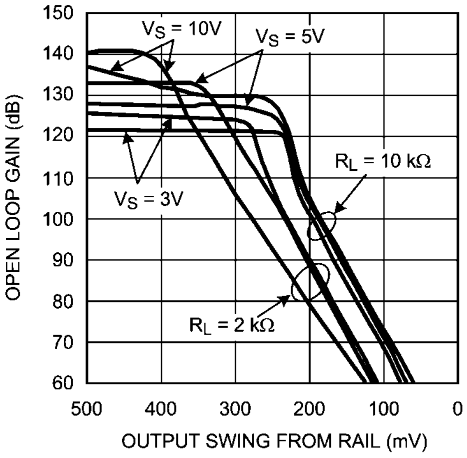
Open Loop Gain vs. Output Voltage Swing



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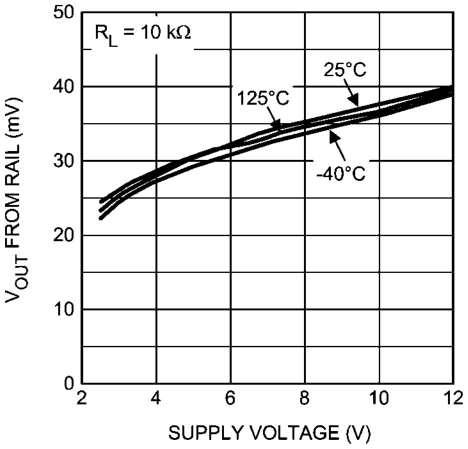
Output Swing High vs. Supply Voltage



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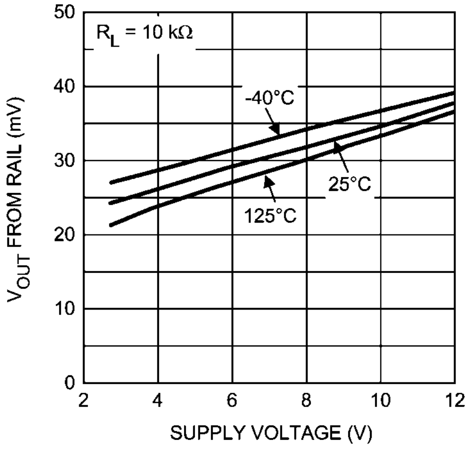
Output Swing Low vs. Supply Voltage



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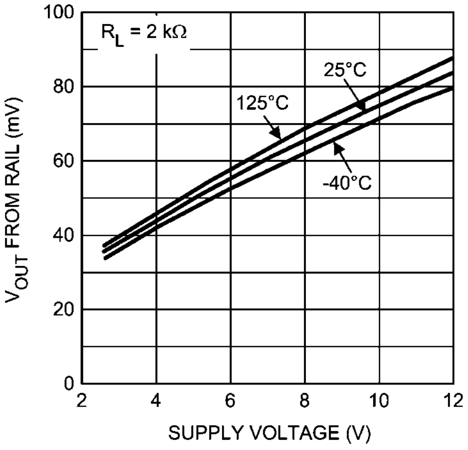
Output Swing High vs. Supply Voltage



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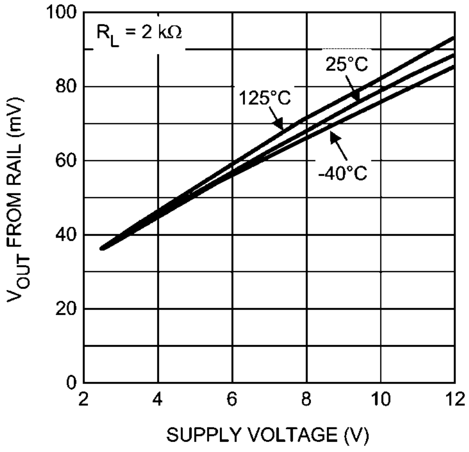
Output Swing Low vs. Supply Voltage



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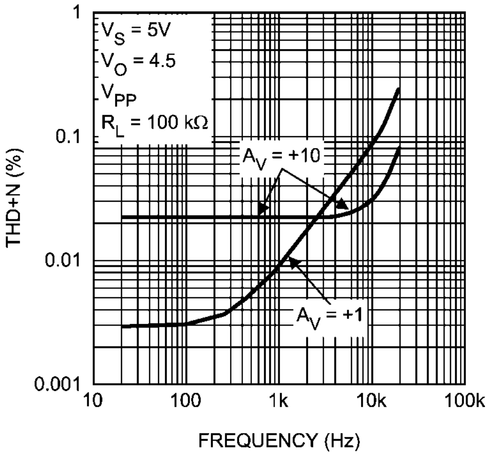

THD+N vs. Frequency

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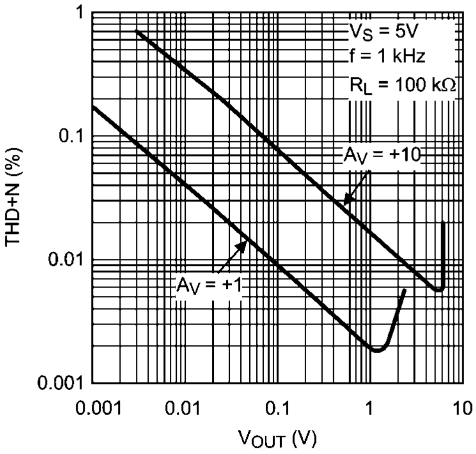

THD+N vs. Output Voltage

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Application Information

SM72501

The SM72501 is a low offset voltage, rail-to-rail input and output precision amplifier with a CMOS input stage and wide supply voltage range of 2.7V to 12V. The SM72501 has a very low input bias current of only ±200 fA at room temperature.

The wide supply voltage range of 2.7V to 12V over the extensive temperature range of −40°C to 125°C makes the SM72501 an excellent choice for low voltage precision applications with extensive temperature requirements.

The SM72501 has only ±37 µV of typical input referred offset voltage and this offset is guaranteed to be less than ±500 µV over temperature. This minimal offset voltage allows more accurate signal detection and amplification in precision applications.

The low input bias current of only ±200 fA along with the low input referred voltage noise of 9 $nV/\sqrt{Hz}$ gives the SM72501 superiority for use in sensor applications. Lower levels of noise from the SM72501 means better signal fidelity and a higher signal-to-noise ratio.

National Semiconductor is heavily committed to precision amplifiers and the market segment they serve. Technical support and extensive characterization data is available for sensitive applications or applications with a constrained error budget.

The SM72501 is offered in the space saving 5-Pin SOT23. This small package is an ideal solution for area constrained PC boards and portable electronics.

CAPACITIVE LOAD

The SM72501 can be connected as a non-inverting unity gain follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

In order to drive heavier capacitive loads, an isolation resistor, R_{ISO}, in *Figure 1* should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO}, the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L. However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

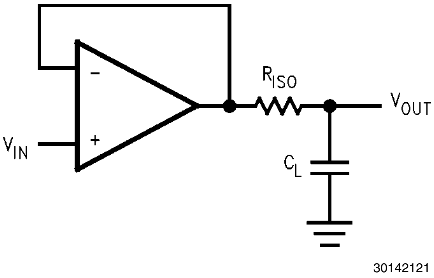

FIGURE 1. Isolating Capacitive Load

INPUT CAPACITANCE

CMOS input stages inherently have low input bias current and higher input referred voltage noise. The SM72501 enhances this performance by having the low input bias current of only ±200 fA, as well as, a very low input referred voltage noise of 9 $nV/\sqrt{Hz}$. In order to achieve this a larger input stage has been used. This larger input stage increases the input capacitance of the SM72501. The typical value of this input capacitance, C_{IN}, for the SM72501 is 25 pF. The input capacitance will interact with other impedances such as gain and feedback resistors, which are seen on the inputs of the amplifier, to form a pole. This pole will have little or no effect on the output of the amplifier at low frequencies and DC conditions, but will play a bigger role as the frequency increases. At higher frequencies, the presence of this pole will decrease phase margin and will also cause gain peaking. In order to compensate for the input capacitance, care must be taken in choosing the feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The DC gain of the circuit shown in *Figure 2* is simply $-R_2/R_1$.

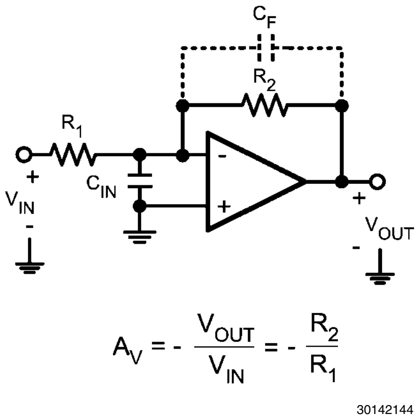

FIGURE 2. Compensating for Input Capacitance

For the time being, ignore C_F. The AC gain of the circuit in *Figure 2* can be calculated as follows:

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2}\right)} + \frac{s^2}{\left(\frac{A_0}{C_{IN} R_2}\right)}\right]}$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{IN}}\left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2}\right)^2 - \frac{4A_0C_{IN}}{R_2}}\,\right] \qquad (1)$$

As shown in *Equation 1*, as values of R_1 and R_2 are increased, the magnitude of the poles is reduced, which in turn decreases the bandwidth of the amplifier. Whenever possible, it is best to choose smaller feedback resistors. *Figure 3* shows the effect of the feedback resistor on the bandwidth of the SM72501.

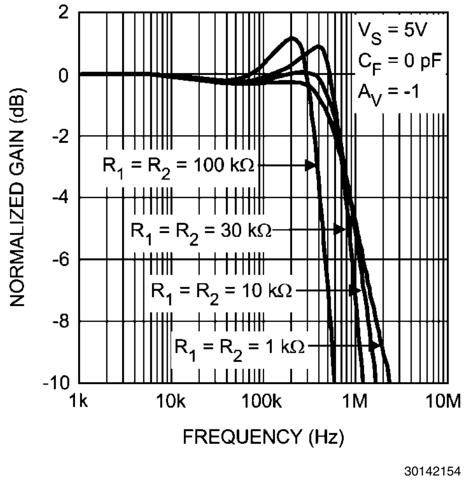

FIGURE 3. Closed Loop Gain vs. Frequency

Equation 1 has two poles. In most cases, it is the presence of pairs of poles that causes gain peaking. In order to eliminate this effect, the poles should be placed in Butterworth position, since poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in *Equation 1* should be set to equal −1. Using this fact and the relation between R_1 and R_2, $R_2 = -A_V R_1$, the optimum value for R_1 can be found. This is shown in *Equation 2*. If R_1 is chosen to be larger than this optimum value, gain peaking will occur.

$$R_1 < \frac{(1 - A_V)^2}{2A_0 A_V C_{IN}} \tag{2}$$

In *Figure 2*, C_F is added to compensate for input capacitance and to increase stability. Additionally, C_F reduces or eliminates the gain peaking that can be caused by having a larger feedback resistor. *Figure 4* shows how C_F reduces gain peaking.

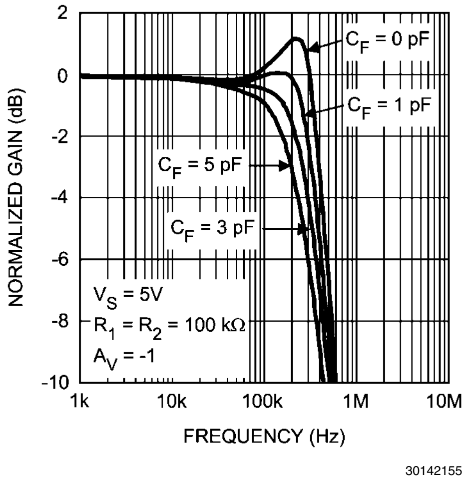

FIGURE 4. Closed Loop Gain vs. Frequency with Compensation

DIODES BETWEEN THE INPUTS

The SM72501 has a set of anti-parallel diodes between the input pins, as shown in *Figure 5*. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ±300 mV or the input current needs to be limited to ±10 mA.

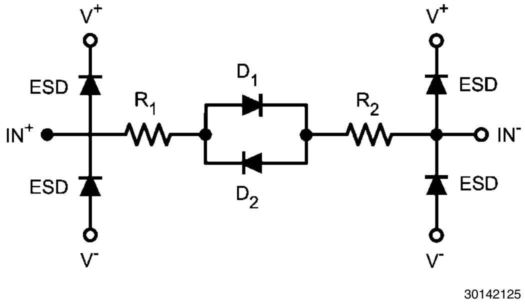

FIGURE 5. Input of SM72501

PRECISION CURRENT SOURCE

The SM72501 can be used as a precision current source in many different applications. *Figure 6* shows a typical precision current source. This circuit implements a precision voltage controlled current source. Amplifier A1 is a differential amplifier that uses the voltage drop across R_S as the feedback signal. Amplifier A2 is a buffer that eliminates the error current from the load side of the R_S resistor that would flow in the feedback resistor if it were connected to the load side of the R_S resistor. In general, the circuit is stable as long as the closed loop bandwidth of amplifier A2 is greater then the closed loop bandwidth of amplifier A1. Note that if A1 and A2 are the same type of amplifiers, then the feedback around A1 will reduce its bandwidth compared to A2.

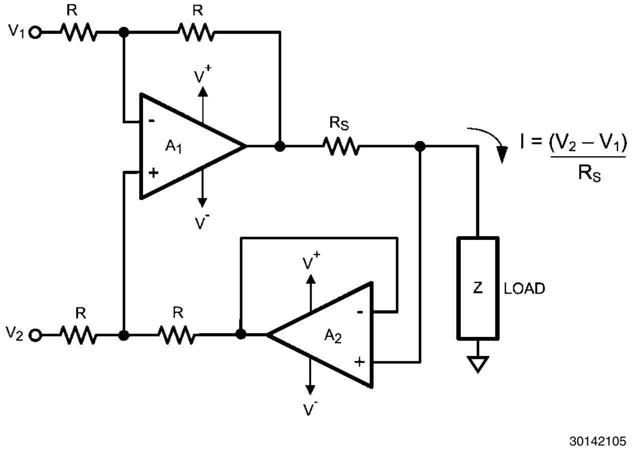

FIGURE 6. Precision Current Source

The equation for output current can be derived as follows:

$$\frac{V_2R}{R+R} + \frac{(V_0 - IR_S)R}{R+R} = \frac{V_1R}{R+R} + \frac{V_0R}{R+R}$$

Solving for the current I results in the following equation:

$$I = \frac{V_2 - V_1}{R_S}$$

LOW INPUT VOLTAGE NOISE

The SM72501 has a very low input voltage noise of $9\ \text{nV}/\sqrt{\text{Hz}}$. This input voltage noise can be further reduced by placing N amplifiers in parallel as shown in *Figure 7*. The total voltage noise on the output of this circuit is divided by the square root of the number of amplifiers used in this parallel combination. This is because each individual amplifier acts as an independent noise source, and the average noise of independent sources is the quadrature sum of the independent sources divided by the number of sources. For N identical amplifiers, this means:

$$\text{REDUCED INPUT VOLTAGE NOISE} = \frac{1}{N}\sqrt{e_{n1}^2 + e_{n2}^2 + \cdots + e_{nN}^2}$$

$$= \frac{1}{N}\sqrt{Ne_n^2} = \frac{\sqrt{N}}{N}\, e_n$$

$$= \frac{1}{\sqrt{N}}\, e_n$$

Figure 7 shows a schematic of this input voltage noise reduction circuit. Typical resistor values are:

$R_G = 10\Omega$, $R_F = 1\ \text{k}\Omega$, and $R_O = 1\ \text{k}\Omega$.

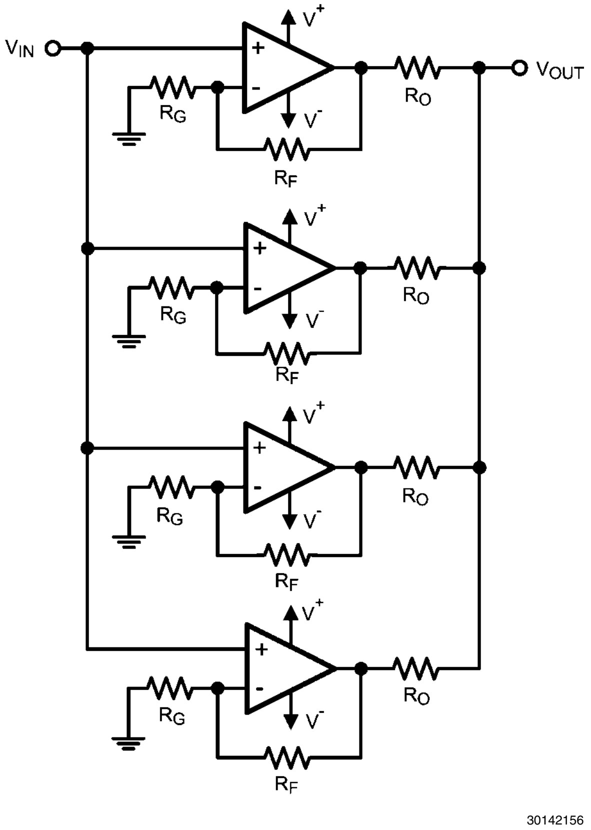

FIGURE 7. Noise Reduction Circuit

TOTAL NOISE CONTRIBUTION

The SM72501 has very low input bias current, very low input current noise, and very low input voltage noise. As a result, these amplifiers are ideal choices for circuits with high impedance sensor applications.

Figure 8 shows the typical input noise of the SM72501 as a function of source resistance where:

e_n denotes the input referred voltage noise

e_i is the voltage drop across source resistance due to input referred current noise or $e_i = R_S * i_n$

e_t shows the thermal noise of the source resistance

e_{ni} shows the total noise on the input.

Where:

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2}$$

The input current noise of the SM72501 is so low that it will not become the dominant factor in the total noise unless source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in *Figure 8*, at lower R_S values, total noise is dominated by the amplifier's input voltage noise. Once R_S is larger than a few kilo-Ohms, then the dominant noise factor becomes the thermal noise of R_S. As mentioned before, the current noise will not be the dominant noise factor for any practical application.

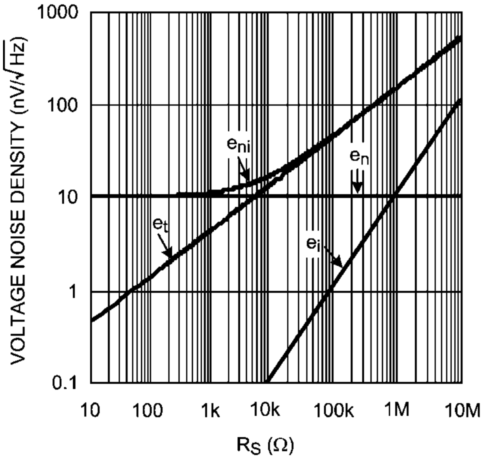

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FIGURE 8. Total Input Noise

HIGH IMPEDANCE SENSOR INTERFACE

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor's output and cause a voltage drop across the source resistance as shown in *Figure 9*, where $V_{IN}^+ = V_S - I_{BIAS} * R_S$

The last term, $I_{BIAS} * R_S$, shows the voltage drop across R_S. To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. This is to keep the error contribution by $I_{BIAS} * R_S$ less than the input voltage noise of the amplifier, so that it will not become the dominant noise factor.

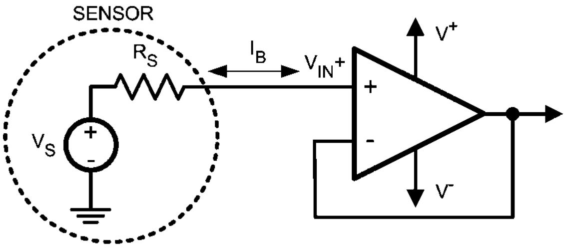

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FIGURE 9. Noise Due to I_{BIAS}

pH electrodes are very high impedance sensors. As their name indicates, they are used to measure the pH of a solution. They usually do this by generating an output voltage which is proportional to the pH of the solution. pH electrodes are calibrated so that they have zero output for a neutral solution, pH = 7, and positive and negative voltages for acidic or alkaline solutions. This means that the output of a pH electrode is bipolar and has to be level shifted to be used in a single supply system. The rate of change of this voltage is usually shown in mV/pH and is different for different pH sensors. Temperature is also an important factor in a pH electrode reading. The output voltage of the senor will change with temperature.

Figure 10 shows a typical output voltage spectrum of a pH electrode. Note that the exact values of output voltage will be different for different sensors. In this example, the pH electrode has an output voltage of 59.15 mV/pH at 25°C.

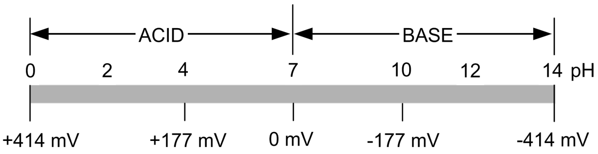

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FIGURE 10. Output Voltage of a pH Electrode

The temperature dependence of a typical pH electrode is shown in *Figure 11*. As is evident, the output voltage changes with changes in temperature.

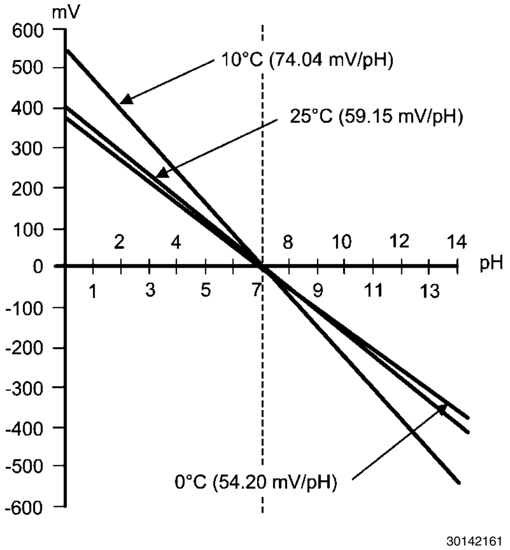


FIGURE 11. Temperature Dependence of a pH Electrode

The schematic shown in *Figure 12* is a typical circuit which can be used for pH measurement. The LM35 is a precision integrated circuit temperature sensor. This sensor is differentiated from similar products because it has an output voltage linearly proportional to Celcius measurement, without the need to convert the temperature to Kelvin. The LM35 is used to measure the temperature of the solution and feeds this reading to the Analog to Digital Converter, ADC. This information is used by the ADC to calculate the temperature effects on the pH readings. The LM35 needs to have a resistor, R_T in *Figure 12*, to $-V^+$ in order to be able to read temperatures below 0°C. R_T is not needed if temperatures are not expected to go below zero.

The output of pH electrodes is usually large enough that it does not require much amplification; however, due to the very high impedance, the output of a pH electrode needs to be buffered before it can go to an ADC. Since most ADCs are operated on single supply, the output of the pH electrode also needs to be level shifted. Amplifier A1 buffers the output of the pH electrode with a moderate gain of +2, while A2 provides the level shifting. V_{OUT} at the output of A2 is given by: $V_{OUT} = -2V_{pH} + 1.024V$.

The LM4140A is a precision, low noise, voltage reference used to provide the level shift needed. The ADC used in this application is the ADC12032 which is a 12-bit, 2 channel converter with multiplexers on the inputs and a serial output. The 12-bit ADC enables users to measure pH with an accuracy of 0.003 of a pH unit. Adequate power supply bypassing and grounding is extremely important for ADCs. Recommended bypass capacitors are shown in *Figure 12*. It is common to share power supplies between different components in a circuit. To minimize the effects of power supply ripples caused by other components, the op amps need to have bypass capacitors on the supply pins. Using the same value capacitors as those used with the ADC are ideal. The combination of these three values of capacitors ensures that AC noise present on the power supply line is grounded and does not interfere with the amplifiers' signal.

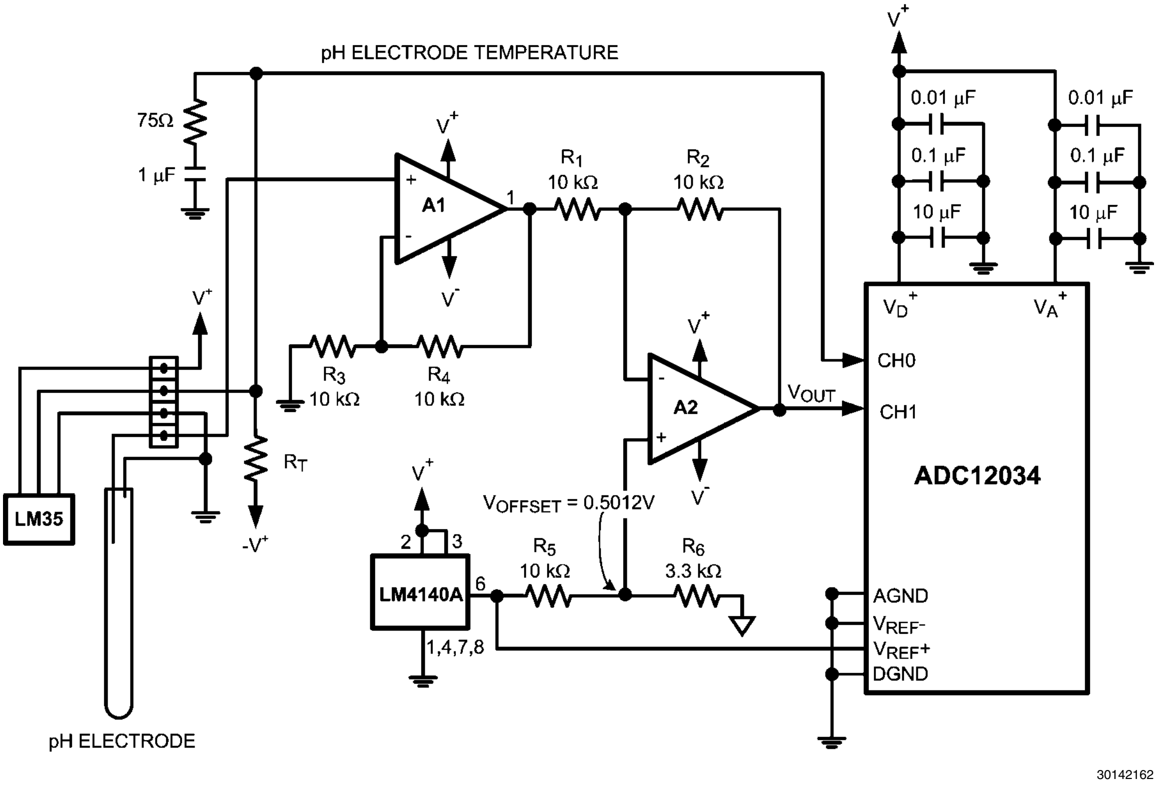
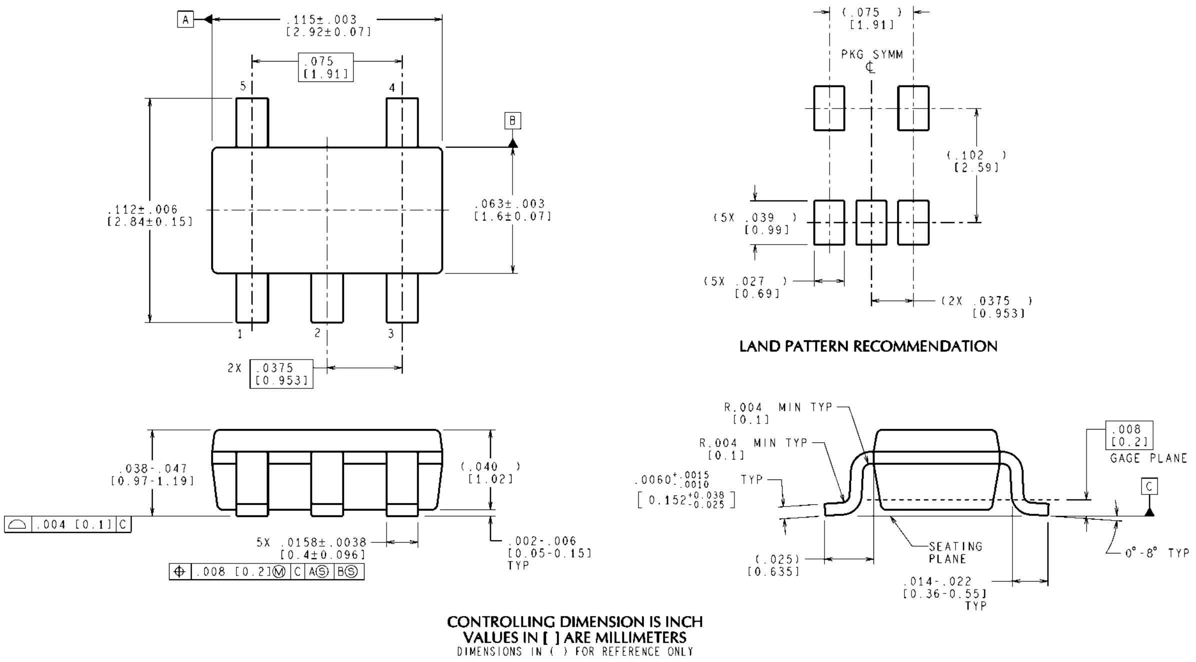


FIGURE 12. pH Measurement Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



MF05A (Rev D)

5-Pin SOT23
NS Package Number MF05A

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