DUAL 4-INPUT MULTIPLEXER; 3-STATE

FEATURES

- Non-inverting data path
- 3-state outputs for bus interface
- and multiplex expansion
- Common select inputs
- Separate output enable inputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT253 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT253 have two identical 4-input multiplexers with 3-state outputs which select two bits from four sources selected by common data select inputs (S_0, S_1).

When the individual output enable ($1\overline{OE}$, $2\overline{OE}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to the high impedance OFF-state.

The "253" is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S_0 and S_1.

The logic equations for the outputs are:

$$1Y = 1\overline{OE}(1I_0.\overline{S}_1.\overline{S}_0 + 1I_1.\overline{S}_1.S_0 + 1I_2.S_1.\overline{S}_0 + 1I_3.S_1.S_0)$$

$$2Y = 2\overline{OE}(2I_0.\overline{S}_1.\overline{S}_0 + 2I_1.\overline{S}_1.S_0 + 2I_2.S_1.\overline{S}_0 + 2I_3.S_1.S_0)$$

APPLICATIONS

- Data selectors
- Data multiplexers

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay $1I_n$, $2I_n$ to nY; S_n to nY	C_L = 15 pF V_{CC} = 5 V	17 18	17 19	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	55	55	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{OE}$, $2\overline{OE}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
7, 9	1Y, 2Y	3-state multiplexer outputs
8	GND	ground (0 V)
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

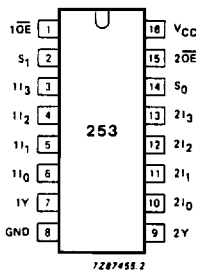

Fig. 1 Pin configuration.

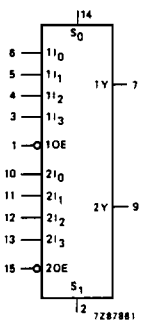

Fig. 2 Logic symbol.

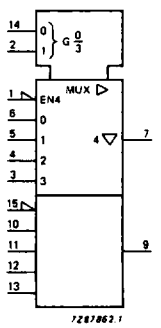

Fig. 3 IEC logic symbol.

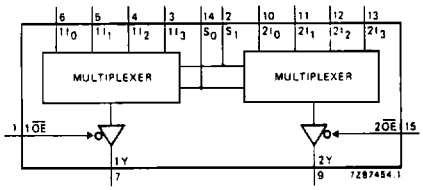

Fig. 4 Functional diagram.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	nI_0	nI_1	nI_2	nI_3	$n\overline{OE}$	nY
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

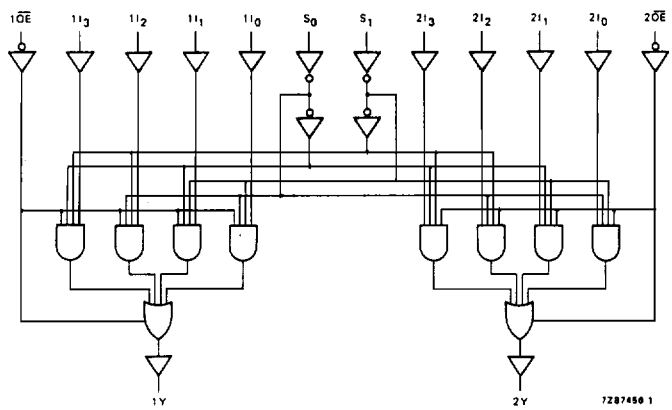

Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY		58 21 17	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		30 11 9	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		41 15 12	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$1I_n$	0.40
$2I_n$	0.40
$n\overline{OE}$	1.10
S_0	1.10
S_1	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay $1I_n$ to nY; $2I_n$ to nY		20	38		48		57	ns	4.5	Fig. 6
t_{PHL}/t_{PLH}	propagation delay S_n to nY		22	40		50		60	ns	4.5	Fig. 6
t_{PZH}/t_{PZL}	3-state output enable time $n\overline{OE}$ to nY		14	30		38		45	ns	4.5	Fig. 7
t_{PHZ}/t_{PLZ}	3-state output disable time $n\overline{OE}$ to nY		13	30		38		45	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Fig. 6

AC WAVEFORMS

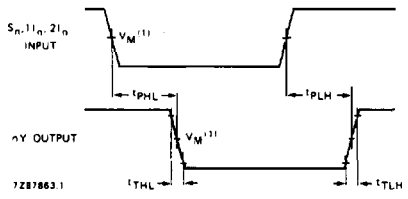

Fig. 6 Waveforms showing the input ($1I_n$, $2I_n$) to output (1Y, 2Y) propagation delays and the output transition times.

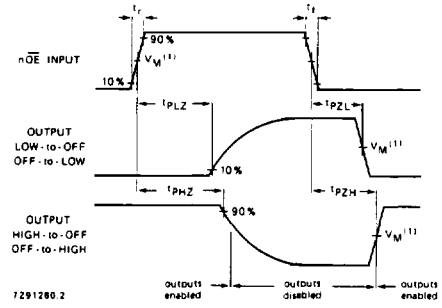

Fig. 7 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.