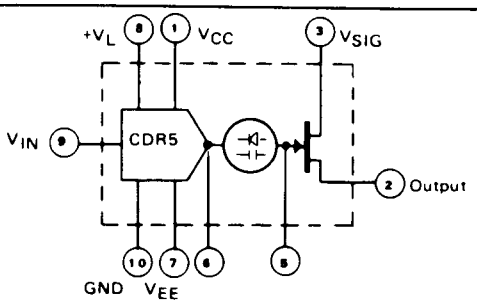
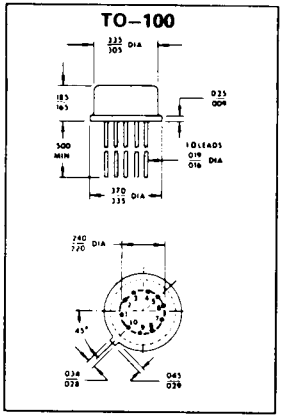
LOW COST
FET ANALOG GATE
SPST

CAG30

- 60 OHM MAX. R_{on}
- WORKS DIRECTLY FROM LOGIC
- HIGH LOGIC NOISE IMMUNITY
- BREAK BEFORE MAKE ACTION
- ± 10V SIGNAL LEVELS AC OR DC



PINS 5 AND 6 ARE NOT USED IN NORMAL OPERATION (LEAVE OPEN)



Logic 1 (≥ 2.0V) closes contacts
Logic 0 (≤ 1.0V) opens contacts

MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Operating Temperature	T_{op}	-55	+125	°C
Storage Temperature	T_{stg}	-55	+150	°C
Logic Supply Voltage	V_L	+4.5	+5.5	V
Logic Input Voltage	V_{IN}	0	V_L	V
Positive Supply Voltage	V_{CC}	0	+18	V
Negative Supply Voltage	V_{EE}	-18	-7	V

The CAG30 is a low cost general purpose FET analog gate capable of switching up to ±10V signals directly from DTL or TTL while providing high logic noise immunity (typically 1.0V). The use of a monolithic switching circuit as a driver has the advantage of small size and full military temperature range at low cost. The CAG30 turns off faster than it turns on to allow multiplexing without shorting.

ELECTRICAL SPECIFICATIONS: V_L = +5.0V; V_{EE} = -18V; V_{CC} = +18V (unless otherwise stated), T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Signal Voltage Range	V_{SIG}	See Note (1)	-10	–	+10	V
Off Leakage Current	$I_{D\ (off)}$	V_{SIG} = -10V, V_{IN} = 1.0V	–	–	1.0	nA
Drain-Source On-Resistance	R_{ds}	I_{SIG} = 1mA, V_{IN} = 2.0V	–	–	60	Ohms
** Turn-on Time	t_{on}	V_{SIG} = +5V, R_L = 1K	–	–	1.0	μsec
** Turn-off Time	t_{off}	V_{SIG} = +5V, R_L = 1K	–	–	0.5	μsec
Logic "1" Input Voltage	$V_{IN}(1)$		2.0	–	–	V
Logic "0" Input Voltage	$V_{IN}(0)$		–	–	1.0	V
* Logic "1" Input Current	$I_{IN}(1)$	V_{IN} = 2.0V	–	–	30	μA
* Logic "0" Input Current	$I_{IN}(0)$	V_{IN} = 1.0V	–	–	10	μA
* Signal Current Limit	$I_{SIG\text{-}LIM}$	V_{DS} = 2.0V, V_{GS} = 0	–	20	–	mA
* Drain-Gate Capacitance	C_{dgo}	V_{dg}=10V, I_S=0, f=140kHz	–	6	–	pfd
* Source-Gate Capacitance	C_{sgo}	V_{sg}=10V, I_D=0, f=140kHz	–	6	–	pfd
* Logic Supply Current	I_L		–	1.8	4	mA
* Positive Supply Current	I_{CC}		–	3.5	5	mA
* Negative Supply Current	I_{EE}		–	3.5	5	mA
* Total Power Dissipation	P_T		–	75	150	mW

NOTE: 1) V_{SIG} limits are determined by the VCC and VEE voltages. VSIG min. = (VEE + 8V) and VSIG max. = (VCC-2V)
Ex: VEE = -8V, VCC = +8V, VSIG = 0 to +6V
*These parameters guaranteed but may not be tested.
**Includes propagation delay.

TELEDYNE CRYSTALONICS
147 Sherman Street, Cambridge, MA 02140 USA
Tel: (617) 491-1670 • FAX: 617/547-6119 • TWX: 710-320-1196