M5M51004P,J-25,-35,-45,-25L,-35L,-45L

1048576-BIT (262144-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M51004 is a family of 262144-word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate process and designed for high-speed application. These devices operate on a single 5V supply, and are TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M51004P,J-25,-25L ..... 25ns(max)
  M5M51004P,J-35,-35L ..... 35ns(max)
  M5M51004P,J-45,-45L ..... 45ns(max)
- Low power dissipation Active ..... 400mW(typ)
  Stand by ..... 5mW(typ)
- Power down by $\overline{S}$
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by $\overline{S}$
- $\overline{OE}$ prevents data contention in the I/O bus

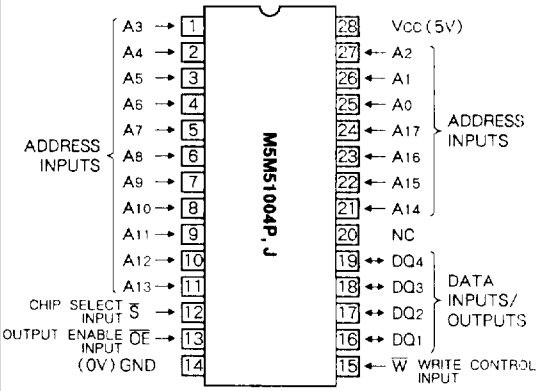
PACKAGE

M5M51004P ..... 28pin 400mil DIP
M5M51004J ..... 28pin 400mil SOJ

APPLICATION

High-speed memory systems

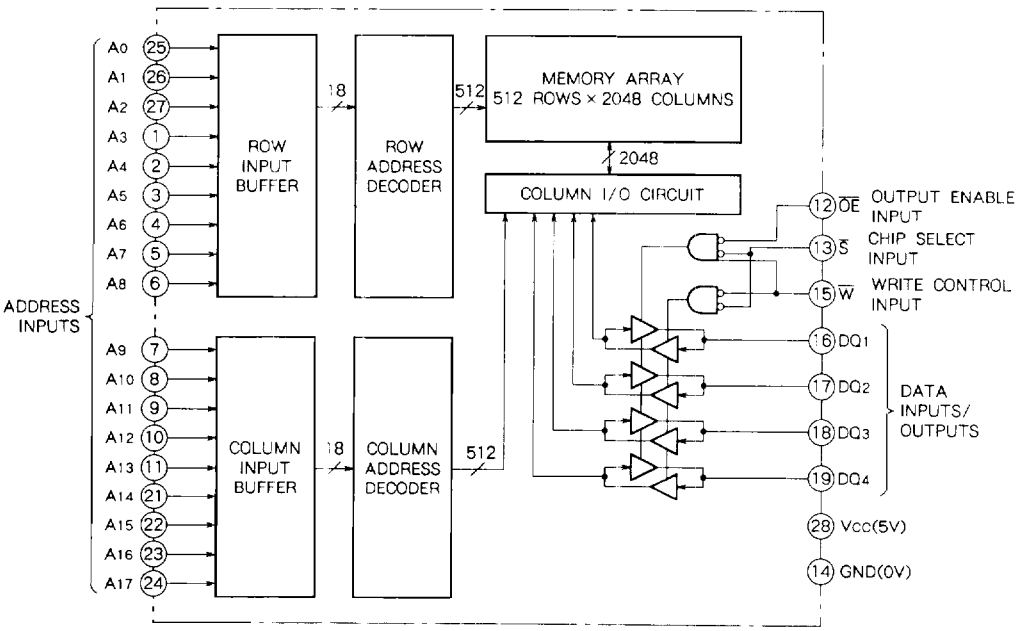
PIN CONFIGURATION (TOP VIEW)



Outline 28P4F (P)
28P0K (J)

NC : NO CONNECTION

BLOCK DIAGRAM



FUNCTION

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period address signals must be stable. When $\overline{W}$ is low, the DQ terminals are maintained in the high impedance state, so it is possible to connect D and Q terminal directly.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ and $\overline{OE}$ to low if the address signals are stable, the data is available at DQ terminal.

When $\overline{S}$ is high, the chip is the non-selectable state, disabling both reading and writing. In this case, the output is in the floating (high-impedance) state, useful for OR-tie with other devices.

Setting the $\overline{OE}$ at a high level, the output stage is in a high impedance state, and the data bus contention problem in the write cycle is eliminated.

Signal $\overline{S}$ controls the power-down features. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

FUNCTION TABLE

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
H	X	X	Not select	Hi-Z	Stand by
L	L	X	Write	D_{in}	Active
L	H	L	Read	D_{out}	Active
L	H	H		Hi-Z	Active

Note. H : V_{IH}, L : V_{IL}, X : Don't care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−3.5*~7	V
V_I	Input voltage		−3.5*~7	V
V_O	Output voltage		−3.5*~7	V
P_d	Power dissipation		1	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		−65~150	℃
$T_{stg(bias)}$	Storage temperature		−10~85	℃

* Pulse width ≤ 20ns, in case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.2		Vcc+0.3	V
V_{IL}	Low-level input voltage			−0.5*		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −4mA		2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8mA				0.4	V
I_I	Input current	V_I = 0~Vcc				2	μA
I_{OZ}	Off-state output current	$V_{I(S)}$ = V_{IH}, V_O = 0~Vcc				10	μA
I_{CC1}	Supply current from Vcc	$V_{I(S)}$ = V_{IL}, Output open	AC (Min cycle)			140	mA
			DC		60	75	mA
I_{CC2}	Stand by current	$V_{I(S)}$ = V_{IH}	AC (Min cycle)			40	mA
			DC			30	mA
I_{CC3}	Stand by current	$V_{I(S)}$ ≧ Vcc − 0.2V, Other V_I ≦ 0.2V or V_I ≧ Vcc − 0.2V	-25, -35, -45		1	10	mA
			-25L, -35L, -45L		10	100	μA

* Pulse width ≤ 20ns, in case of DC : −0.5V

CAPACITANCE (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I = GND, V_I = 25mVrms, f = 1MHz			6	pF
C_O	Input output capacitance	$V_{I/O}$ = GND, $V_{I/O}$ = 25mVrms, f = 1MHz			6	pF

Note 1. Current flowing into an IC is positive, out is negative.

* C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ..... V_{IH} = 3V, V_{IL} = 0V
Input rise and fall time 3ns
Input timing reference levels ..... V_{IH} = 1.5V, V_{IL} = 1.5V
Output timing reference levels ..... V_{OH} = 1.5V, V_{OL} = 1.5V

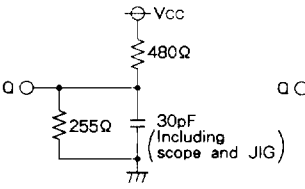


Fig.1 Output load

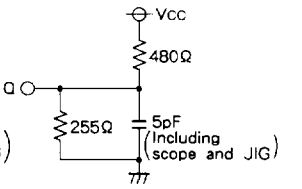


Fig. 2 Output load for t_{en}, t_{dis}

(2) READ CYCLE

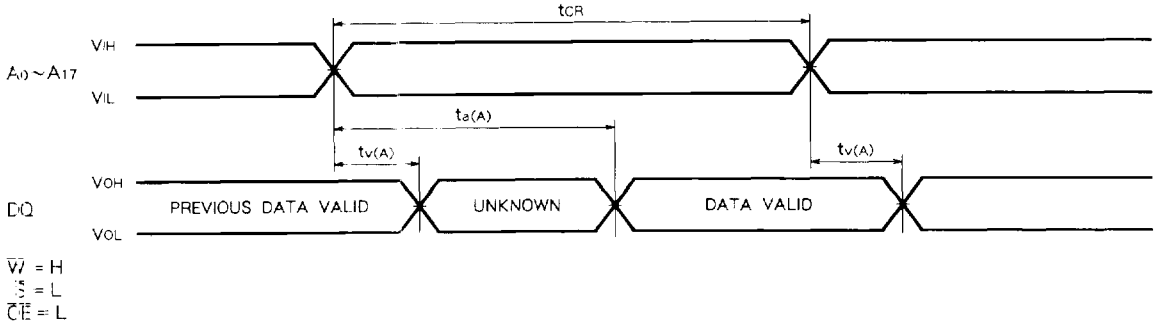
Symbol	Parameter	Limits									Unit
		M5M51004-25,-25L			M5M51004-35,-35L			M5M51004-45,-45L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CR}	Read cycle time	25			35			45			ns
$t_{a(A)}$	Address access time			25			35			45	ns
$t_{a(S)}$	Chip select access time			25			35			45	ns
$t_{a(OE)}$	Output enable access time			13			18			23	ns
$t_{v(A)}$	Data valid time after address	5			5			5			ns
$t_{en(S)}$	Output enable time from $\overline{S}$ low	5			5			5			ns
$t_{dis(S)}$	Output disable time from $\overline{S}$ high	0		15	0		20	0		20	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0			0			0			ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		10	0		10	0		15	ns
t_{PU}	Power-up time after chip selection	0			0			0			ns
t_{PD}	Power-down time after chip selection			25			35			45	ns

(3) WRITE CYCLE

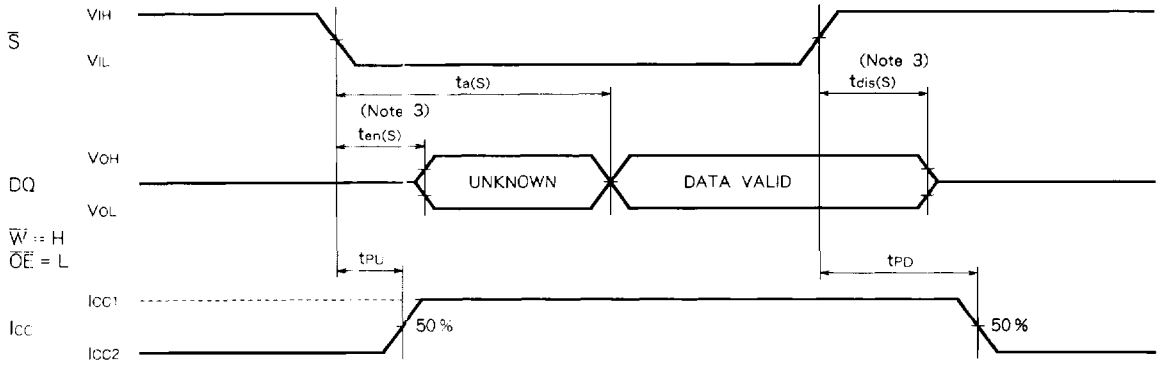
Symbol	Parameter	Limits									Unit
		M5M51004-25,-25L			M5M51004-35,-35L			M5M51004-45,-45L			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{CW}	Write cycle time	25			35			45			ns
$t_{su(S)}$	Chip select set up time	20			30			35			ns
$t_{su(A)}$	Address set up time($\overline{W}$)	0			0			0			ns
$t_{su(A)2}$	Address set up time($\overline{S}$)	0			0			0			ns
$t_{w(W)}$	Write pulse width	20			30			35			ns
$t_{rec(W)}$	Write recovery time	3			3			3			ns
$t_{su(D)}$	Data set up time	15			15			20			ns
$t_{h(D)}$	Data hold time	0			0			0			ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low	0		10	0		15	0		15	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	0			0			0			ns
$t_{su(A\text{-}\overline{W}H)}$	Address to $\overline{W}$ high	20			30			35			ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high	0		10	0		10	0		15	ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	0			0			0			ns

(4) TIMING DIAGRAMS FOR READ CYCLE

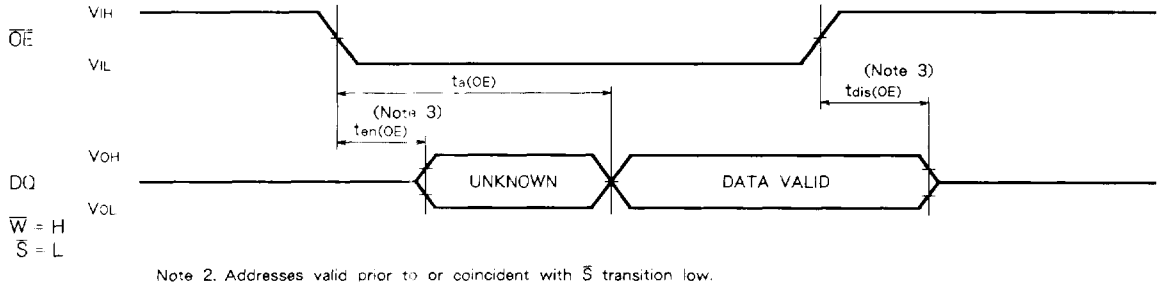
Read cycle 1



Read cycle 2 (Note 2)



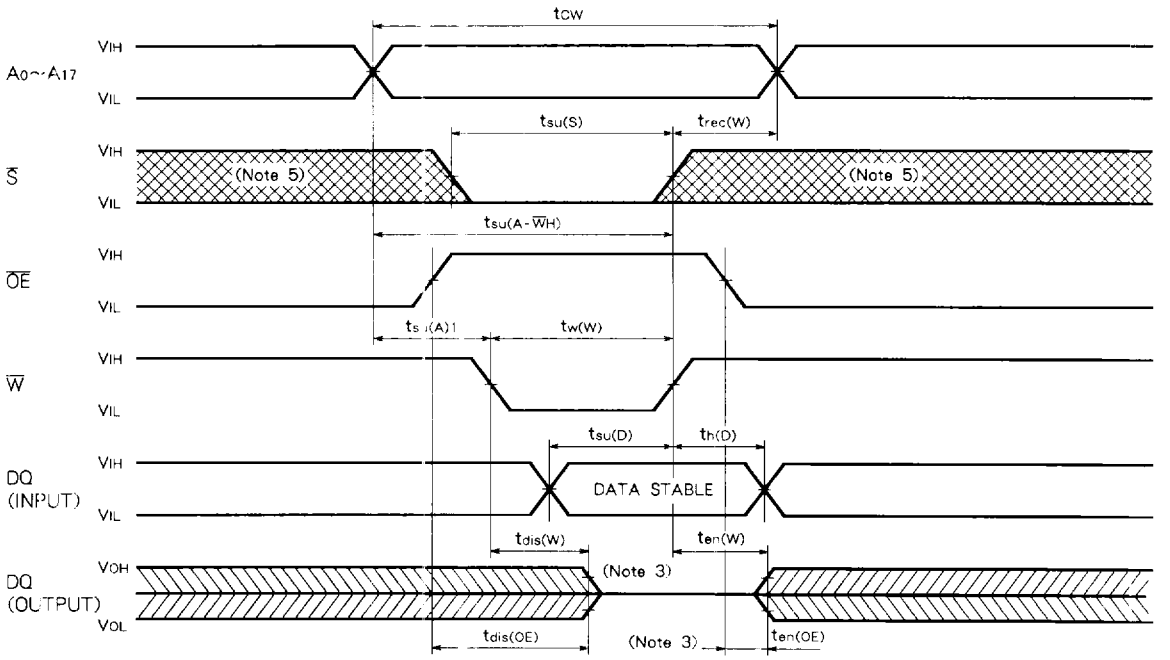
Read cycle 3 (Note 4)



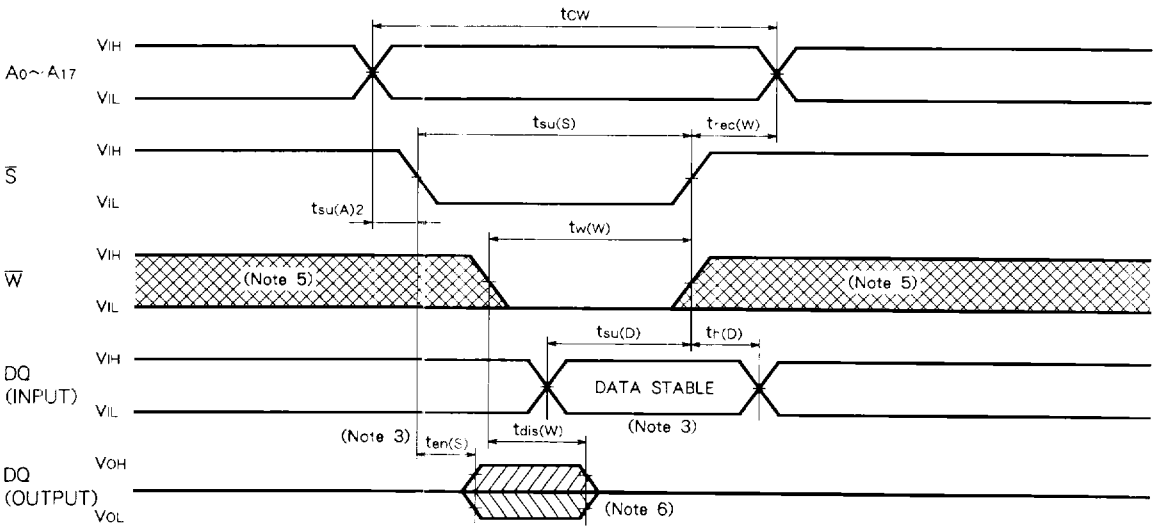
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ±500mV from steady state voltage with specified loading in Fig. 2.
4. Address and $\overline{S}$ valid prior to $\overline{OE}$ transistion low by (ta(A) − ta(OE)),(ta(S) − ta(OE)).

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control)



Write cycle 2 ($\overline{S}$ control)



Note 5. Hatching indicates the states don't care.
6. When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S}$, the outputs are maintained in the high impedance.
* ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS (T_a = 0~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage			2			V
$V_{I(\overline{S})}$	Chip select input voltage	$V_{I(\overline{S})} \geqq V_{CC} - 0.2V$		$V_{CC}-0.2$			V
$t_{su(PD)}$	Power down setup time	$V_I \geqq V_{CC} - 0.2V$ or		0			ns
$t_{rec(PD)}$	Power down recovery time	$0V \leqq V_I \leqq 0.2V$	-25L	25			ns
			-35L	35			
			-45L	45			
$I_{CC(PD)}$	Power down supply current	V_{CC} = 3.0V				50	μA
		V_{CC} = 5.5V				100	

Note 7. This is only M5M51004P, J-25L, -35L, -45L.

TIMING WAVEFORM FOR POWER DOWN