4V Drive Pch MOSFET

UM6J1N

● **Structure**

Silicon P-channel MOSFET

● **Features**

1) Two RSU002P03 transistors in a single UMT package.
2) The MOSFET elements are independent, eliminating mutual interference.
3) Mounting cost and area can be cut in half.

● **Applications**

Switching

● **Packaging specifications**

Type	Package		Taping
	Code		TN
	Basic ordering unit (pieces)		3000
UM6J1N			○

● **Dimensions** (Unit : mm)

UMT6
SOT-363

Each lead has same dimensions
Abbreviated symbol : J01

● **Inner circuit**

(1) Tr1 Source
(2) Tr1 Gate
(3) Tr2 Drain
(4) Tr2 Source
(5) Tr2 Gate
(6) Tr1 Drain

∗1 ESD PROTECTION DIODE
∗2 BODY DIODE
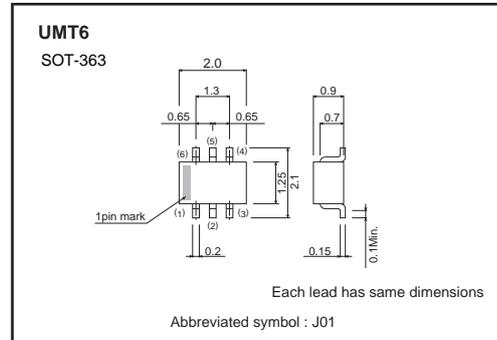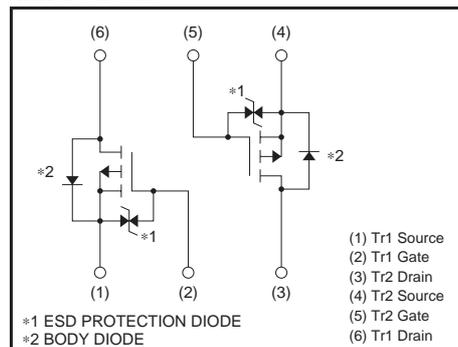
● **Absolute maximum ratings** (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	−30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±0.2	A
	Pulsed	I_{DP} ∗1	±0.4	A
Total power dissipation		P_D ∗2	150	mW / TOTAL
			120	mW / ELEMENT
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

∗1 Pw≤10μs, Duty cycle≤1%
∗2 Each terminal mounted on a recommended land

● **Thermal resistance**

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) ∗	833	°C/W / TOTAL
		1042	°C/W / ELEMENT

∗ Each terminal mounted on a recommended land

●**Electrical characteristics** (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	–30	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –30V, V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	–1.0	–	–2.5	V	V_{DS}= –10V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS(on)}$ *	–	0.9	1.4	Ω	I_D= –0.2A, V_{GS}= –10V
		–	1.4	2.1	Ω	I_D= –0.15A, V_{GS}= –4.5V
		–	1.6	2.4	Ω	I_D= –0.15A, V_{GS}= –4V
Forward transfer admittance	$|Y_{fs}|$ *	0.2	–	–	S	V_{DS}= –10V, I_D= –0.15A
Input capacitance	C_{iss}	–	30	–	pF	V_{DS}= –10V
Output capacitance	C_{oss}	–	4	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	5	–	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$ *	–	8	–	ns	V_{DD}≒ –15V
Rise time	t_r *	–	5	–	ns	I_D= –0.15A
Turn-off delay time	$t_{d(off)}$ *	–	30	–	ns	V_{GS}= –10V R_L≒ 100Ω
Fall time	t_f *	–	40	–	ns	R_G=10Ω

∗ Pulsed

●**Body diode characteristics** (source-drain)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	I_S= –0.1A, V_{GS}=0V

∗Pulsed

●**Electrical characteristic curves**
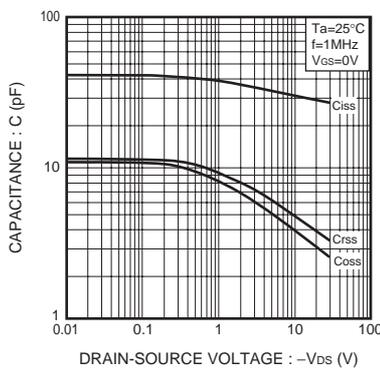
Fig.1 Typical Capacitance vs. Drain-Source Voltage
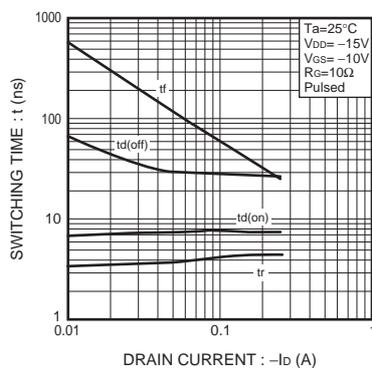
Fig.2 Switching Characteristics
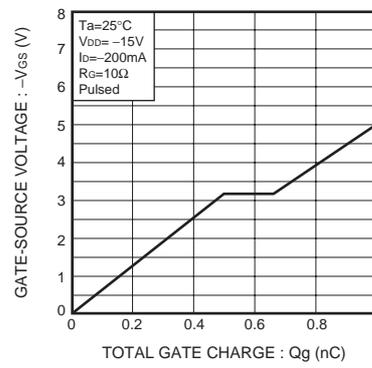
Fig.3 Dynamic Input Characteristics
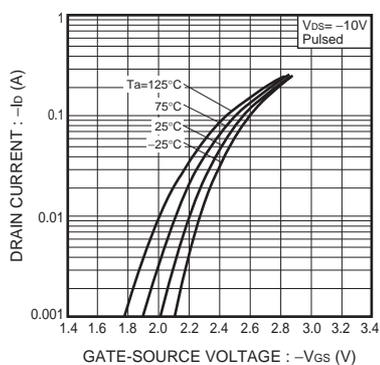
Fig.4 Typical Transfer Characteristics
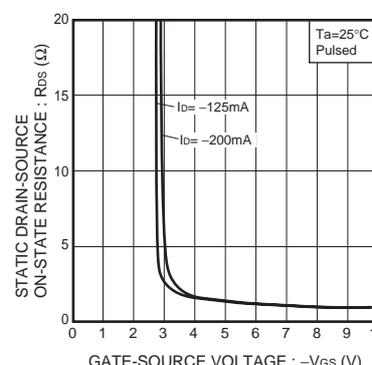
Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage
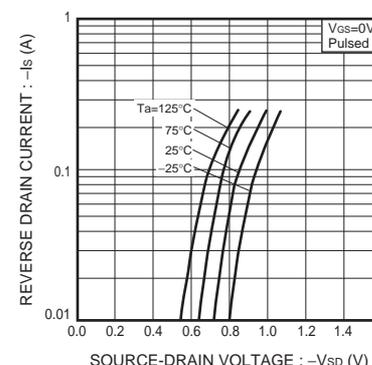
Fig.6 Reverse Drain Current vs. Source-Drain Voltage
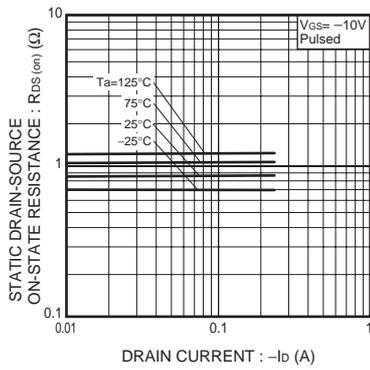
Fig.7 Static Drain-Source
On-State Resistance
vs. Drain Current (Ⅰ)
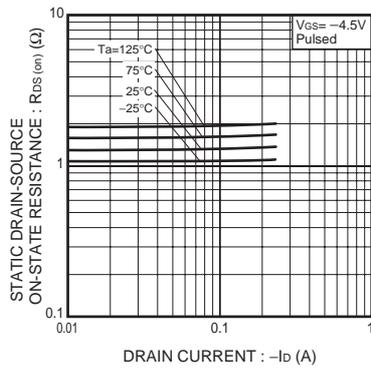
Fig.8 Static Drain-Source
On-State Resistance
vs. Drain Current (Ⅱ)
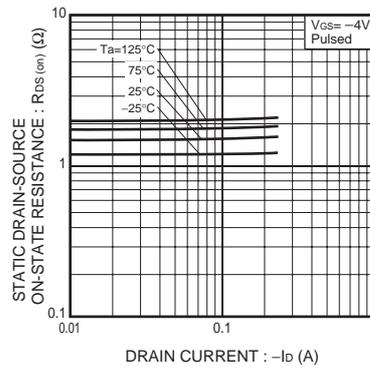
Fig.9 Static Drain-Source
On-State Resistance
vs. Drain Current (Ⅲ)
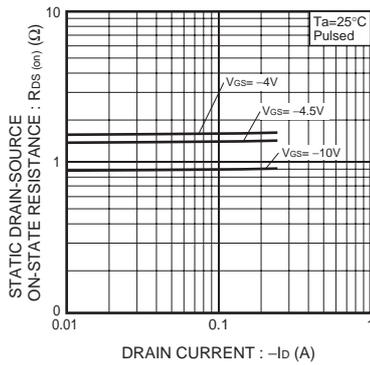
Fig.10 Static Drain-Source
On-State Resistance
vs. Drain Current (Ⅳ)

●**Notice**

This product might cause chip aging and breakdown under the large electrified environment.

Please consider to design ESD protection circuit.

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