FUJITSU
MICROELECTRONICS, INC.

MB8418-20
MB8418-20L

MB8418

CMOS 16,384-BIT STATIC RANDOM ACCESS MEMORY

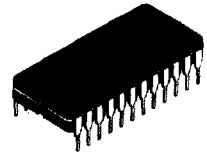
8418LCC

DESCRIPTION

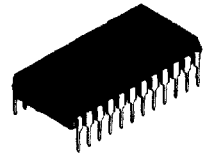
The Fujitsu MB8418 is a 2048 word by 8-bit static random access memory fabricated with high density, high reliability Complementary MOS silicon-gate technology.

The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All input and output pins are TTL-compatible, and a single 5 volt power supply is used. It is possible to retain data at low power supply voltage.

The MB8418 can be optimized for high performance applications such as microcomputer systems where fast access time and ease of use are required. Two Chip Enables ($\overline{E}_2$ and $\overline{E}_1$) permit the selection of an individual device when the outputs are OR-tied. $\overline{E}_2$ controls minimum power consumption. The MB8418 is packaged in an industry standard 24-pin dual in-line package, or 32-pin leadless chip carrier.



CERDIP PACKAGE
DIP-24C-C03



PLASTIC PACKAGE
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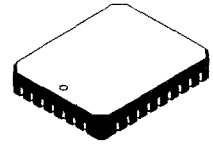
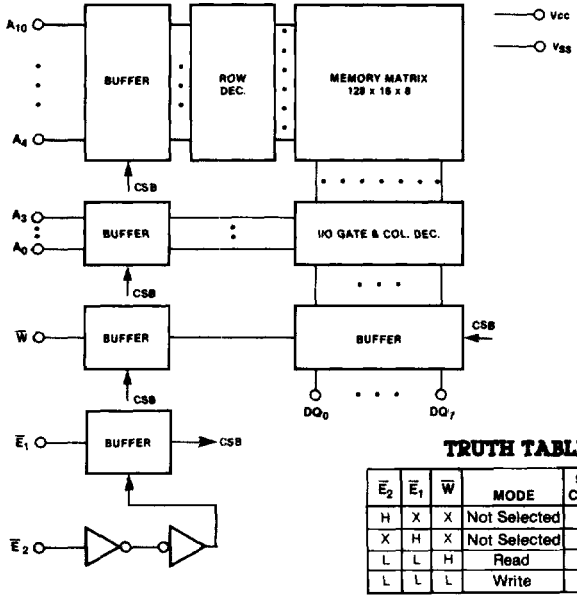


LEADLESS CHIP CARRIER
LCC-32-A02

FEATURES

- **Extended temperature range:**
  MB8418-20: −40°C to +85°C
  MB8418-20L: −40°C to +70°C
- **Organized as 2048 words by 8-bits**
- **Fast Access Time: 200 ns Max.**
- **Low Standby Power:**
  MB8418-20: 55μW
  MB8418-20L: 5.5μW
- **Completely Static Operation, no clocks required**
- **Single +5 Volt Power Supply**
- **TTL Compatible Inputs/Outputs**
- **Low Data Retention Voltage: 2.0V Min.**
- **Pin compatible with HM6116, TC5517 and μPD446**

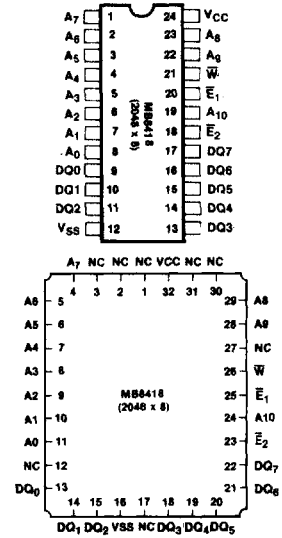
MB8418 BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}_2$	$\overline{E}_1$	$\overline{W}$	MODE	SUPPLY CURRENT	I/O PIN
H	X	X	Not Selected	I_{SB}	High-Z
X	H	X	Not Selected	I_{SB}	High-Z
L	L	H	Read	I_{CC}	D_{OUT}
L	L	L	Write	I_{CC}	D_{IN}

PIN ASSIGNMENTS



8418LCC

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit
Storage Temperature	Cerdip	T_{stg}	−65	150	°C
	Plastic		−40	125	
Temperature Under Bias		T_{bias}	−40	85	°C
Supply Voltage		V_{CC}	−0.5	8.0	V
Input Voltage		V_{IN}	−0.5	V_{CC} + 0.5	V
Input/Output Voltage		$V_{I/O}$	−0.5	V_{CC} + 0.5	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit.

RECOMMENDED OPERATING CONDITIONS, (Referenced to V_{SS} = GND)

Parameter	Symbol		MB8418 Min	MB8418 Typ	MB8418 Max	Unit
Ambient Temperature	T_A	MB8418-20L	−40	—	+70	°C
		MB8418-20	−40	—	+85	
Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		−0.3	—	0.8	V

CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Condition
Input Capacitance	C_{IN}	—	7	pF	V_{IN} = 0V
Input / Output Capacitance	$C_{I/O}$	—	10	pF	$V_{I/O}$ = 0V

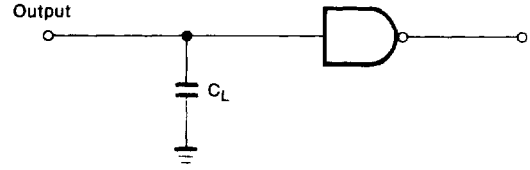
STATIC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Condition	Symbol		Min	Max	Units
Standby Supply Current	$\overline{E}_2 = V_{CC} \pm 0.2$ OR $E_1 = V_{CC} + 0.2V$ and $\overline{E}_2 = V_{SS} \pm 0.2V$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB1}	MB8418-20L	—	1	μA
			MB8418-20	—	10	
Standby Supply Current	$\overline{E}_2$ or $E_1 = V_{IH}$ $V_{IN} = -0.2V$ to $V_{CC} + 0.2V$	I_{SB2}		—	2	mA
Active Supply Current	$\overline{E}_2 = V_{IL}$ $V_{IN} = V_{IL}$ or V_{IH}; $I_{OUT} = 0$	I_{CC1}		—	60	mA
Operating Supply Current	Cycle = Min, Duty = 100% $I_{OUT} = 0$	I_{CC2}		—	60	mA
Input Leakage Current	V_{IN} = 0V to V_{CC}	I_{LI}		−1.0	1.0	μA
Output Leakage Current	$V_{I/O}$ = 0V to V_{CC} $\overline{E}_2 = V_{IH}$ or $E_1 = V_{IH}$	I_{LO}		−1.0	1.0	μA
Output High Voltage	I_{OUT} = −1.0 mA	V_{OH}		2.4	—	V
Output Low Voltage	I_{OUT} = 4.0 mA	V_{OL}		—	0.4	V

AC TEST CONDITIONS

Input Pulse Levels:	**0.6V to 2.4V**
Input Pulse Rise and Fall Times:	**10 ns (0.8V to 2.2 V)**
Input Timing Reference Level:	**0.8V to 2.2V**
Output Timing Reference Level:	**0.8V to 2.2V**
Output Load:	**1 TTL Gate and**
	C_L = 5 pF for TEHQZ and TWHQZ
	C_L = 100 pF for all others.



DYNAMIC CHARACTERISTICS

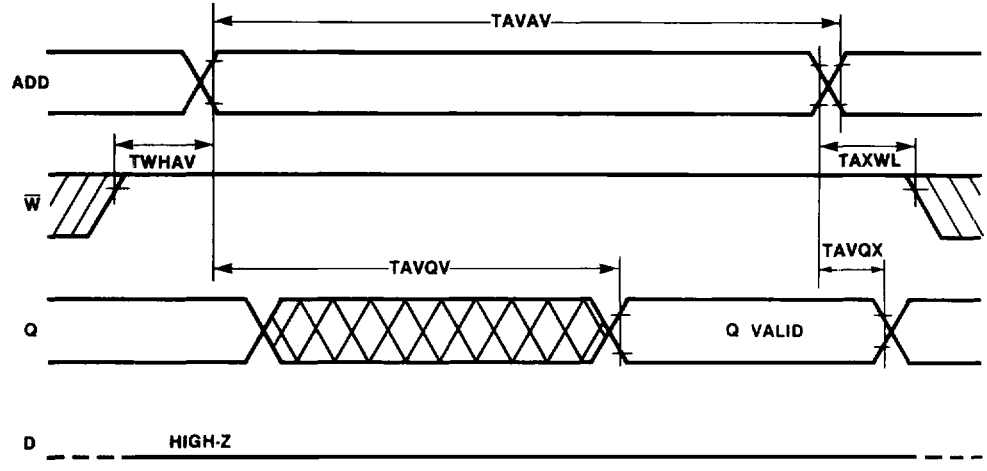
R26

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	TAVAV	200	—	ns
Write Cycle Time	TAVAV	200	—	ns
Address Access Time	TAVQV	—	200	ns
Chip Enable Access Time	TELQV	—	200	ns
Output Hold from Address Change	TAVQX	15	—	ns
Output Low Z from $\overline{E}_2$ or $\overline{E}_1$	TELQX	15	—	ns
Output High Z from $\overline{E}_2$ or $\overline{E}_1$	TEHQZ	—	60	ns
Output Low Z from $\overline{W}$	TWHQV	15	—	ns
Output High Z from $\overline{W}$	TWLQZ	—	60	ns
Address Set Up Time	TAVEL, TAVWL	0	—	ns
Read Set Up Time	TWHEL, TWHAV	0	—	ns
Read Hold Time	TAXWL, TEHWL	0	—	ns
Write Set Up Time	TWLEL	0	—	ns
Write Hold Time	TEHWH	0	—	ns
Address Valid to End of Write	TAVWH	160	—	ns
Chip Enable to End of Write	TELEH	160	—	ns
Write Pulse Width	TWLWH	140	—	ns
Write Recovery Time	TWHAX, TEHAX	10	—	ns
Data Set Up Time	TDVEH, TDVWH	60	—	ns
Data Hold Time	TWHDX, TEHDX	0	—	ns

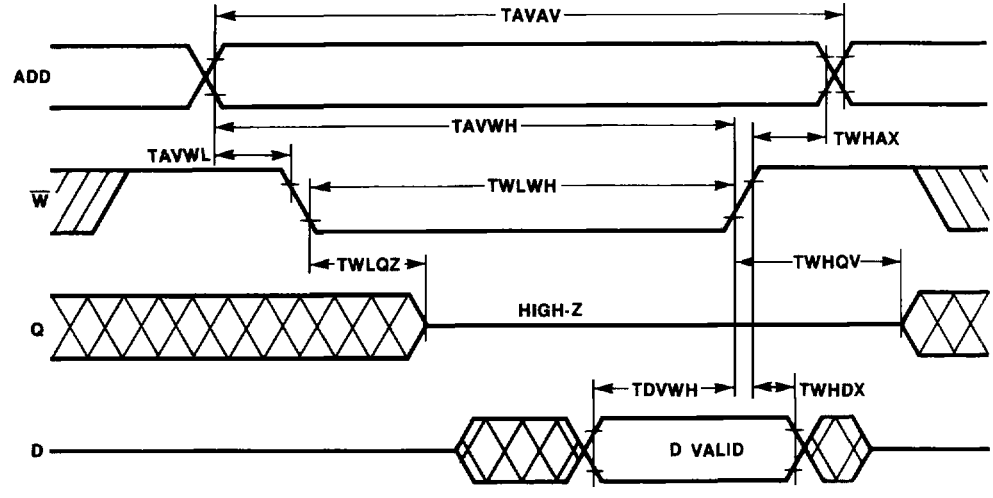
WAVEFORMS

MODE 1: W Controlled: ($\overline{E}_2 = \overline{E}_1 = LOW$)

Read Cycle



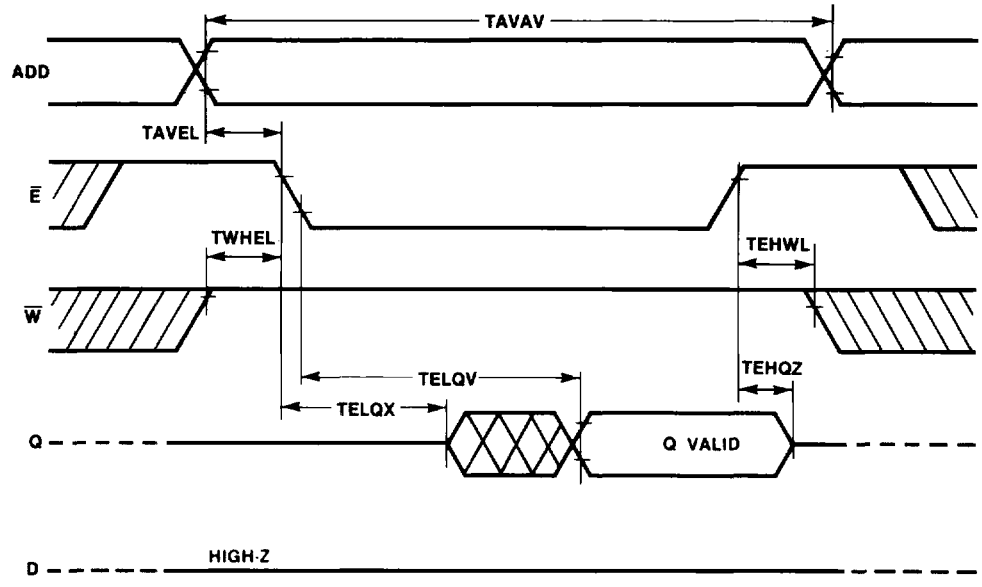
Write Cycle



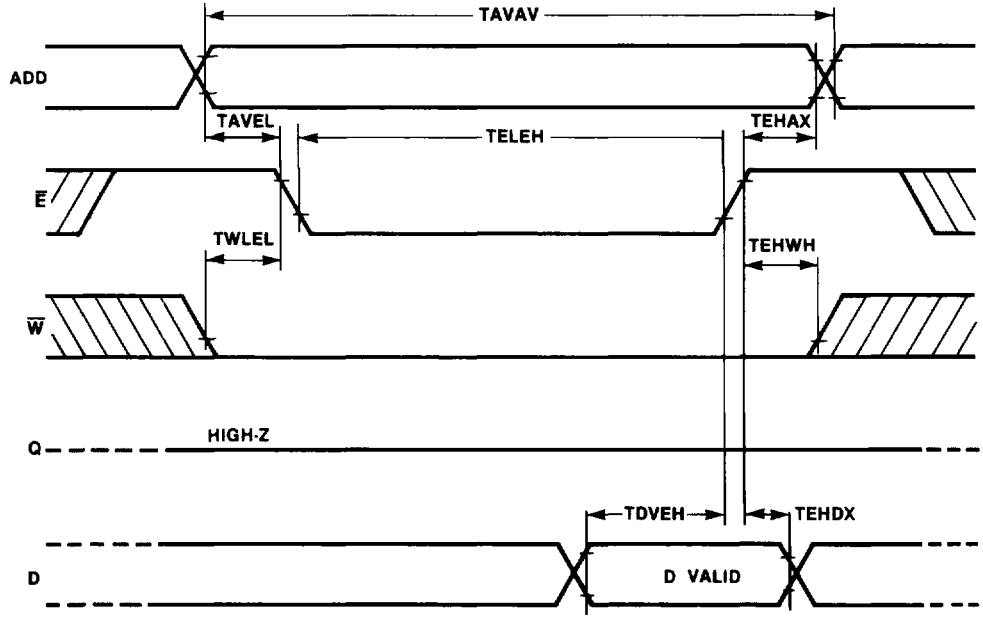
WAVEFORMS (Continued)

MODE 2: $\overline{E}_2$ or $\overline{E}_1$ Controlled ($\overline{E}_2$ = Low or $\overline{E}_1$ = Low)

Read Cycle



Write Cycle



DYNAMIC CHARACTERISTICS

Data Retention Characteristics, NOTES [1, 2, 3] (Recommended operating conditions unless otherwise noted.)

Parameter	Notes	Symbol		Min	Max	Unit
Data Retention Supply Voltage	[1]	VDR		2.0	5.5	V
Data Retention Supply Current	[2]	IDR	MB8418-20	—	10	μA
			MB8418-20L	—	1	μA
Data Retention Set Up Time	[3]	TEHVCL		60	—	ns
Recovery Time	[3]	TVHEL		60	—	ns

Notes:

[1] $\overline{E}_2 = 2.2V$ to $V_{CC} \pm 0.3V$ for VDR = 2.5V to 5.5V
$\overline{E}_2 = V_{CC} \pm 0.3V$ for VDR = 2.0 to 2.5V.

[2] $V_{CC} = V_{DR}$, $\overline{E}_2 = V_{DR} - 0.2V$ to $V_{DR} + 0.2V$, $V_{IN} = -0.2V$ to $V_{DR} + 0.2V$.

[3] $V_L = 4.5V$ on the falling transition, $V_H = 4.5V$ on the rising transition.