DATA SHEET

74LVC157
Quad 2-input multiplexer

Product specification
Supersedes data of February 1996
IC24 Data Handbook

1997 Mar 18

Philips
Semiconductors

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Quad 2-input multiplexer 74LVC157

FEATURES

- Wide supply voltage range of 1.2 to 3.6 V
- In accordance with JEDEC standard no. 8-1A
- Inputs accept voltages up to 5.5 V
- CMOS lower power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 85°C
- Non-inverting data path

DESCRIPTION

The 74LVC157 is a high-performance, low-power, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

The 74LVC157 is a quad 2-input multiplexer which select 4 bits of data from two sources under the control of a common data select input (S). The four outputs present the selected data in the true (non-inverted) form. The enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (1Y to 4Y) are forced LOW regardless of all other input conditions. Moving the data from two groups of registers to four common output buses is a common use of the 74LV157. The state of the common data select input (S) determines the particular register from which the data comes. It can also be used as function generator.

The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The 74LVC157 is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S.

The 74LVC157 is identical to the the 74LVC158 but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; $t_r = t_f \leq$ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay nI_0, nI, to nY $\overline{E}$ to nY S to nY	C_L = 50 pF; V_{CC} = 3.3 V	4.2 3.8 4.7	ns
C_I	Input capacitance		5.0	pF
C_{PD}	Power dissipation capacitance per gate	V_I = GND to V_{CC}[1]	30	pF

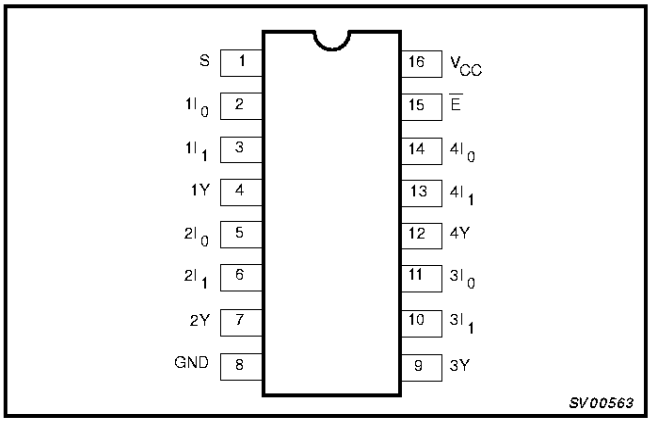
NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW)
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic SO	−40°C to +85°C	74LVC157 D	74LVC157 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +85°C	74LVC157 DB	74LVC157 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +85°C	74LVC157 PW	74LVC157PW DH	SOT403-1

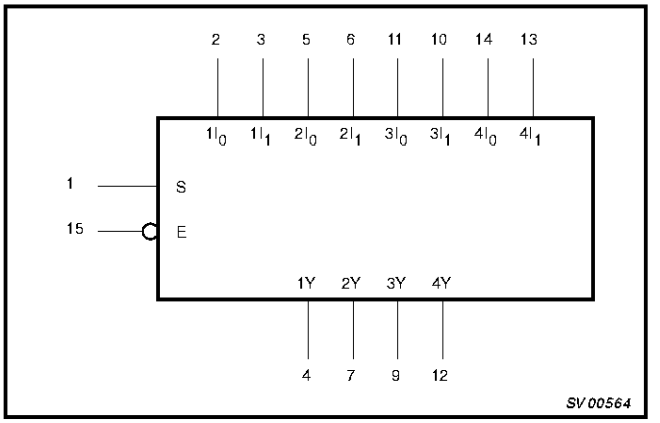
PIN CONFIGURATION



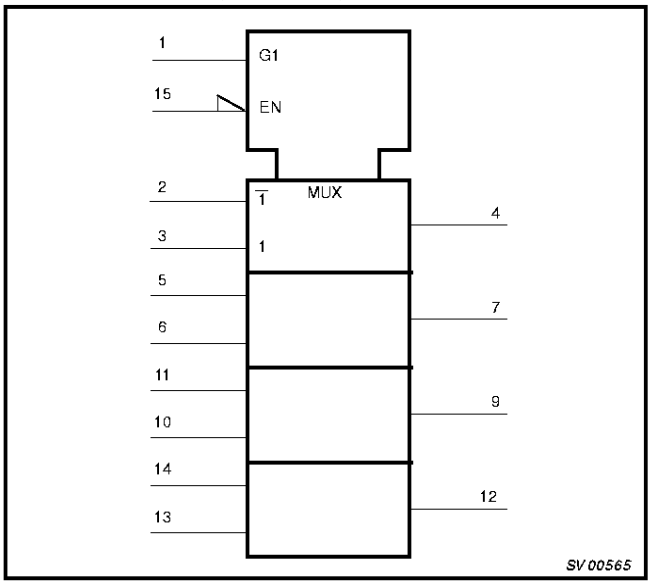
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	S	Common data select input
2, 5, 11, 14	$1I_0$ to $4I_0$	Data inputs from source 0
3, 6, 10, 13	$1I_1$ to $4I_1$	Data inputs from source 1
4, 7, 9, 12	1Y to 4Y	Multiplexer outputs
8	GND	Ground (0 V)
15	$\overline{E}$	Enable inputs (active LOW)
16	V_{CC}	Positive supply voltage

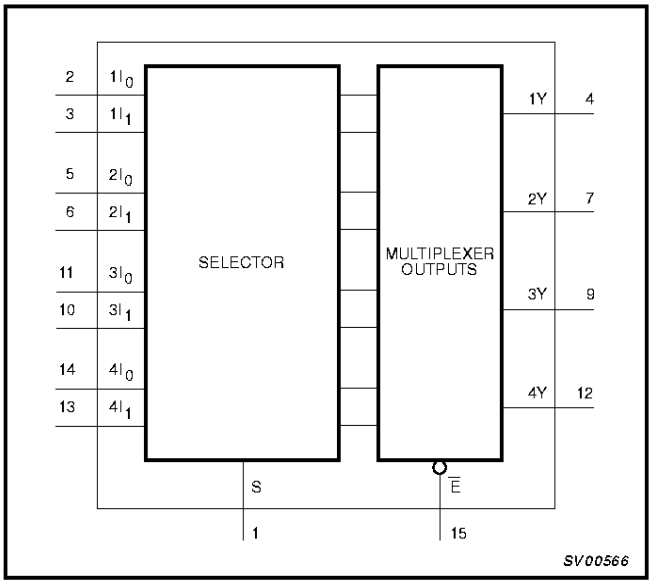
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



FUNCTIONAL DIAGRAM

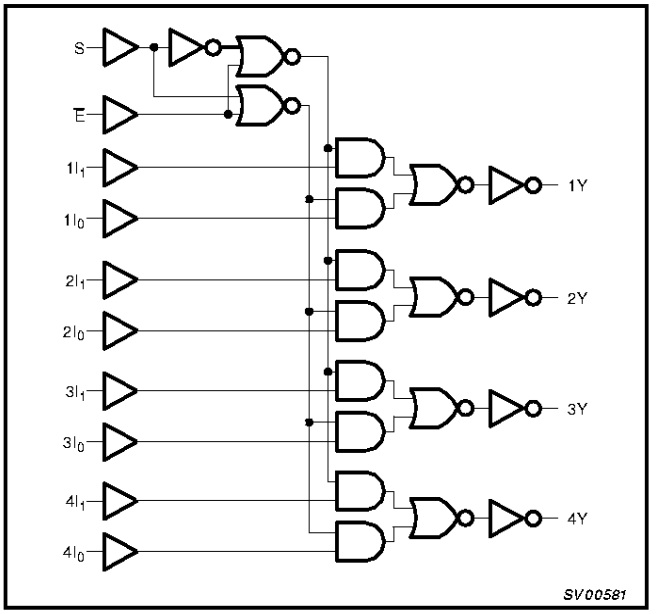


FUNCTION TABLE

INPUTS				OUTPUTS
$\overline{E}$	S	nI_0	nI_1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = don't care

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage (for max. speed performance)		2.7	3.6	V
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input voltage range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.2 to 2.7V V_{CC} = 2.7 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +6.5	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	Note 2	–0.5 to +5.5	V
$V_{I/O}$	DC input voltage range for I/Os		–0.5 to V_{CC} +0.5	V
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_{OUT}	DC output voltage	Note 2	–0.5 to V_{CC} +0.5	V
I_{OUT}	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–60 to +150	°C
P_{TOT}	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	 above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	 500 500	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V		V_{CC}			V
		V_{CC} = 2.7 to 3.6V		2.0			
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V				GND	V
		V_{CC} = 2.7 to 3.6V				0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA		V_{CC} − 0.5			V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −100µA		V_{CC} − 0.2	V_{CC}		
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −12mA		V_{CC} − 0.6			
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = −24mA		V_{CC} − 1.0			
V_{OL}	LOW level output voltage	V_{CC} = 2.7V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA				0.40	V
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA			GND	0.20	
		V_{CC} = 3.0V; $V_I = V_{IH}$ or V_{IL}; I_O = 24mA				0.55	
I_I	Input leakage current	V_{CC} = 3.6V; V_I = 5.5V or GND	Not for I/O pins		±0.1	±5	µA
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND			±0.1	±15	µA
I_{OZ}	3-State output OFF-state current	V_{CC} = 3.6V; $V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND			0.1	±10	µA
I_{CC}	Quiescent supply current	V_{CC} = 3.6V; $V_I = V_{CC}$ or GND; I_O = 0			0.1	20	µA
ΔI_{CC}	Additional quiescent supply current per input pin	V_{CC} = 2.7V to 3.6V; $V_I = V_{CC}$ −0.6V; I_O = 0			5	500	µA

NOTE:

1. All typical values are measured at V_{CC} = 3.3V and T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\Omega$; $T_{amb} = -40°C$ to $+85°C$

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V			V_{CC} = 1.2V	
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	TYP	
t_{PHL}/t_{PLH}	Propagation delay nI_0 to nY; nI_1 to nY	Figure 1, 3		4.2	7.5		5.0	8.5		ns
t_{PHL}/t_{PLH}	Propagation delay $\overline{E}$ to nY	Figure 2, 3		3.8	7.5		4.5	8.5		ns
t_{PHL}/t_{PLH}	Propagation delay S to nY	Figure 1, 3		4.7	8.5		5.5	9.5		ns

NOTE:
1. These typical values are at $V_{CC} = 3.3$V and $T_{amb} = 25°C$.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V
$V_M = 0.5 \bullet V_{CC}$ at $V_{CC} < 2.7$ V
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

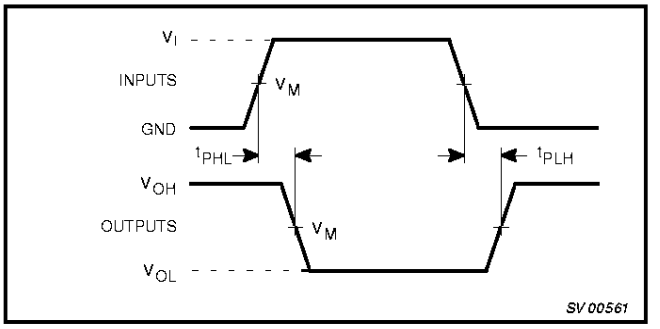


Figure 1. Enable input ($\overline{E}$) to output (nY) propagation delays.

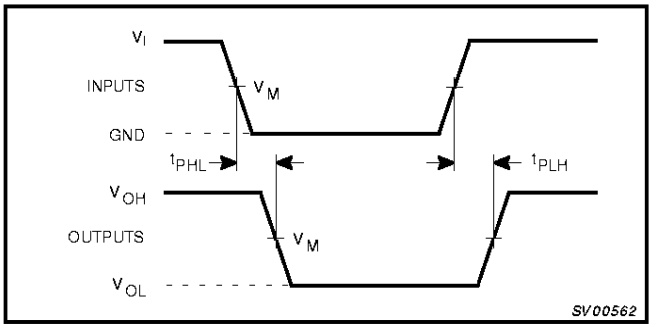


Figure 2. Data inputs (nI_0, nI_1) and common data select input (S) to output (nY) propagation delays.

TEST CIRCUIT

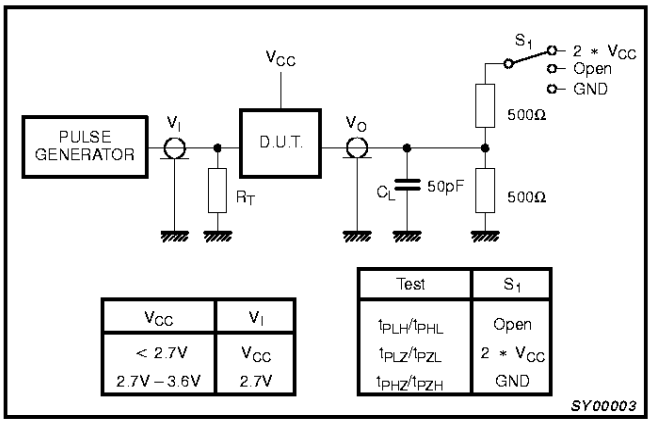
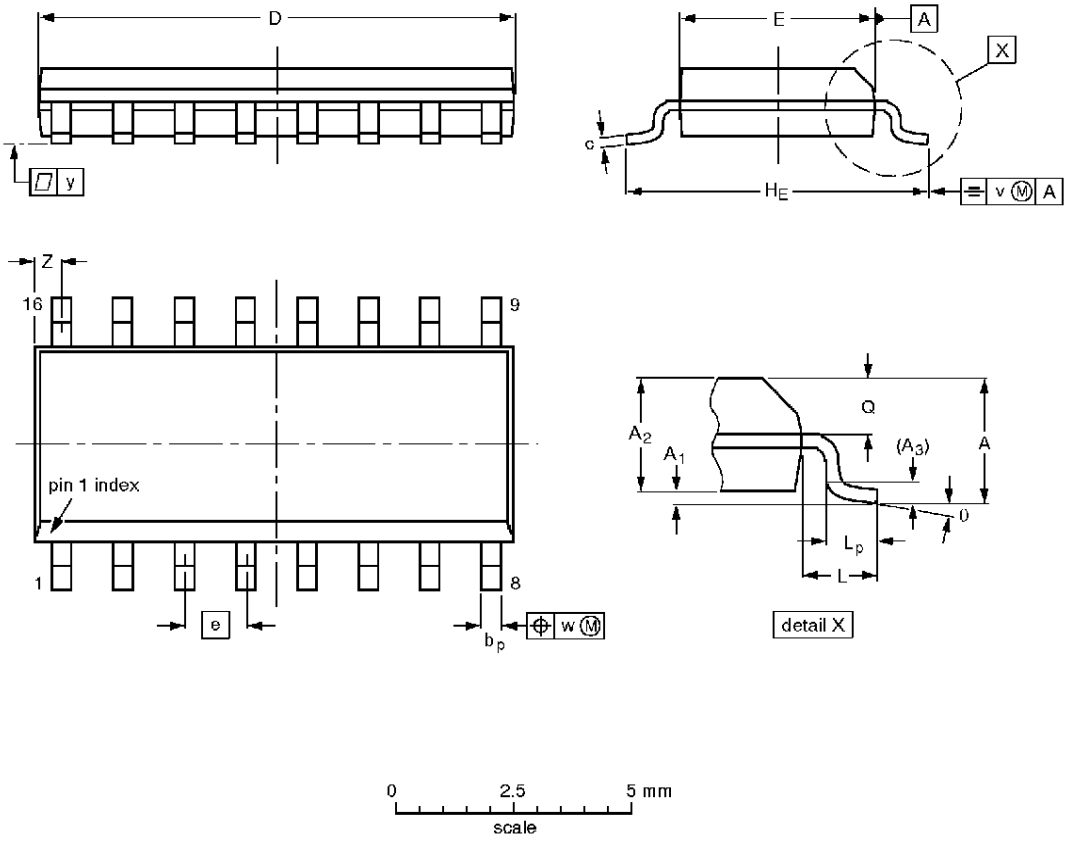


Figure 3. Load circuitry for switching times.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

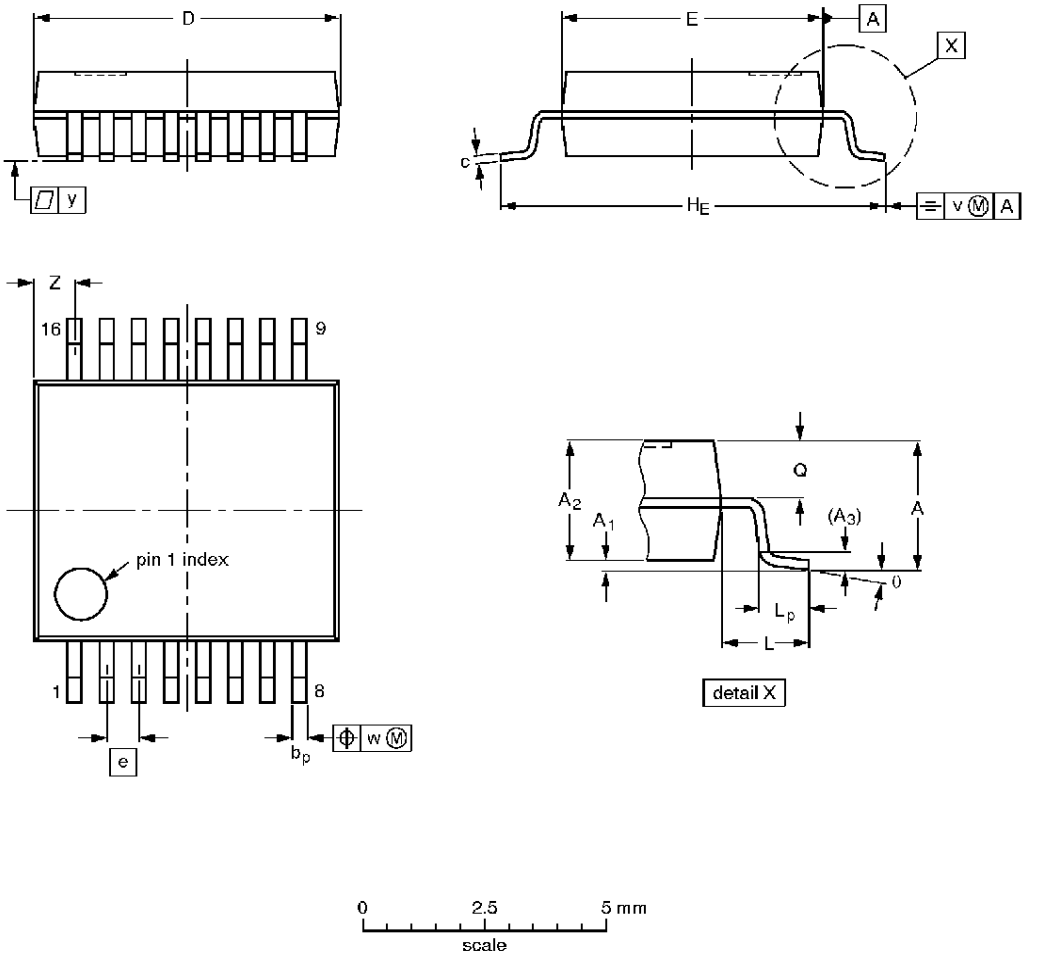
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

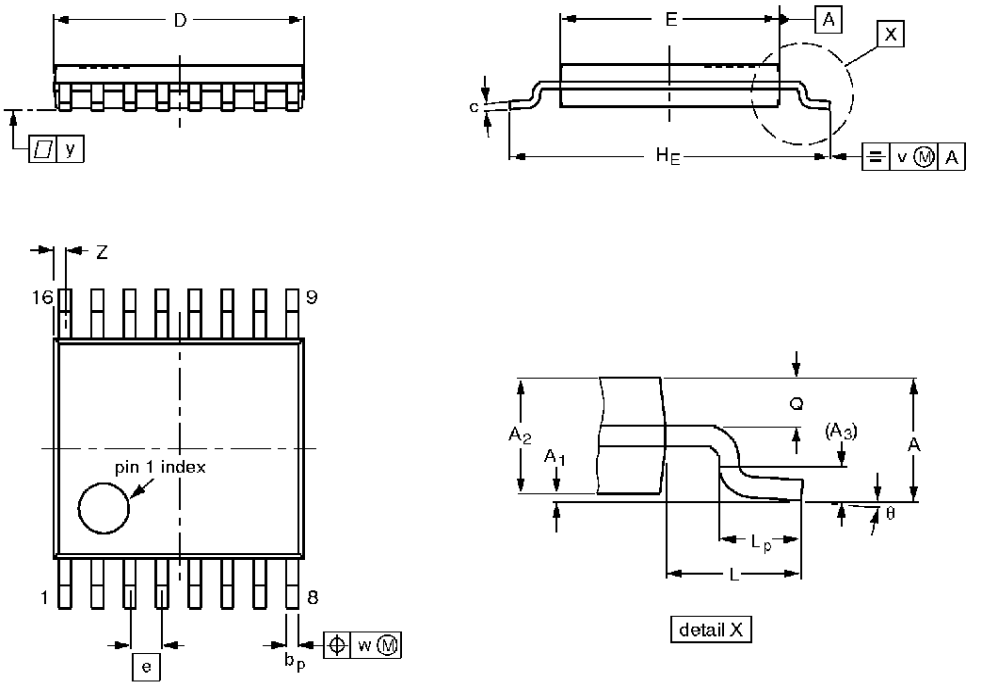
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

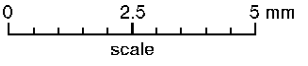
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or in Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088–3409
Telephone 800-234-7381

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