TC74LCX652FW

(TENTATIVE)

LOW VOLTAGE OCTAL BUS TRANSCEIVER / REGISTER WITH 5V TOLERANT INPUTS AND OUTPUTS

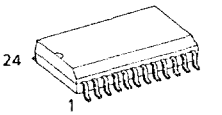
The TC74LCX652 is a high parformance CMOS OCTAL BUS TRANSCEIVER/REGISTER. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

This device is bus transceiver with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the internal registers. All inputs are equipped with protection circuits against static discharge.

FEATURES :

- Low Voltage Operation : V_{CC} = 2.0~3.6V
- High Speed Operation : t_{pd} = ns(max.) at V_{CC} = 3.0~3.6V
- Output Current : $|I_{OH}| / I_{OL}$ = 24mA(min.) at V_{CC} = 3.0V
- Latch-up Performance : ±300mA
- ESD Performance : ±2000V (Human Body Model)
  : ±200V (Machine Model)
- Available in JEDEC SOP
- Bidirectional interface between 5V and 3.3V signals.
- Power Down Protection is provided on all inputs and outputs.
- Pin and Function Compatible with the 74 series (74AC/HC/F/ALS/LS etc.) 652 type.

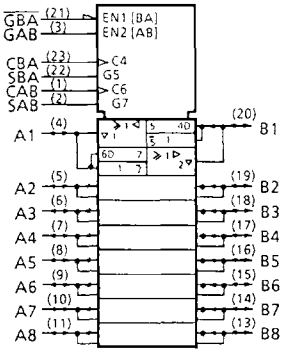


FW (SOL24-P-300)
Weitht : 0.57g (TYP.)

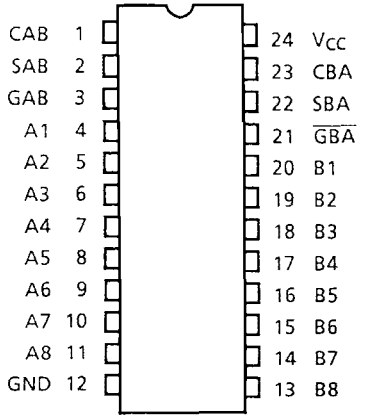
APPLICATION NOTES

1) Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.
2) All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

IEC LOGIC SYMBOL



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

GAB	$\overline{GBA}$	CAB	CBA	SAB	SBA	A	B	Function
L	H	X*	X*	X	X	INPUTS Z	INPUTS Z	The output functions of A and B Busses are disabled.
		↓	↓	X	X	X	X	Both A and B Busses are used as inputs to the internal flip-flops. Data on the Bus will be stored on the rising edge of the Clock.
H	H	X*	X*	L	X	INPUTS L H	OUTPUTS L H	The data on the A bus are displayed on the B bus.
		↓	X*	L	X	L H	L H	The data on the A bus are displayed on the B Bus, and are stored into the A storage flip-flops on the rising edge of CAB.
		X*	X*	H	X	X	Qn	The data in the A storage flop-flops are displayed on the B Bus.
		↓	X*	H	X	L H	L H	The data on the A Bus are stored into the A storage flip-flops on the rising edge of CAB, and the stored data propagate directly onto the B Bus.
L	L	X*	X*	X	L	OUTPUTS L H	INPUTS L H	The data on the B Bus are displayed on the A bus.
		X*	↓	X	L	L H	L H	The data on the B Bus are displayed on the A Bus, and are stored into the B storage flip-flops on the rising edge of CBA.
		X*	X*	X	H	Qn	X	The data in the B storage flip-flops are displayed on the A Bus.
		X*	↓	X	H	L H	L H	The data on the B Bus are stored into the B storage flip-flops on the rising edge of CBA, and the stored data propagate directly onto the A Bus.
H	L	X*	X*	H	H	OUTPUTS Qn	OUTPUTS Qn	The data in the A storage flop-flops are displayed on the B Bus, and the data in the B storage flop-flops are displayed on the A.

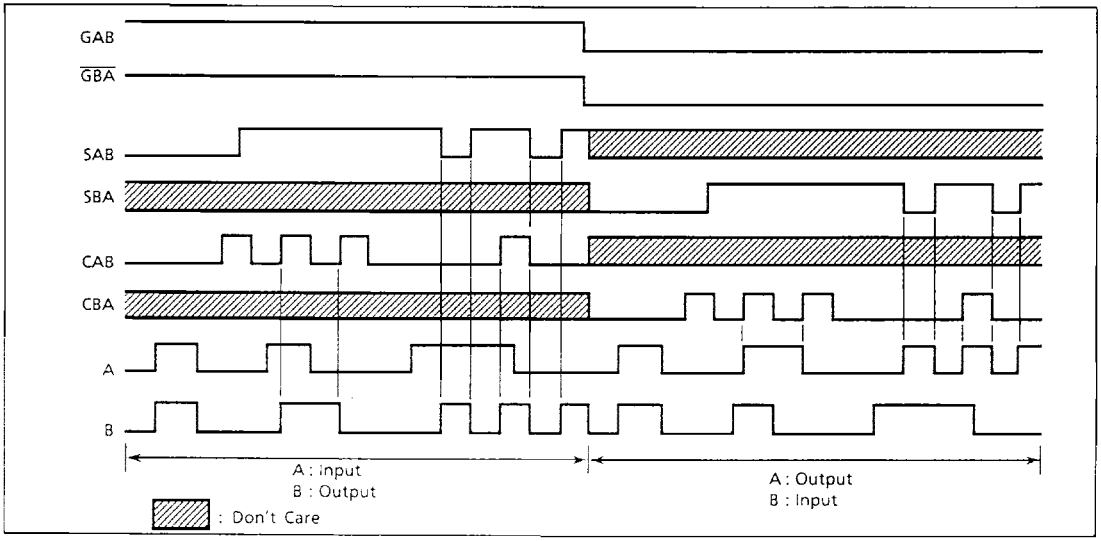
Notes: X: Don't Care

Qn: The data stored into the internal flip-flops by most recent low to high transition of the clock inputs.

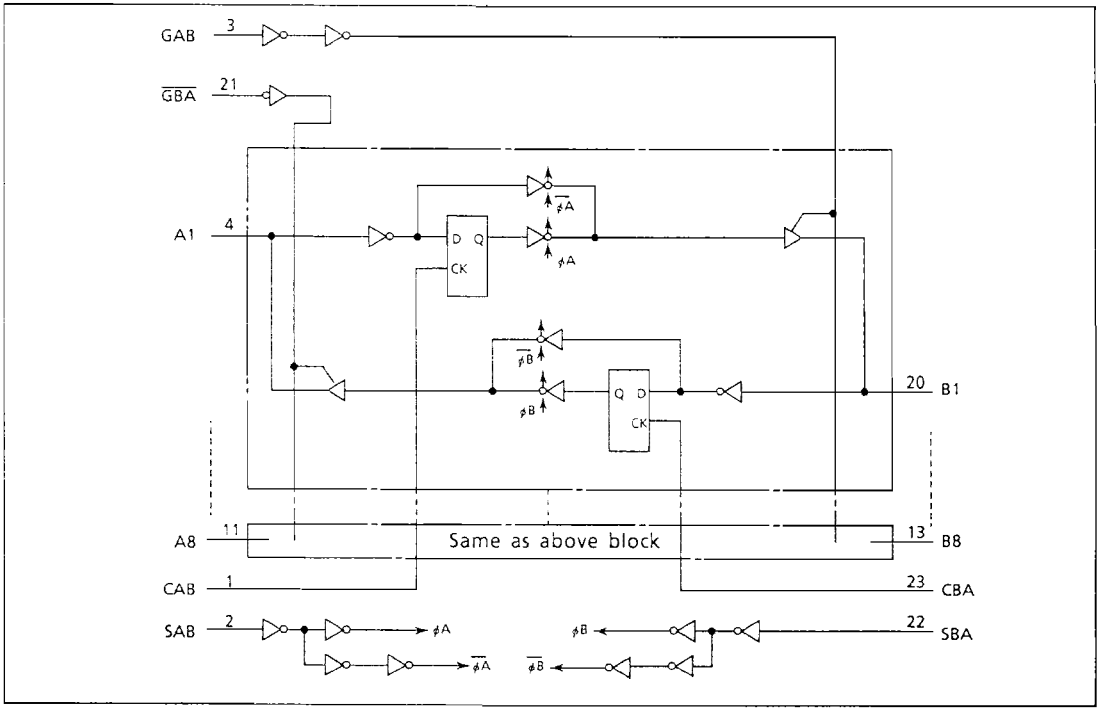
Z: High Impedance

*: The clocks are not internally gated with either GAB or $\overline{GBA}$. Therefore, data on the A and/or B Busses may be clocked into the storage flip-flops at any time.

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~7.0 (Off-State) −0.5~V_{CC}+0.5 (High or Low State)*	V
Input Diode Current	I_{IK}	−50	mA
Output Diode Current	I_{OK}	±50 (V_{OUT}<GND, V_{OUT}>V_{CC})	mA
DC Output Current	I_{OUT}	±50	mA
DC V_{CC}/Ground Current	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

* : I_{OUT} absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~3.6 (Operating) 1.5~3.6 (Data Retention Only)	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~5.5 (Off-State) 0~V_{CC} (High or Low State)	V
Output Current	I_{OH} / I_{OL}	±24 (V_{CC} = 3.0~3.6) ±12 (V_{CC} = 2.7~3.0)	mA
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dV	0~10 (V_{IN} = 0.8~2V, V_{CC} = 3V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = −40~85°C		UNIT
					MIN.	MAX.	
High-Level Input Voltage	V_{IH}			2.7~3.6	2.0	−	V
Low-Level Input Voltage	V_{IL}			2.7~3.6	−	0.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −100μA	2.7~3.6	V_{CC}−0.2	−	V
			I_{OH} = −12mA	2.7	2.2	−	
			I_{OH} = −18mA	3.0	2.4	−	
			I_{OH} = −24mA	3.0	2.2	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100μA	2.7~3.6	−	0.2	V
			I_{OL} = 12mA	2.7	−	0.4	
			I_{OL} = 24mA	3.0	−	0.55	
Input Leakage Current	I_{IN}	V_{IN} = 0~5.5V		2.7~3.6	−	±5.0	μA
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = 0~5.5V		2.7~3.6	−	±5.0	μA
Power Off Leakage Current	I_{OFF}	V_{IN} / V_{OUT} = 5.5V (per Pin)		0	−	100	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		2.7~3.6	−	10.0	μA
		V_{IN} / V_{OUT} = 3.6~5.5V		2.7~3.6	−	±10.0	
Increase in I_{CC} per Input	ΔI_{CC}	V_{IH} = V_{CC} − 0.6V		2.7~3.6	−	500	μA

TIMING REQUIRNENTS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Minimum Pulse Width	t_w (L) t_w (H)	(Fig. 1, 5)		−		ns
Minimum Set-up Time	t_s	(Fig. 1, 5)		−		ns
Minimum Hold Time	t_h	(Fig. 1, 5)		−		ns

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	Ta = −40~85°C			UNIT
			V_{CC} = 2.7V	V_{CC} = 3.3 ± 0.3V		
			MAX.	MIN.	MAX.	
Propagation Delay Time (An, Bn − Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 2)		1.5		ns
Propagation Delay Time (CAB, CBA − Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 5)		1.5		ns
Propagation Delay Time (SAB, SBA − Bn, An)	t_{pLH} t_{pHL}	(Fig. 1, 2)		1.5		ns
3 − State output Enable Time (GAB, $\overline{GBA}$ − Bn, An)	t_{pZL} t_{pZH}	(Fig. 1, 3, 4)		1.5		ns
3 − State output Disable Time (GAB, $\overline{GBA}$ − Bn, An)	t_{pLZ} t_{pHZ}	(Fig. 1, 3, 4)		1.5		ns
Maximum Clock Frequency	f_{MAX}		−		−	MHz
Output to Output Skew	t_{osLH} t_{osHL}	(Note 1)	−	−	1.0	ns

Note (1) Parameter guaranteed by design. ($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

DYNAMIC SWITCHING CHARACTERISTICS (Input $t_r = t_f = 2.5$ns, $C_L = 50$pF, $R_L = 500\Omega$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C	UNIT
				TYPICAL	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V
Quiet Output Minimum Dynamic V_{OL}	$\|V_{OLV}\|$	V_{IH} = 3.3V, V_{IL} = 0V	3.3	TBD	V

TBD : Actual performance will be noted upon completion of characterization.

CAPACITIVE CHARACTERISTICS

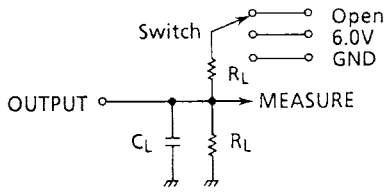
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C TYPICAL	UNIT
Input Capacitance	C_{IN}		3.3	7	pF
Bus Input Capacitance	$C_{I/O}$		3.3	8	pF
Power Dissipation Capacitance	C_{PD}	f_{IN} = 10MHz (Note 1)	3.3		pF

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC}(opr.) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per bit)}$$

TEST CIRCUIT

Fig. 1



C_L = 50pF
R_L = 500Ω

Parameter	Switch
tpLH, tpHL	Open
tpLZ, tpZL	6.0V
tpHZ, tpZH	GND
tw, ts, th	Open

AC WAVEFORM

Fig. 2 (tpLH, tpHL)

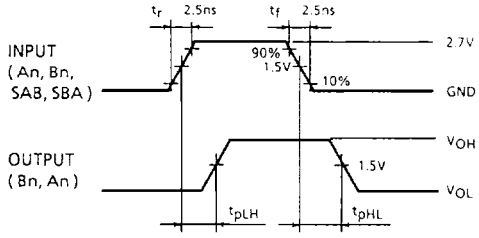


Fig. 3 (tpLZ, tpHZ, tpZL, tpZH)

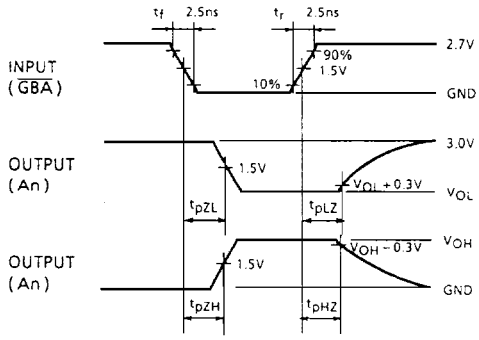


Fig. 4 (tpLZ, tpHZ, tpZL, tpZH)

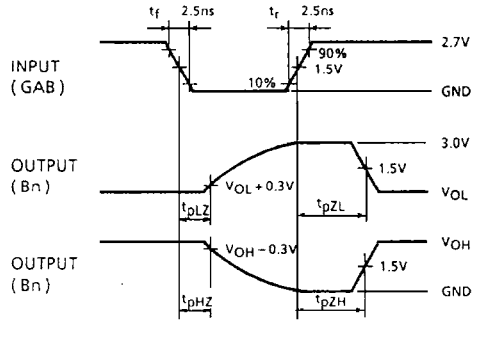


Fig. 5 (tpLH, tpHL, tw, ts, th)