

(Rev. 3.0)

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER-PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMs, fabricated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

## FEATURES

Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V16165BXX-6,6S	60	15	30	15	104	285
M5M4V16165BXX-7,7S	70	20	35	20	124	255
M5M4V16165BXX-8,8S	80	20	40	20	144	225

XX=J,TP

- Standard 42 pin SOJ, 50 pin TSOP
- Single 3.3V  $\pm 0.3V$  supply
- Low stand-by power dissipation  
1.8mW (Max) ..... CMOS Input level
- Low operating power dissipation  
M5M4V16165Bxx- 6,6S..... 345.0mW (Max)  
M5M4V16165Bxx- 7,7S..... 310.0mW (Max)  
M5M4V16165Bxx- 8,8S..... 270.0mW (Max)
- Hyper-page mode, Read-modify-write, RAS-only refresh  
CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance  
All inputs, output TTL compatible and low capacitance
- 4096 refresh cycles every 64ms (A0 ~ A11)

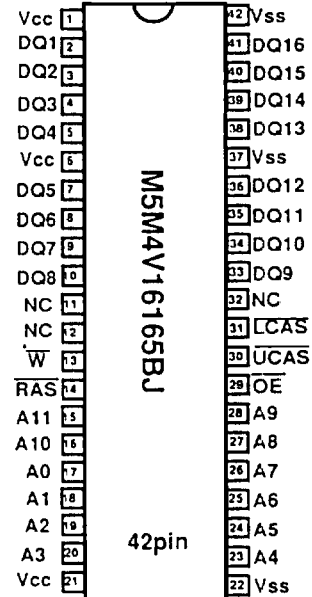
## APPLICATION

Main memory unit for computers, Microcomputer memory,  
Refresh memory for CRT

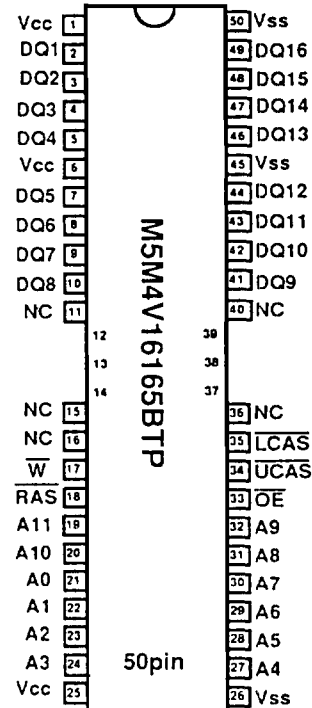
## PIN DESCRIPTION

Pin Name	Function
A0-A11	Address Inputs
DQ1-DQ16	Data Inputs / Outputs
RAS	Row Address Strobe Input
UCAS	Upper Bite Control Column Address Strobe Input
LCAS	Lower Bite Control Column Address Strobe Input
W	Write Control Input
OE	Output Enable Input
Vcc	Power Supply (+3.3V)
Vss	Ground (0V)

## PIN CONFIGURATION (TOP VIEW)



Outline 42P0K (400mil SOJ)



Outline 50P3W-L (400mil TSOP Normal Bend)

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## FUNCTION

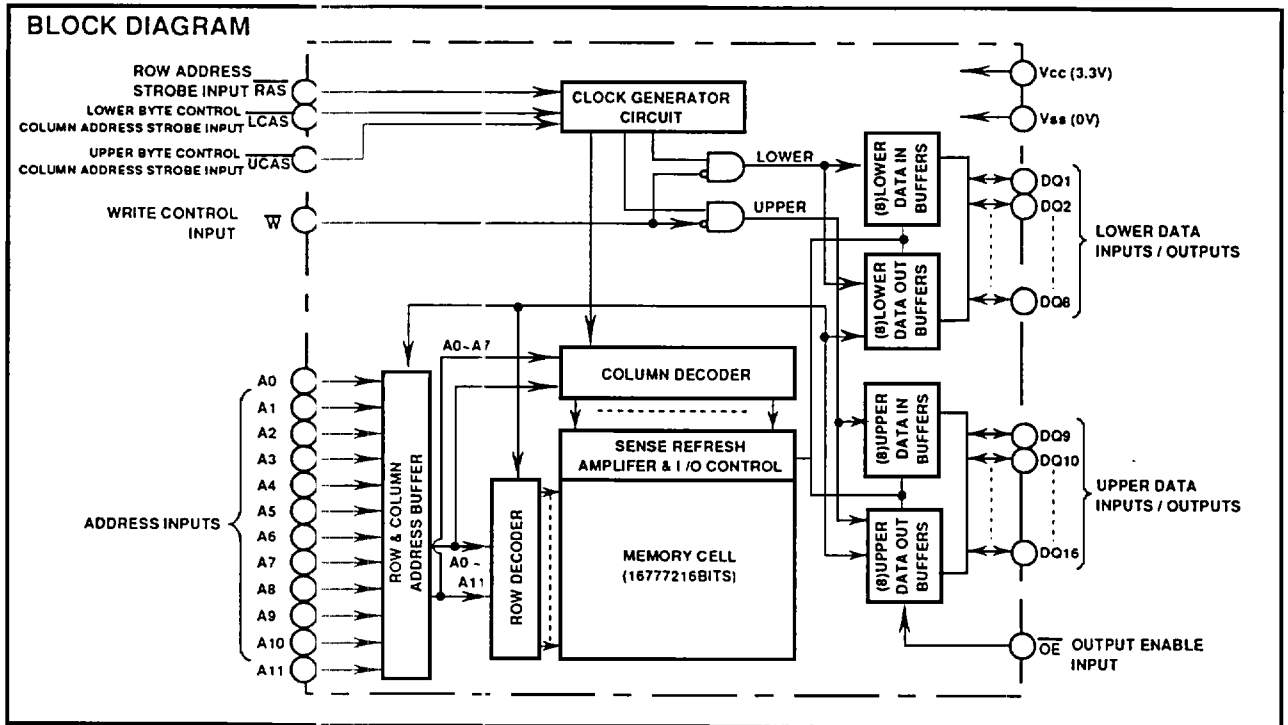
The M5M4V16165BJ, TP provides, in addition to normal read, write, and read-modify-write operations,

a number of other functions, e.g., hyper page mode, RAS only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
RAS-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
CAS before RAS refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, IVD : Invalid, APD : applied, OPN : open



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.5 ~ 4.6	V
V <sub>I</sub>	Input voltage	With respect to V <sub>SS</sub>	-0.5 ~ 4.6	V
V <sub>O</sub>	Output voltage		-0.5 ~ 4.6	V
I <sub>O</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> =25°C	1000	mW
T <sub>opr</sub>	Operating temperature		0 ~ 70	°C
T <sub>stg</sub>	Storage temperature		-65 ~ 150	°C

## RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub>=0 ~ 70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V <sub>CC</sub>	Supply voltage	3.0	3.3	3.6	V
V <sub>SS</sub>	Supply voltage	0	0	0	V
V <sub>IH</sub>	High-level input voltage, all inputs	2.0		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Low-level input voltage, all inputs	-0.3		0.8	V

Note 1: All voltage values are with respect to V<sub>SS</sub>

## ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=0 ~ 70°C, V<sub>CC</sub>=3.3V ± 0.3V, V<sub>SS</sub>=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> =-2.0mA	2.4		V <sub>CC</sub>	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> =2.0mA	0		0.4	V
I <sub>oz</sub>	Off-state output current	O floating 0V ≤ V <sub>out</sub> ≤ 3.3V	-5		5	μA
I <sub>I</sub>	Input current	0V ≤ V <sub>IH</sub> ≤ 3.6V, Other inputs pins=0V	-5		5	μA
I <sub>CC1</sub> (AV)	Average supply current from V <sub>CC</sub> operating (Note 3,4,5)	M5M4V16165B-6,6S	R <sub>AS</sub> , C <sub>AS</sub> cycling t <sub>rc</sub> =t <sub>wc</sub> =min. output open		95	mA
		M5M4V16165B-7,7S			85	
		M5M4V16165B-8,8S			75	
I <sub>CC2</sub>	Supply current from V <sub>CC</sub> , stand-by (Note 4)	R <sub>AS</sub> =C <sub>AS</sub> =V <sub>IH</sub> , output open R <sub>AS</sub> =C <sub>AS</sub> ≥ V <sub>CC</sub> -0.2V			2 0.5	mA
I <sub>CC3</sub> (AV)	Average supply current from V <sub>CC</sub> refreshing (Note 3,5)	M5M4V16165B-6,6S M5M4V16165B-7,7S M5M4V16165B-8,8S	R <sub>AS</sub> cycling, C <sub>AS</sub> =V <sub>IH</sub> t <sub>rc</sub> =min. output open		95 85 75	
I <sub>CC4</sub> (AV)	Average supply current from V <sub>CC</sub> Hyper-Page-Mode (Note 3,4,5)	M5M4V16165B-6,6S M5M4V16165B-7,7S M5M4V16165B-8,8S	R <sub>AS</sub> =V <sub>IL</sub> , C <sub>AS</sub> cycling t <sub>pc</sub> =min. output open		115 100 85	
I <sub>CC6</sub> (AV)	Average supply current from V <sub>CC</sub> C <sub>AS</sub> before R <sub>AS</sub> refresh mode (Note 3)	M5M4V16165B-6,6S M5M4V16165B-7,7S M5M4V16165B-8,8S	C <sub>AS</sub> before R <sub>AS</sub> refresh cycling t <sub>rc</sub> =min. output open		95 85 75	mA

Note 2: Current flowing into an IC is positive, out is negative.

3: I<sub>CC1</sub>(AV), I<sub>CC3</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on cycle rate. Maximum current is measured at the latest cycle rate.

4: I<sub>CC1</sub>(AV) and I<sub>CC4</sub>(AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while R<sub>AS</sub>=V<sub>IL</sub> and LCAS/UCAS=V<sub>IH</sub>.

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## CAPACITANCE (Ta=0 ~ 70°C, V<sub>CC</sub>=3.3V ±0.3V, V<sub>SS</sub>=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
C <sub>i(A)</sub>	Input capacitance, address inputs	M5M4V16165BJ, TP	V <sub>i</sub> =V <sub>SS</sub> f=1MHz V <sub>i</sub> =25mVrms			5	pF
C <sub>i(OE)</sub>	Input capacitance, OE input					7	pF
C <sub>i(W)</sub>	Input capacitance, write control input					7	pF
C <sub>i(RAS)</sub>	Input capacitance, RAS input					7	pF
C <sub>i(CAS)</sub>	Input capacitance, CAS input					7	pF
C <sub>i/O</sub>	Input/Output capacitance, data ports					8	pF

## SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, V<sub>CC</sub> = 5V ± 10%, V<sub>SS</sub>=0V, unless otherwise noted, see notes 6,14,15)

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
t <sub>CAC</sub>	Access time from CAS (Note 7,8)		15		20		20	ns
t <sub>RAC</sub>	Access time from RAS (Note 7,9)		60		70		80	ns
t <sub>AA</sub>	Column address access time (Note 7,10)		30		35		40	ns
t <sub>CPA</sub>	Access time from CAS precharge (Note 7,11)		35		40		45	ns
t <sub>OEa</sub>	Access time from OE (Note 7)		15		20		20	ns
t <sub>OHC</sub>	Output hold time from CAS	5		5		5		ns
t <sub>OHR</sub>	Output hold time from RAS (Note 13)	5		5		5		ns
t <sub>CLZ</sub>	Output low impedance time from CAS low (Note 7)	5		5		5		ns
t <sub>OEZ</sub>	Output disable time after OE high (Note 12)		15		20		20	ns
t <sub>WEZ</sub>	Output disable time after WE high (Note 12)		15		20		20	ns
t <sub>OFF</sub>	Output disable time after CAS high (Note 12,13)		15		20		20	ns
t <sub>REZ</sub>	Output disable time after RAS high (Note 12,13)		15		20		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a RAS clock such as RAS-Only refresh).

Note the RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods (greater than 64 ms) of RAS inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to V<sub>OH</sub>=2.4V(I<sub>OH</sub>=-2mA) / V<sub>OL</sub>=0.4V(I<sub>OL</sub>=-2mA) load 100pF.

The reference levels for measuring of output signals are 2.0V(V<sub>OH</sub>) and 0.8V(V<sub>OL</sub>).

8: Assumes that t<sub>RCD</sub> ≥ t<sub>RCD(max)</sub> and t<sub>ASC</sub> ≥ t<sub>ASC(max)</sub> and t<sub>CP</sub> ≥ t<sub>CP(max)</sub>.

9: Assumes that t<sub>RCD</sub> ≤ t<sub>RCD(max)</sub> and t<sub>RAD</sub> ≤ t<sub>RAD(max)</sub>. If t<sub>RCD</sub> or t<sub>RAD</sub> is greater than the maximum recommended value shown in this table, t<sub>RAC</sub> will increase by amount that t<sub>RCD</sub> exceeds the value shown.

10: Assumes that t<sub>RAD</sub> ≥ t<sub>RAD(max)</sub> and t<sub>ASC</sub> ≤ t<sub>ASC(max)</sub>.

11: Assumes that t<sub>CP</sub> ≤ t<sub>CP(max)</sub> and t<sub>ASC</sub> ≥ t<sub>ASC(max)</sub>.

12: t<sub>OEZ(max)</sub>, t<sub>WEZ(max)</sub>, t<sub>OFF(max)</sub> and t<sub>REZ(max)</sub> defines the time at which the output achieves the high impedance state (I<sub>out</sub> ≤ I ± 10 μA) and is not reference to V<sub>OH(min)</sub> or V<sub>OL(max)</sub>.

13: Output is disabled after both RAS and CAS go to high.

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# M5M4-V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER-PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Hyper-Page Mode Cycles)

(Ta=0 ~ 70°C, Vcc = 5V ±10%, Vss=0V, unless otherwise noted See notes 14,15)

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tREF	Refresh cycle time		64		64		64	ms
tRP	RAS high pulse width	40		50		60		ns
tRCD	Delay time, RAS low to CAS low (Note16)	20	38	20	42	20	42	ns
tCRP	Delay time, CAS high to RAS low	5		5		5		ns
tRPC	Delay time, RAS high to CAS low	0		0		0		ns
tCPN	CAS high pulse width	10		13		13		ns
tRAD	Column address delay time from RAS low (Note17)	15	30	15	35	15	40	ns
tASR	Row address setup time before RAS low	0		0		0		ns
tASC	Column address setup time before CAS low (Note18)	0	13	0	13	0	13	ns
tRAH	Row address hold time after RAS low	10		10		10		ns
tCAH	Column address hold time after CAS low	10		10		10		ns
tDZC	Delay time, data to CAS low (Note19)	0		0		0		ns
tDZO	Delay time, data to OE low (Note19)	0		0		0		ns
tRDD	Delay time, RAS high to data (Note20)	15		20		20		ns
tCDD	Delay time, CAS high to data (Note20)	15		20		20		ns
tODD	Delay time, OE high to data (Note20)	15		20		20		ns
tT	Transition time (Note21)	1	50	1	50	1	50	ns

Note 14: The timing requirements are as:  $t_T = 2ns$ .

15:  $V_{IH(min)}$  and  $V_{IL(max)}$  are reference levels for measuring timing of input signals.

16:  $t_{RCD(max)}$  is specified as a reference point only. If  $t_{RCD}$  is less than  $t_{RCD(max)}$ , access time is  $t_{RAC}$ . If  $t_{RCD}$  is greater than  $t_{RCD(max)}$ , access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .

17:  $t_{RAD(max)}$  is specified as a reference point only. If  $t_{RAD} \geq t_{RAD(max)}$  and  $t_{ASC} \leq t_{ASC(max)}$ , access time is controlled exclusively by  $t_{AA}$ .

18:  $t_{ASC(max)}$  is specified as a reference point only. If  $t_{RCD} \geq t_{RCD(max)}$  and  $t_{ASC} \geq t_{ASC(max)}$ , access time is controlled exclusively by  $t_{CAC}$ .

19: Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.

20: Either  $t_{RDD}$  or  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.

21:  $t_T$  is measured between  $V_{IH(min)}$  and  $V_{IL(max)}$ .

## Read and Refresh Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tRC	Read cycle time	110		130		150		ns
tRAS	RAS low pulse width	60	10000	70	10000	80	10000	ns
tCAS	CAS low pulse width	10	10000	13	10000	13	10000	ns
tCSH	CAS hold time after RAS low	48		55		62		ns
tRSH	RAS hold time after CAS low	15		20		20		ns
tRCS	Read Setup time before CAS low	0		0		0		ns
tRCH	Read hold time after CAS high (Note 22)	0		0		0		ns
tRRH	Read hold time after RAS high (Note 22)	10		10		10		ns
tRAL	Column address to RAS hold time	30		35		40		ns
tCAL	Column address to CAS hold time	18		23		23		ns
tORH	RAS hold time after OE low	15		20		20		ns
tOCH	CAS hold time after OE low	15		20		20		ns

Note 22: Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

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## Write Cycle (Early Write and Delayed Write)

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
t <sub>WC</sub>	Write cycle time	110		130		150		ns
t <sub>RAS</sub>	RAS low pulse width	60	10000	70	10000	80	10000	ns
t <sub>CAS</sub>	CAS low pulse width	10	10000	13	10000	13	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	48		55		63		ns
t <sub>RSH</sub>	RAS hold time after CAS low	15		20		20		ns
t <sub>WCS</sub>	Write setup time before CAS low (Note 24)	0		0		0		ns
t <sub>WCH</sub>	Write hold time after CAS low	10		13		15		ns
t <sub>CWL</sub>	CAS hold time after W low	10		13		15		ns
t <sub>RWL</sub>	RAS hold time after W low	10		13		15		ns
t <sub>WP</sub>	Write pulse width	10		13		15		ns
t <sub>DS</sub>	Data setup time before CAS low or W low	0		0		0		ns
t <sub>DH</sub>	Data hold time after CAS low or W low	10		13		15		ns

## Read-Write and Read-Modify-Write Cycles

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
t <sub>RWC</sub>	Read write/read modify write cycle time (Note 23)	133		161		183		ns
t <sub>RAS</sub>	RAS low pulse width	89	10000	107	10000	126	10000	ns
t <sub>CAS</sub>	CAS low pulse width	44	10000	57	10000	66	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	82		99		116		ns
t <sub>RSH</sub>	RAS hold time after CAS low	44		57		66		ns
t <sub>RCS</sub>	Read setup time before CAS low	0		0		0		ns
t <sub>CWD</sub>	Delay time, CAS low to W low (Note 24)	32		42		44		ns
t <sub>RWD</sub>	Delay time, RAS low to W low (Note 24)	77		92		107		ns
t <sub>AWD</sub>	Delay time, address to W low (Note 24)	47		57		62		ns
t <sub>OEH</sub>	OE hold time after W low	15		20		20		ns

Note 23: t<sub>RWC</sub> is specified as t<sub>RWC(min)</sub> = t<sub>AC(max)</sub> + t<sub>ODD(min)</sub> + t<sub>RVL(min)</sub> + t<sub>RP(min)</sub> + 4t<sub>1</sub>.

24: t<sub>WCS</sub>, t<sub>WCH</sub>, t<sub>RWD</sub> and t<sub>AWD</sub> and t<sub>CWD</sub> are specified as reference points only. If t<sub>WCS</sub> ≥ t<sub>WCS(min)</sub> the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle. If t<sub>CWD</sub> ≥ t<sub>CWD(min)</sub>, t<sub>RWD</sub> ≥ t<sub>RWD(min)</sub>, t<sub>AWD</sub> ≥ t<sub>AWD(min)</sub> and t<sub>CWD</sub> ≥ t<sub>CWD(min)</sub> (for hyper page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address. If neither of the above condition (delayed write) of the DQ (at access time and until CAS or OE goes back to VIH) is indeterminate.

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

Hyper page Mode Cycle (Read, Early Write, Read-Write, Read-Modify-Write Cycle, Read Write Mix Cycle, Hi-Z control by  $\overline{OE}$  or  $\overline{W}$ ) (Note 25)

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tHPC	Hyper page mode read/write cycle time	25		30		30		ns
tHPRWC	Hyper Page Mode read write / read modify write cycle time	66		79		88		ns
tDOH	Output hold time from $\overline{CAS}$ low	5		5		5		ns
tRAS	RAS low pulse width for read write cycle (Note26)	77	100000	92	100000	107	100000	ns
tCP	CAS high pulse width (Note27)	10	18	13	18	13	18	ns
tCPRH	RAS hold time after $\overline{CAS}$ precharge	35		40		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low (Note24)	52		62		62		ns
tCHOL	Hold time to maintain the data Hi-Z until CAS access	7		7		7		ns
tOEPE	$\overline{OE}$ Pulse Width (Hi-Z control)	7		7		7		ns
tWPE	$\overline{W}$ Pulse Width (Hi-Z control)	7		7		7		ns
tHCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low after read	32		42		52		ns
tHAWD	Delay time, Address to $\overline{W}$ low after read	62		72		82		ns
tHPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low after read	72		82		92		ns
tHCOD	Delay time, $\overline{CAS}$ low to $\overline{OE}$ high after read	15		20		20		ns
tHAOD	Delay time, Address to $\overline{OE}$ high after read	30		35		35		ns
tHPOD	Delay time, $\overline{CAS}$ precharge to $\overline{OE}$ high after read	35		40		40		ns

Note 25: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

26: tRAS(min) is specified as two cycles of  $\overline{CAS}$  input are performed.

27: tCP(max) is specified as a reference point only.

## $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 27)

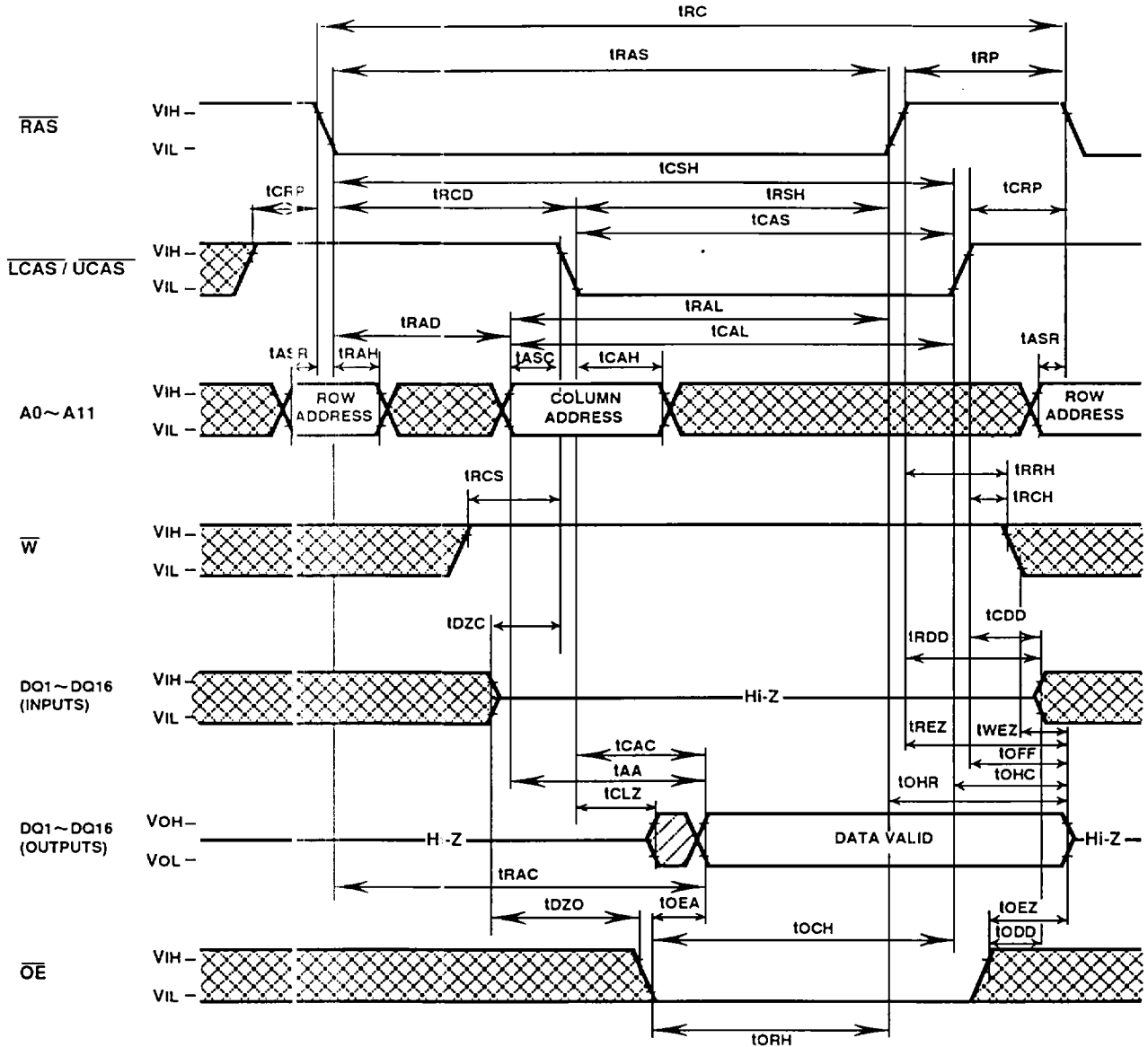
Symbol	Parameter	Limits						Unit
		M5M4V16165B-6,6S		M5M4V16165B-7,7S		M5M4V16165B-8,8S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		15		ns

Note 28: Eight or more  $\overline{CAS}$  before  $\overline{RAS}$  cycles instead of eight  $\overline{RAS}$  cycles are necessary for proper operation of  $\overline{CAS}$  before  $\overline{RAS}$  refresh mode.

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## Timing Diagrams (Note 29) Read Cycle



Note 29



Indicates the don't care input.  
 $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$  or  $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$



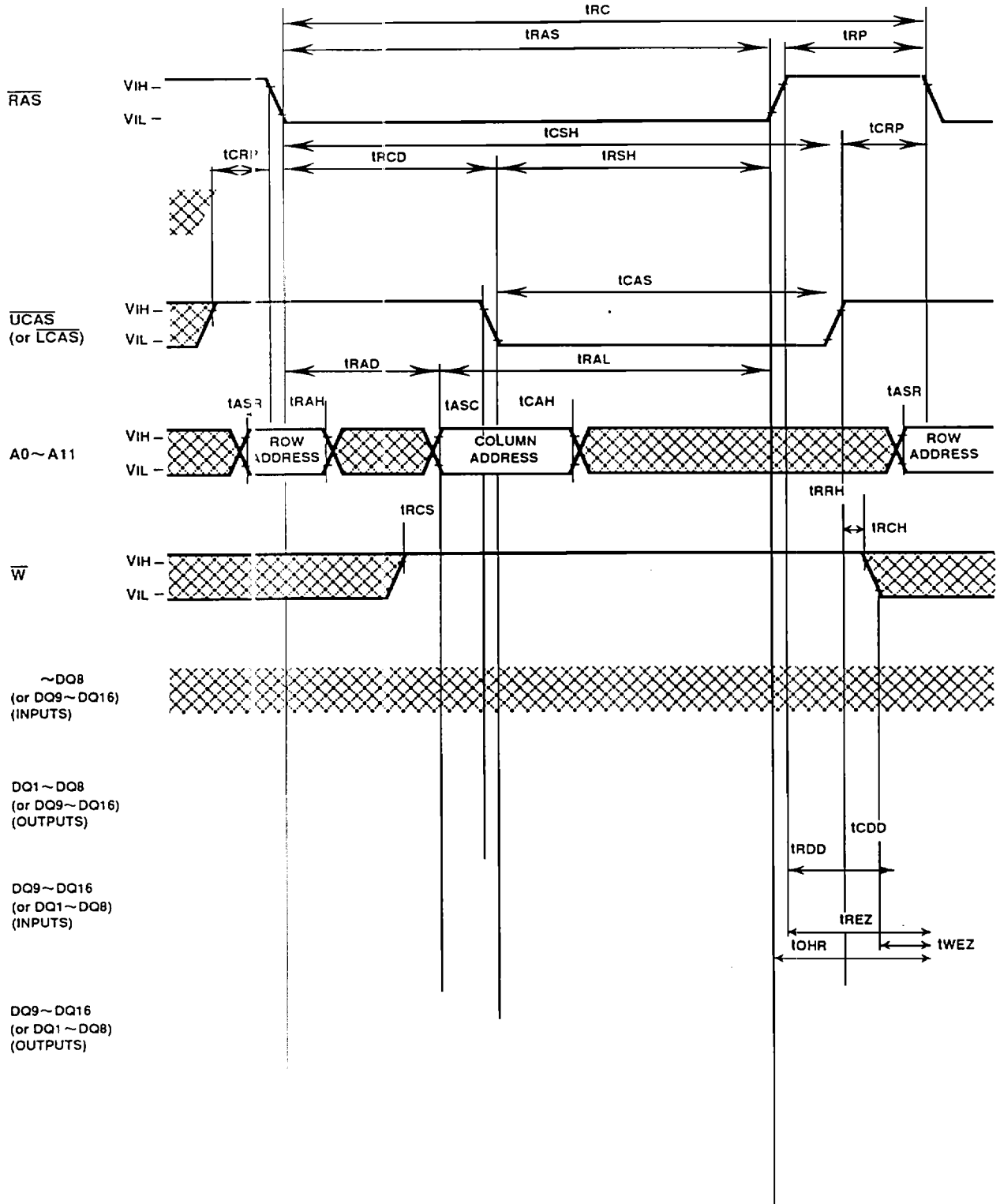
Indicates the invalid output.



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

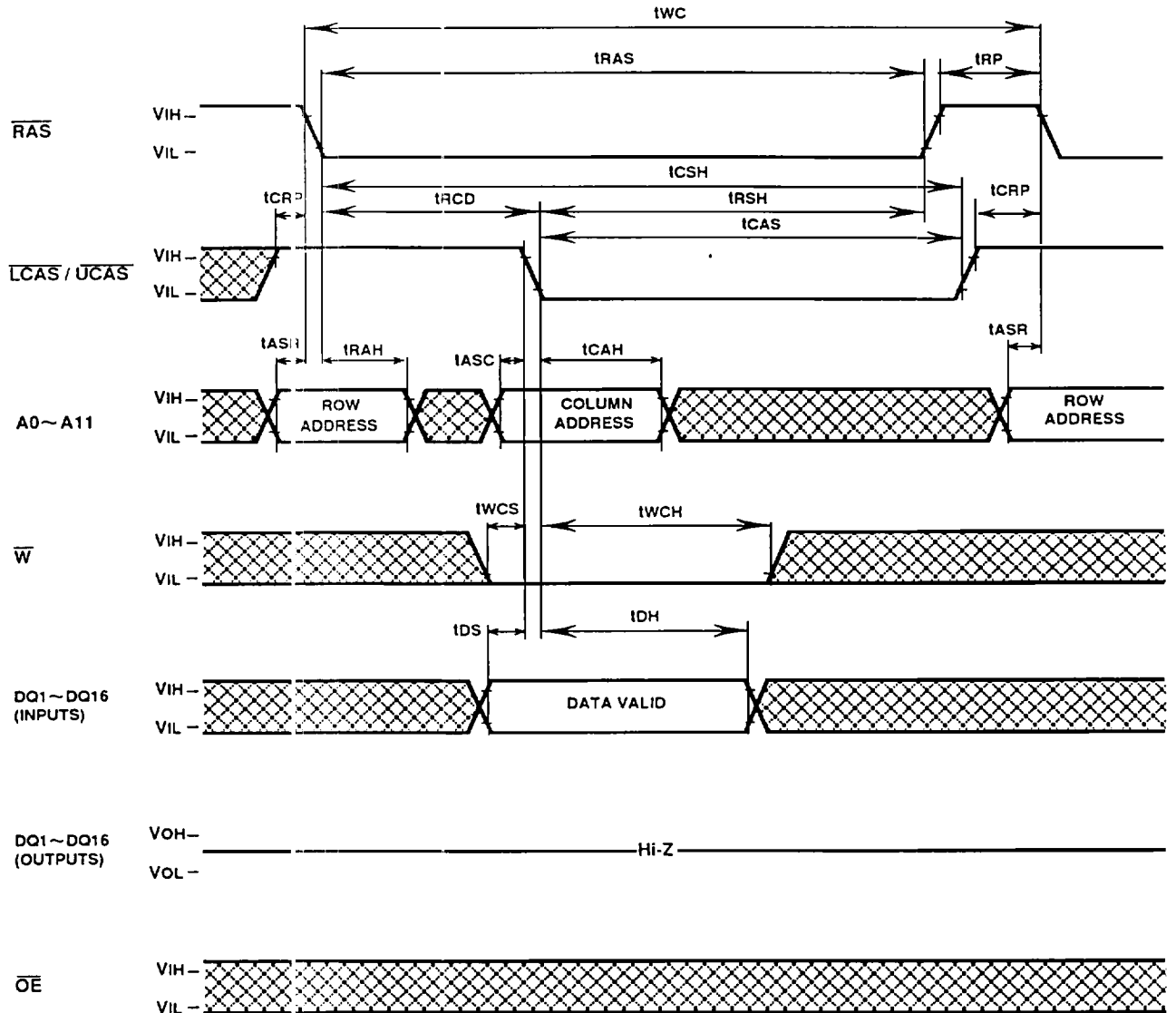
## Byte Read Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

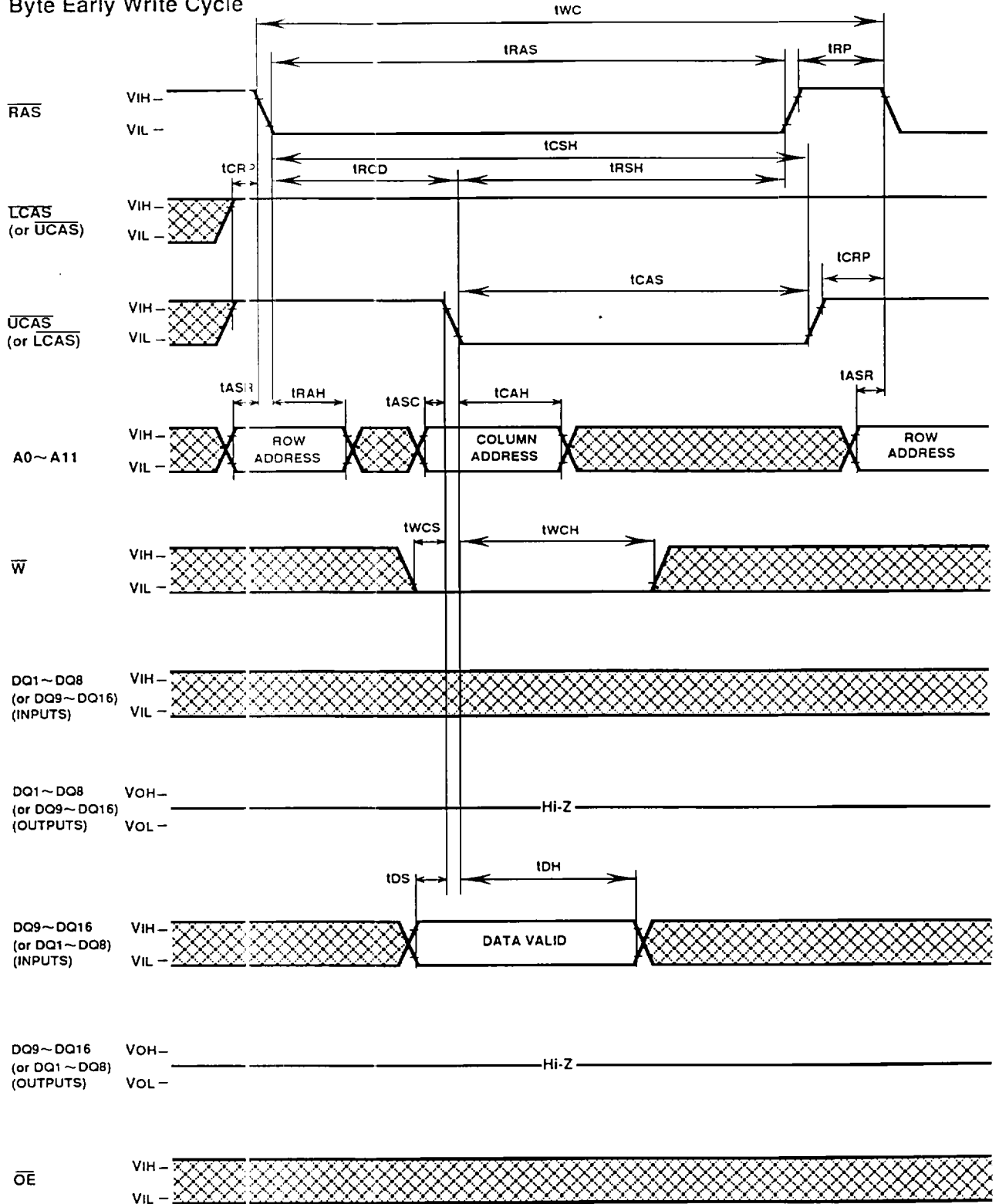
## Early Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## Byte Early Write Cycle

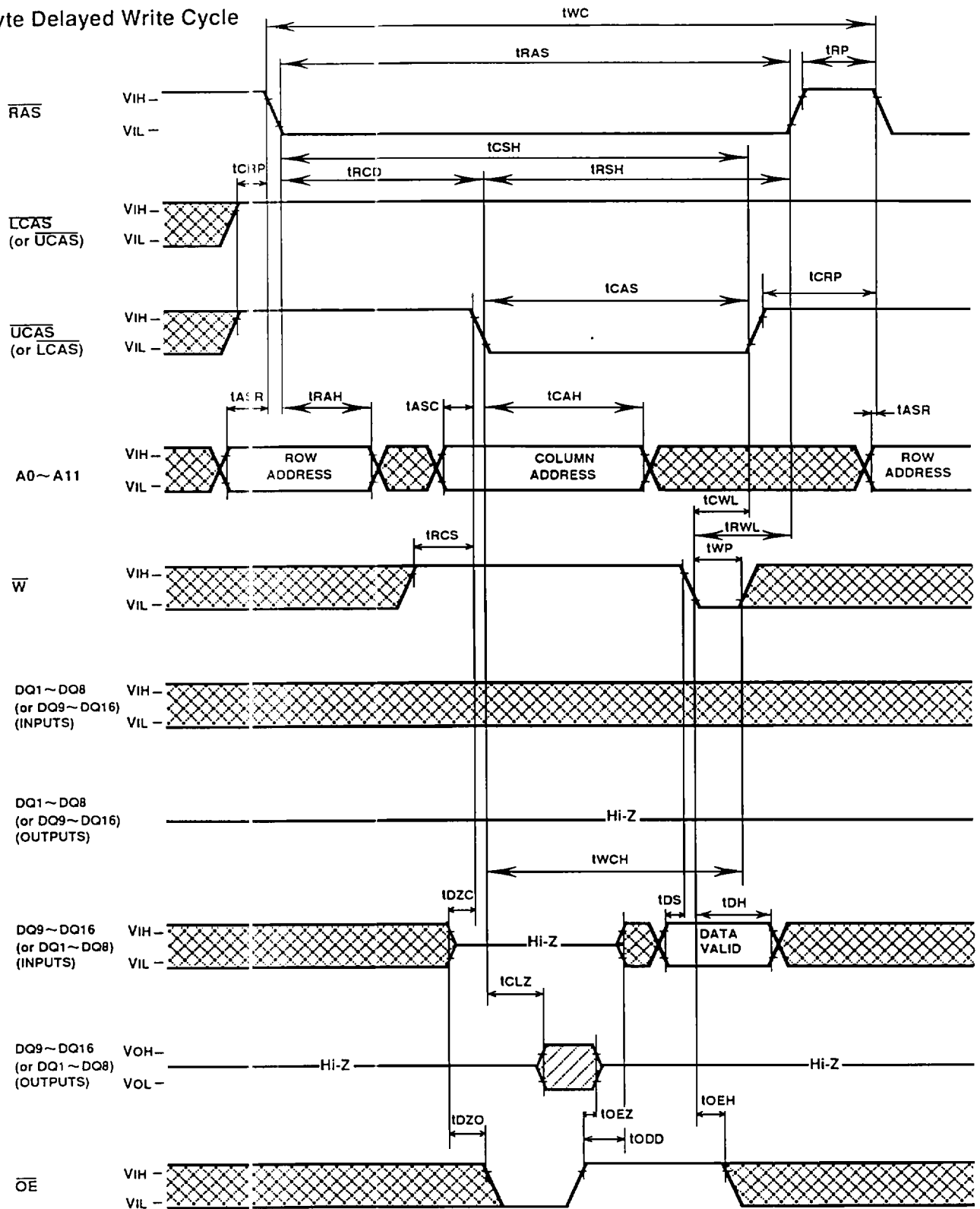




# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

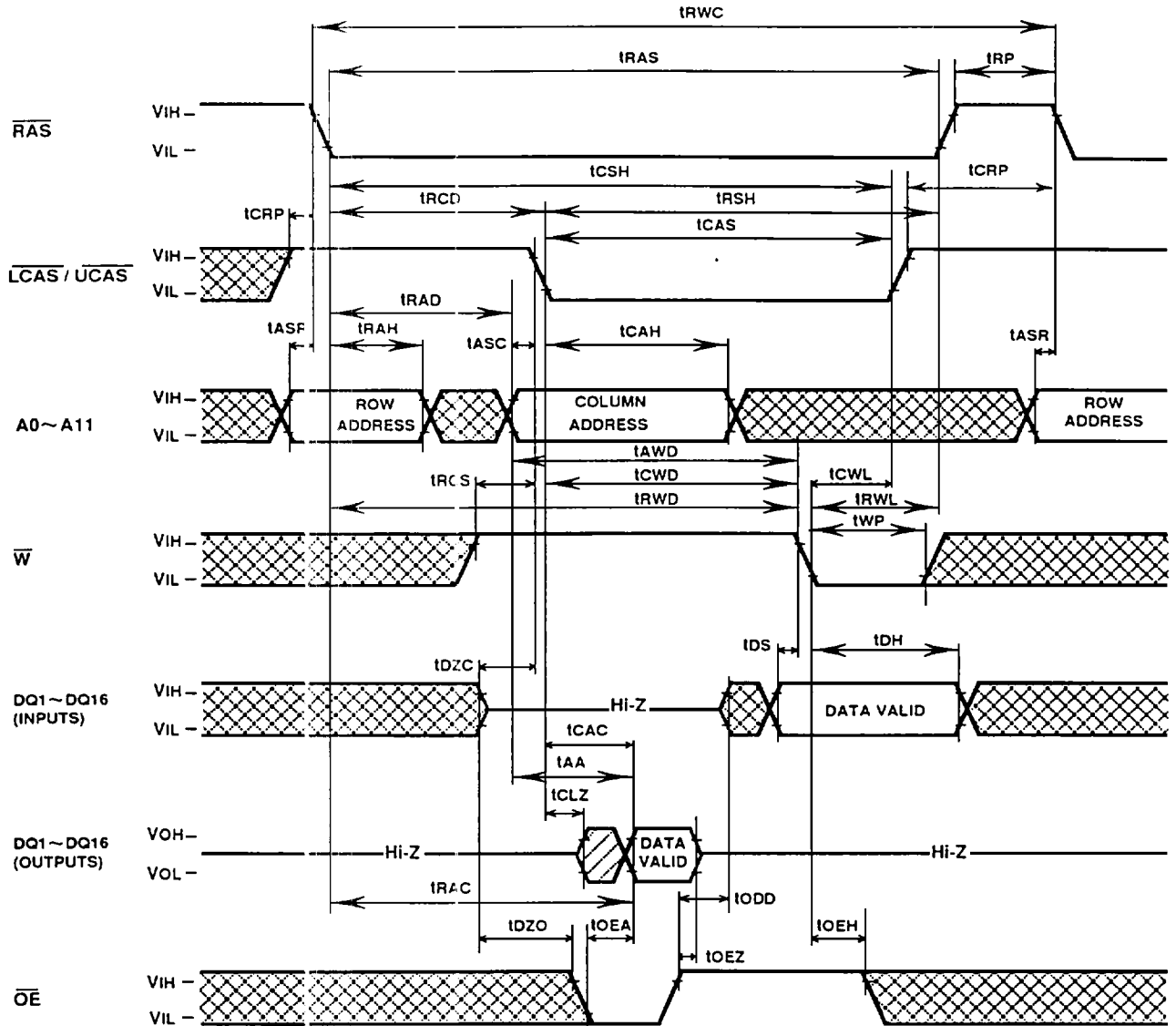
### Byte Delayed Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

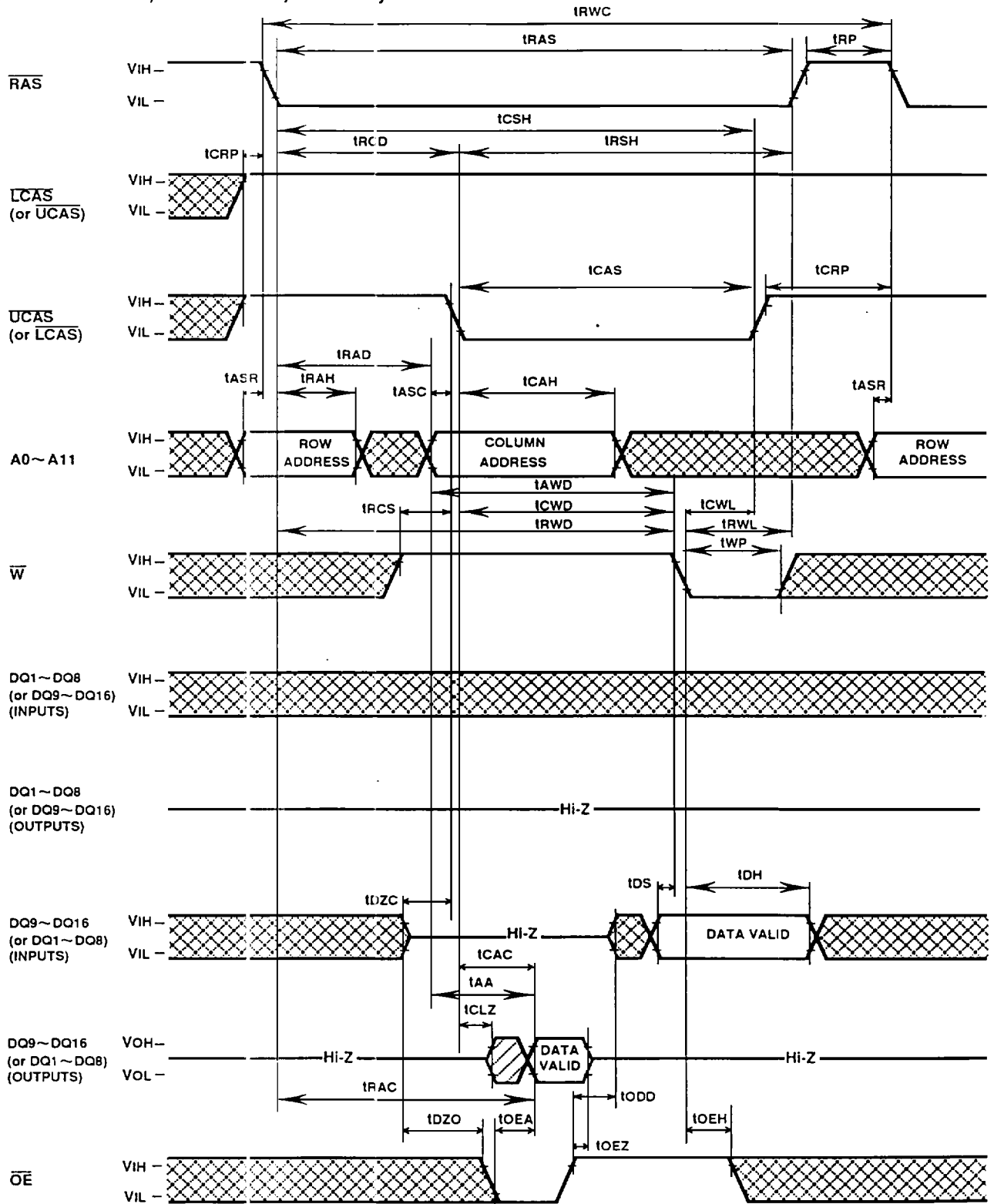
## Read-Write, Read-Modify-Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

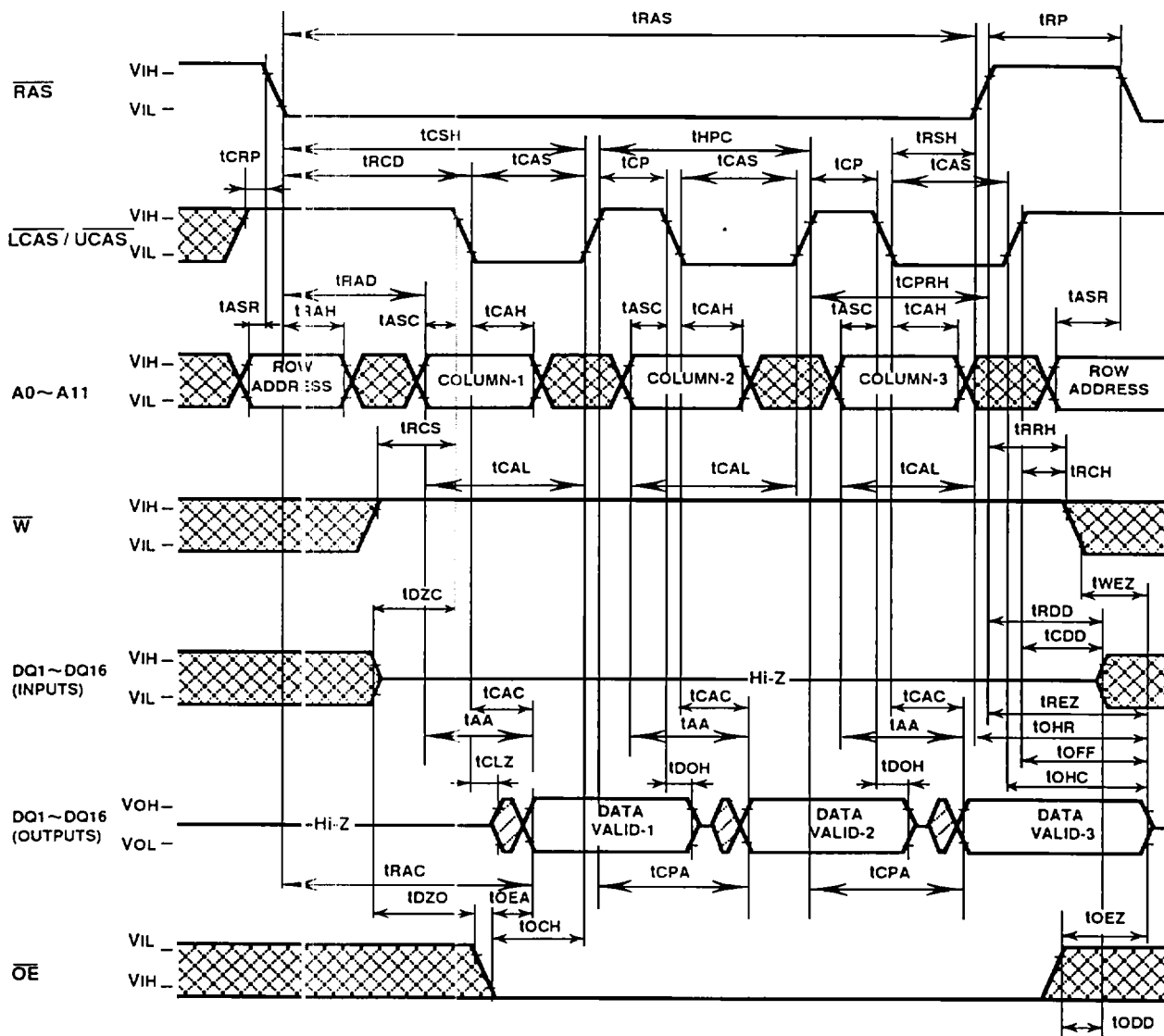
## Byte Read-Write, Read-Modify-Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

## Hyper Page Mode Read Cycle

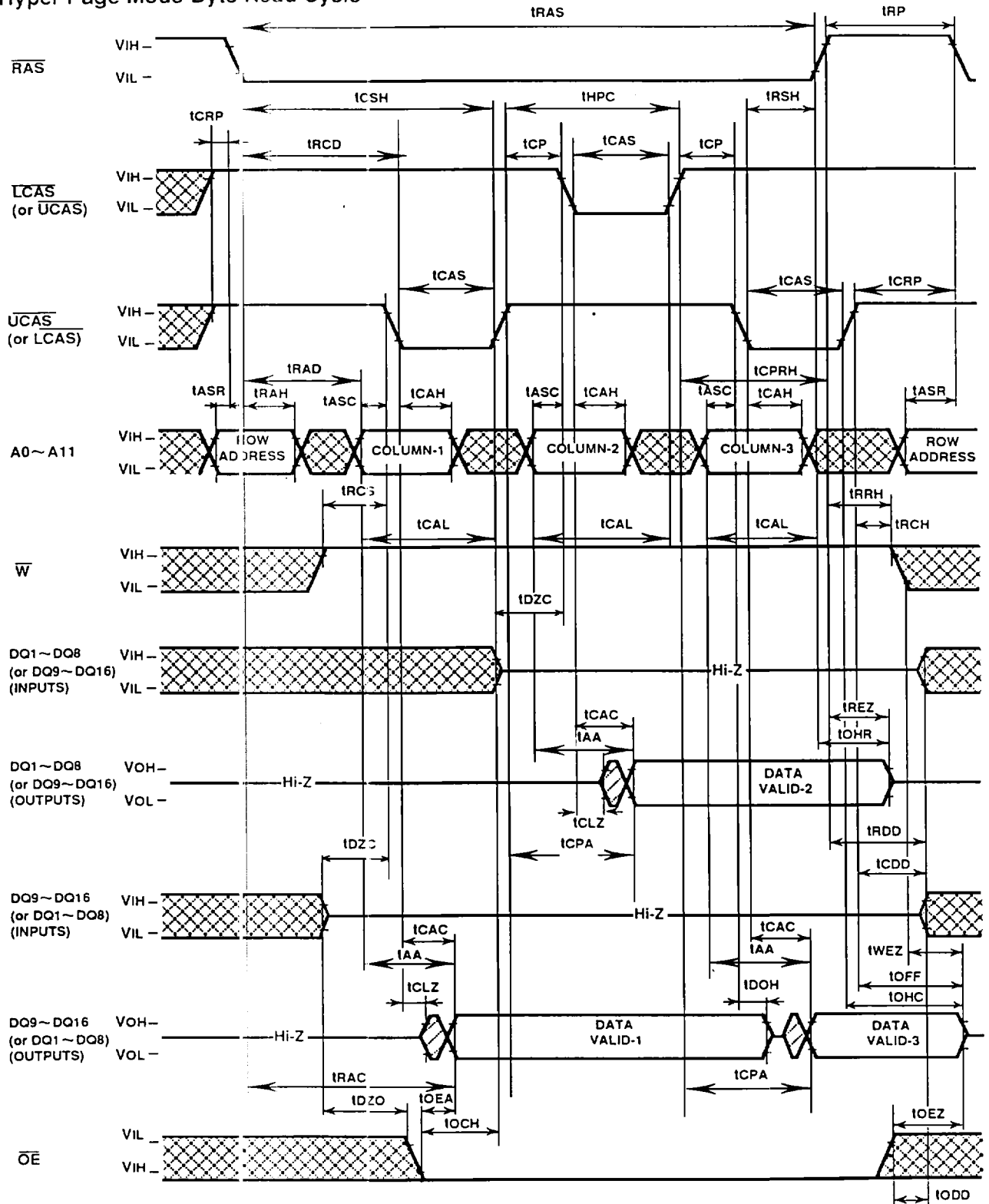




# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

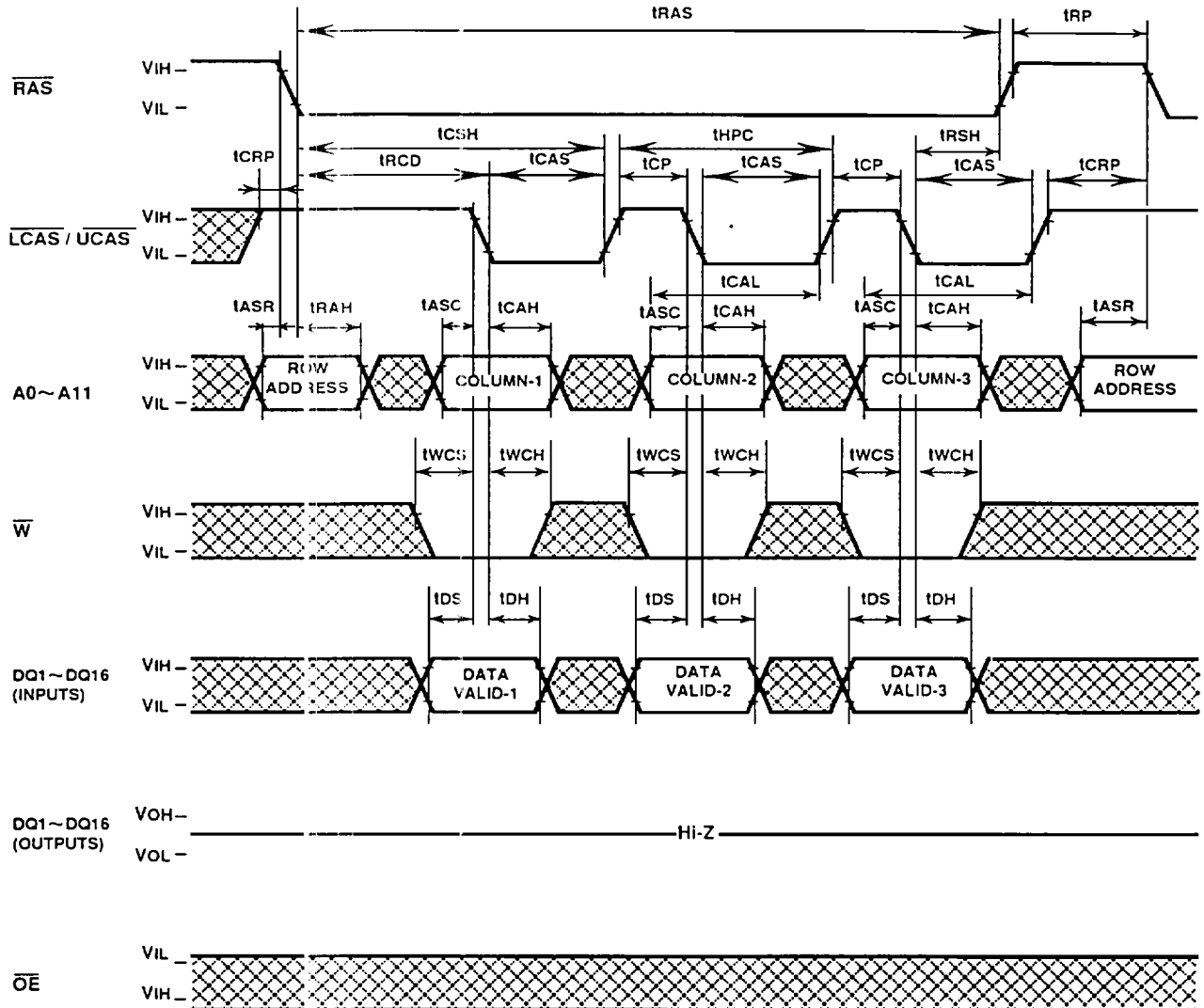
## Hyper Page Mode Byte Read Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

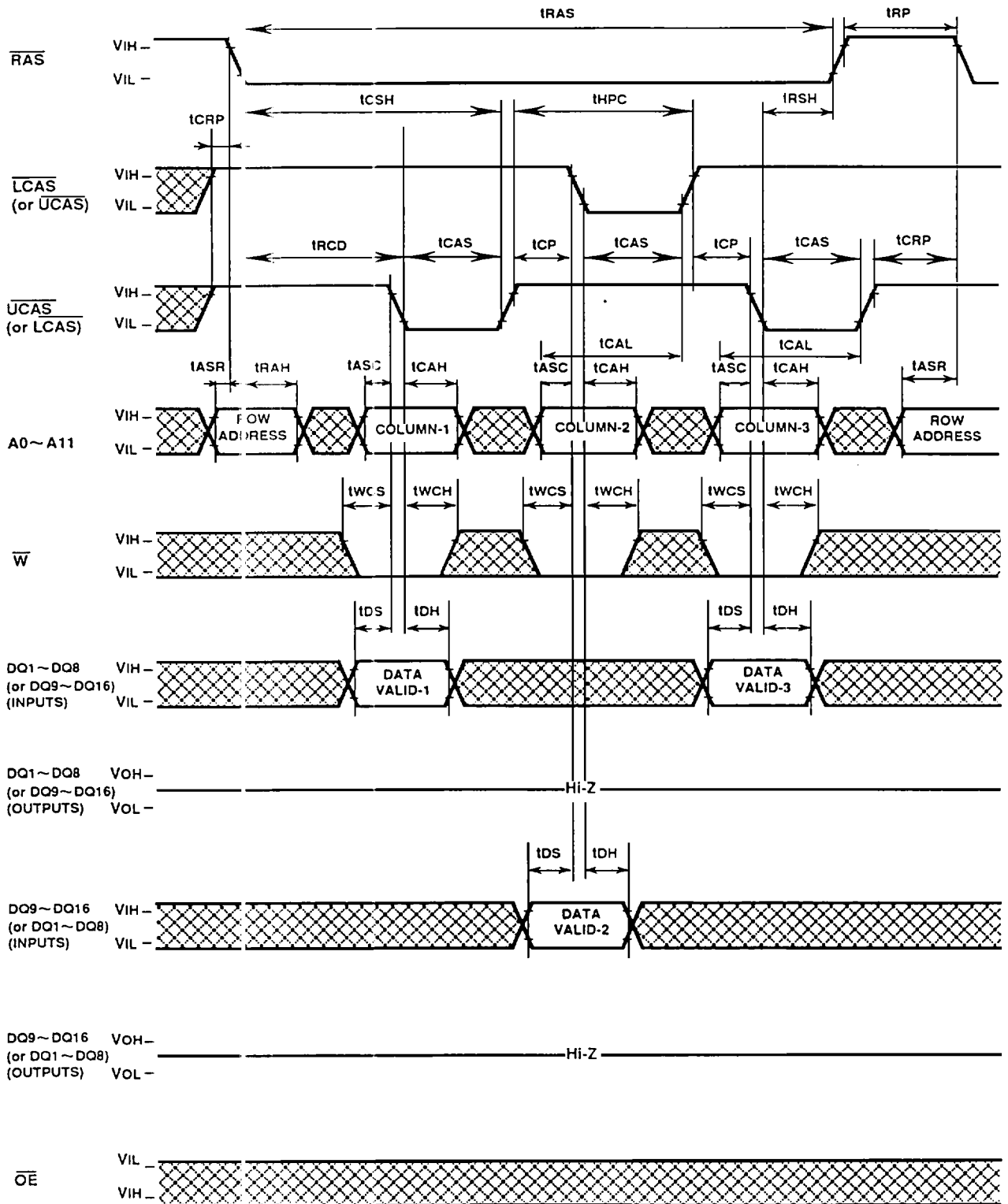
## Hyper Page Mode Early Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

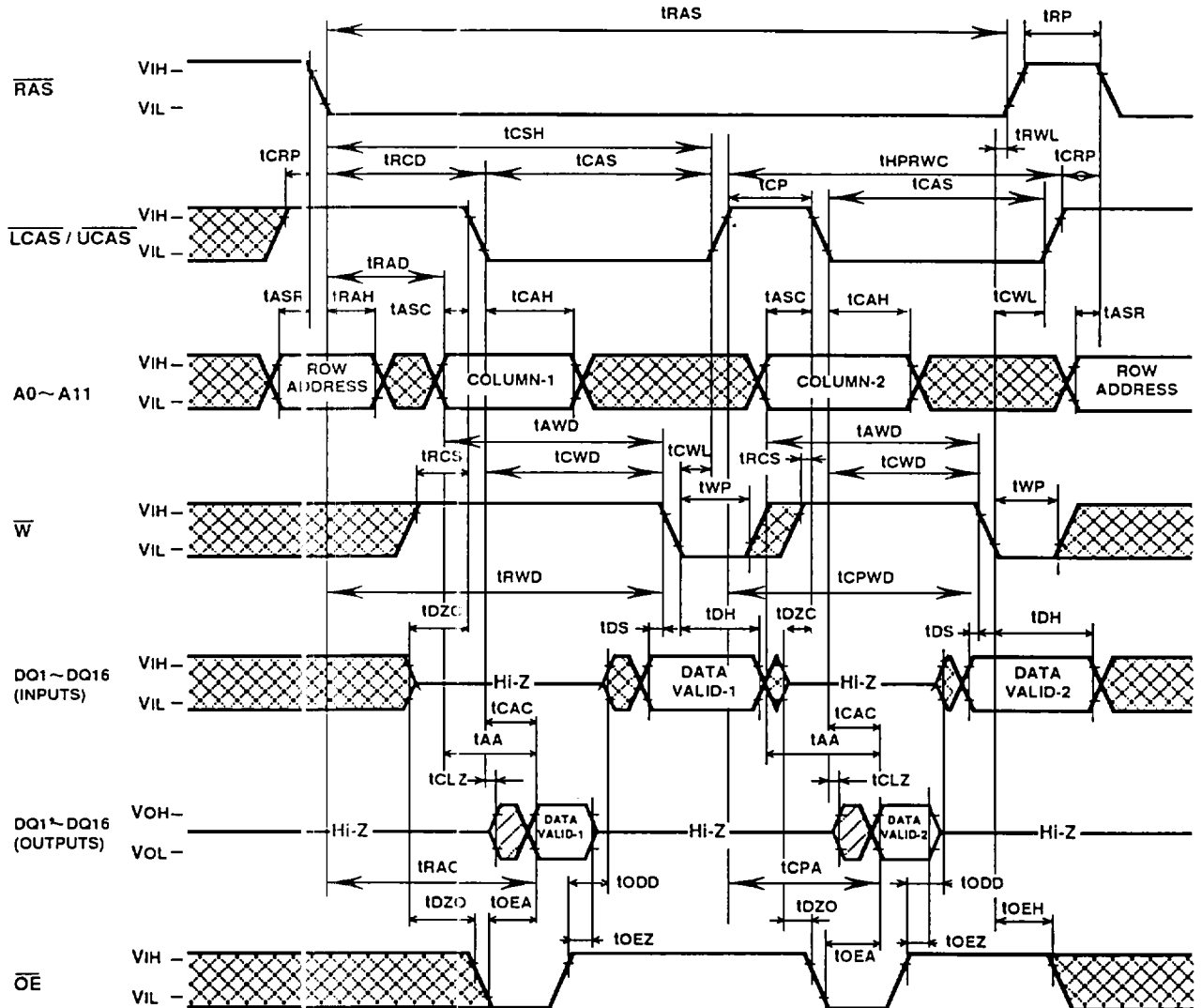
## Hyper Page Mode Byte Early Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

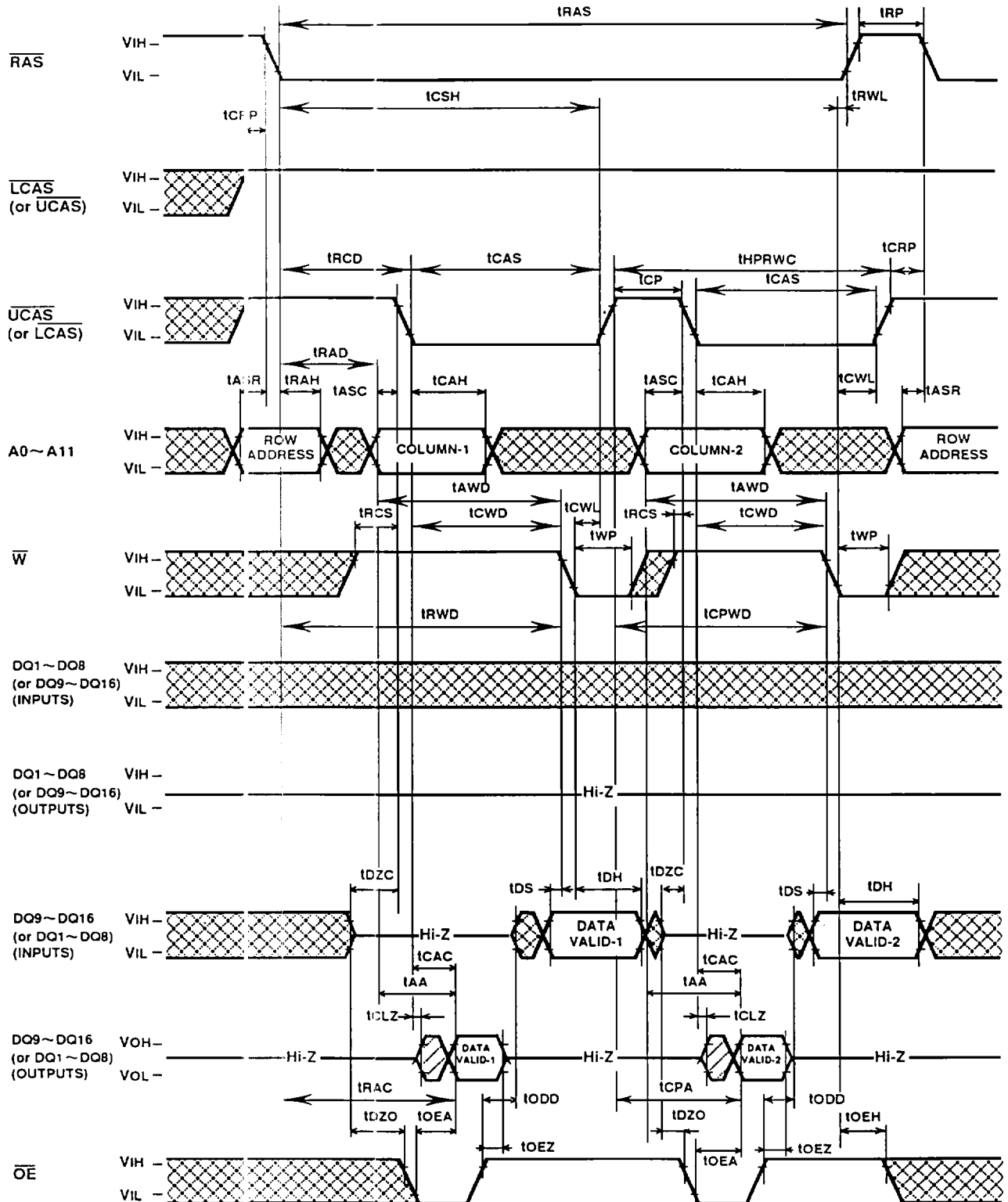
## Hyper Page Mode Read-Write, Read-Modify-Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

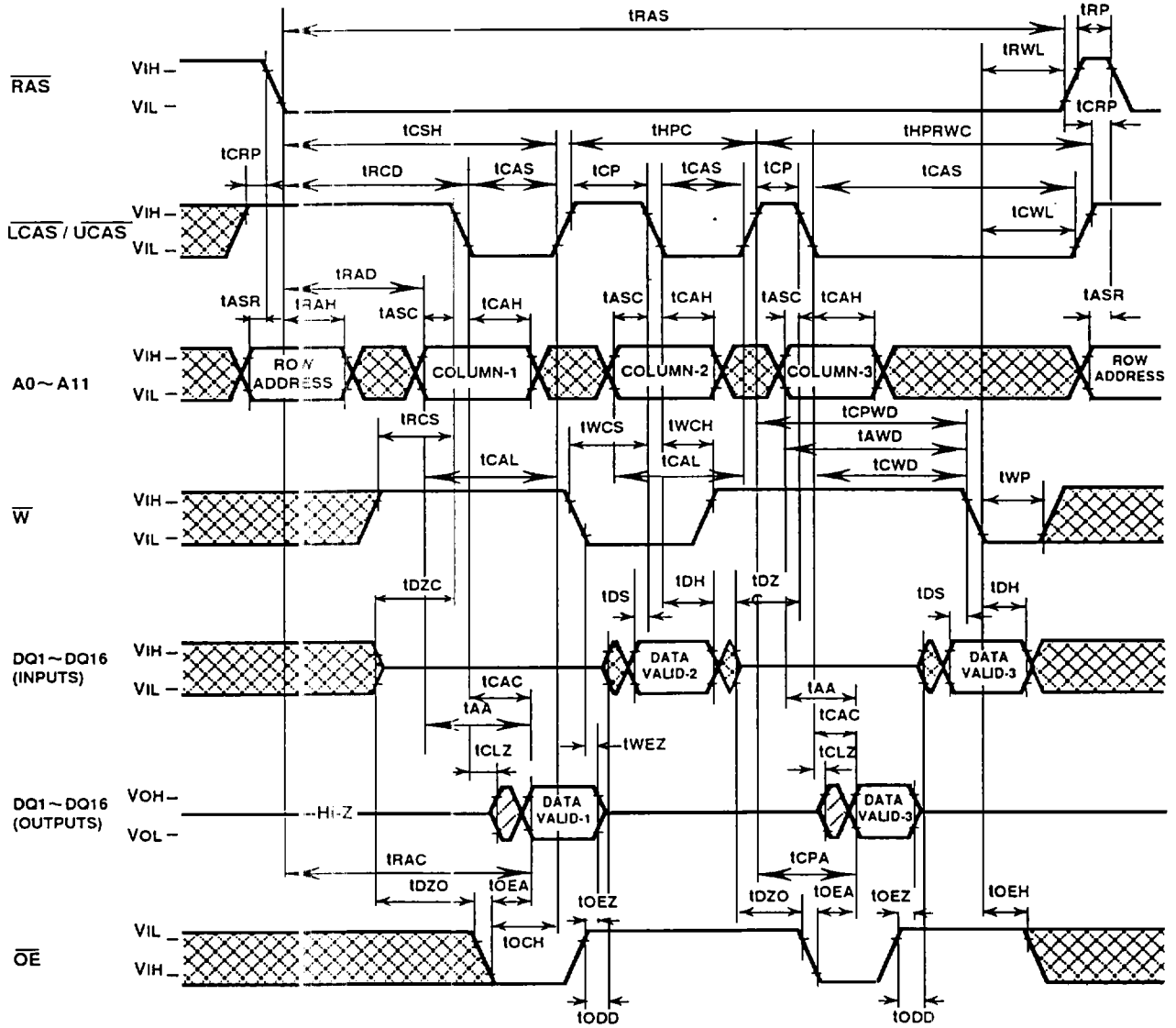
## Hyper Page Mode Byte Read-Write, Read-Modify-Write Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

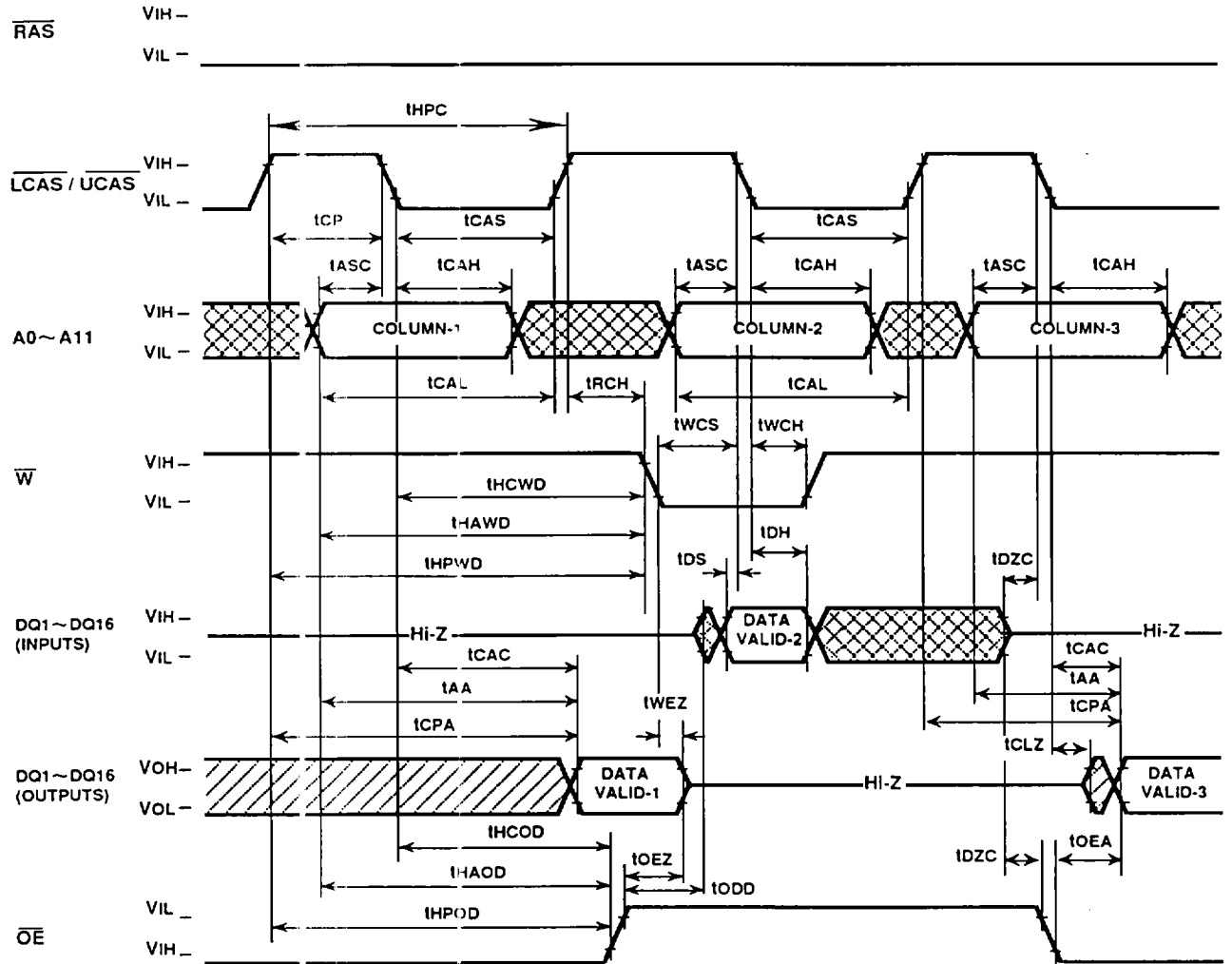
Hyper Page Mode Mix Cycle (1)



# M5M4V16165BJ,TP-6,-7,-8,-6S,-7S,-8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

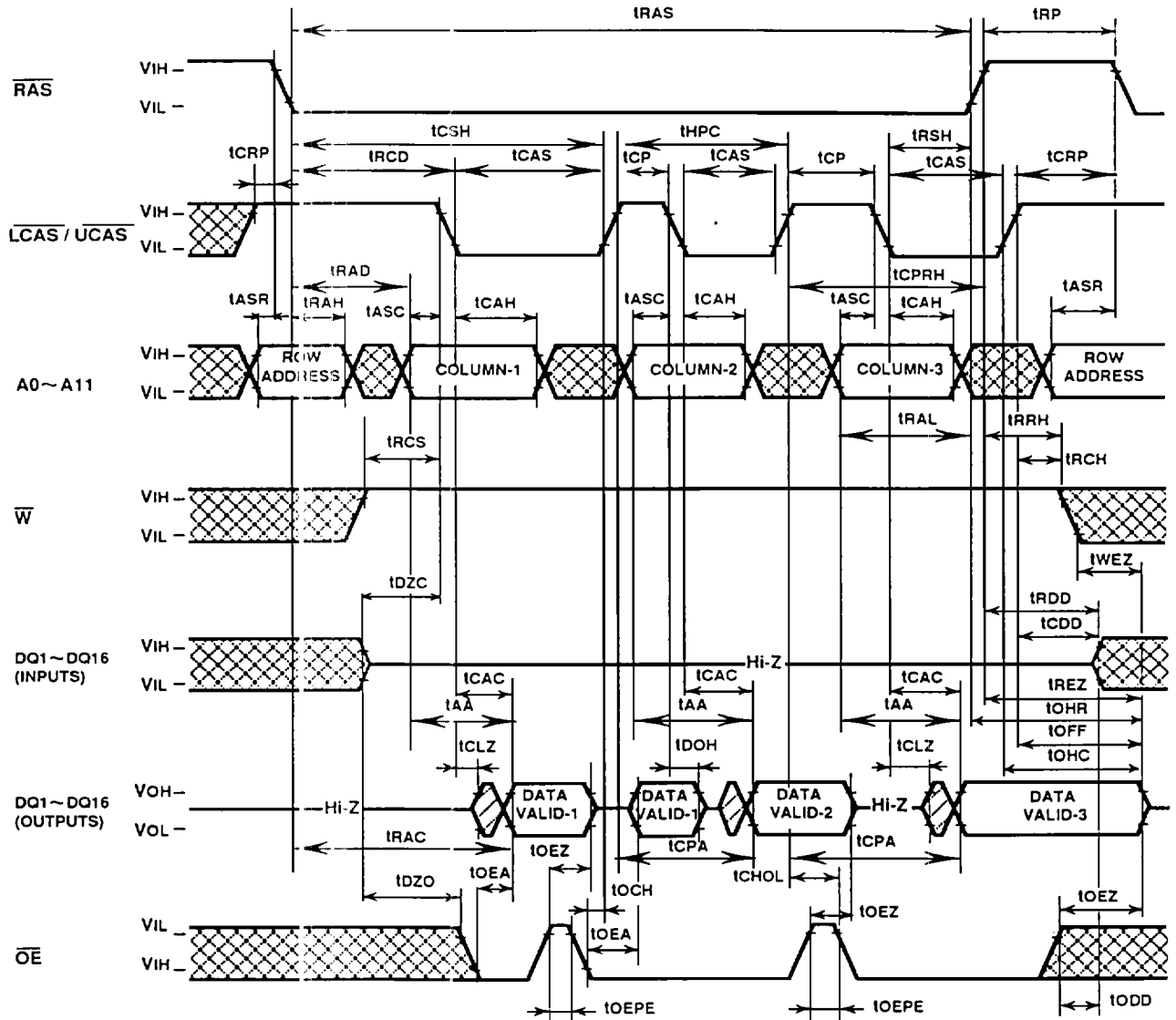
## Hyper Page Mode Mix Cycle (2)



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## Hyper Page Mode Read Cycle ( Hi-Z control by $\overline{OE}$ )

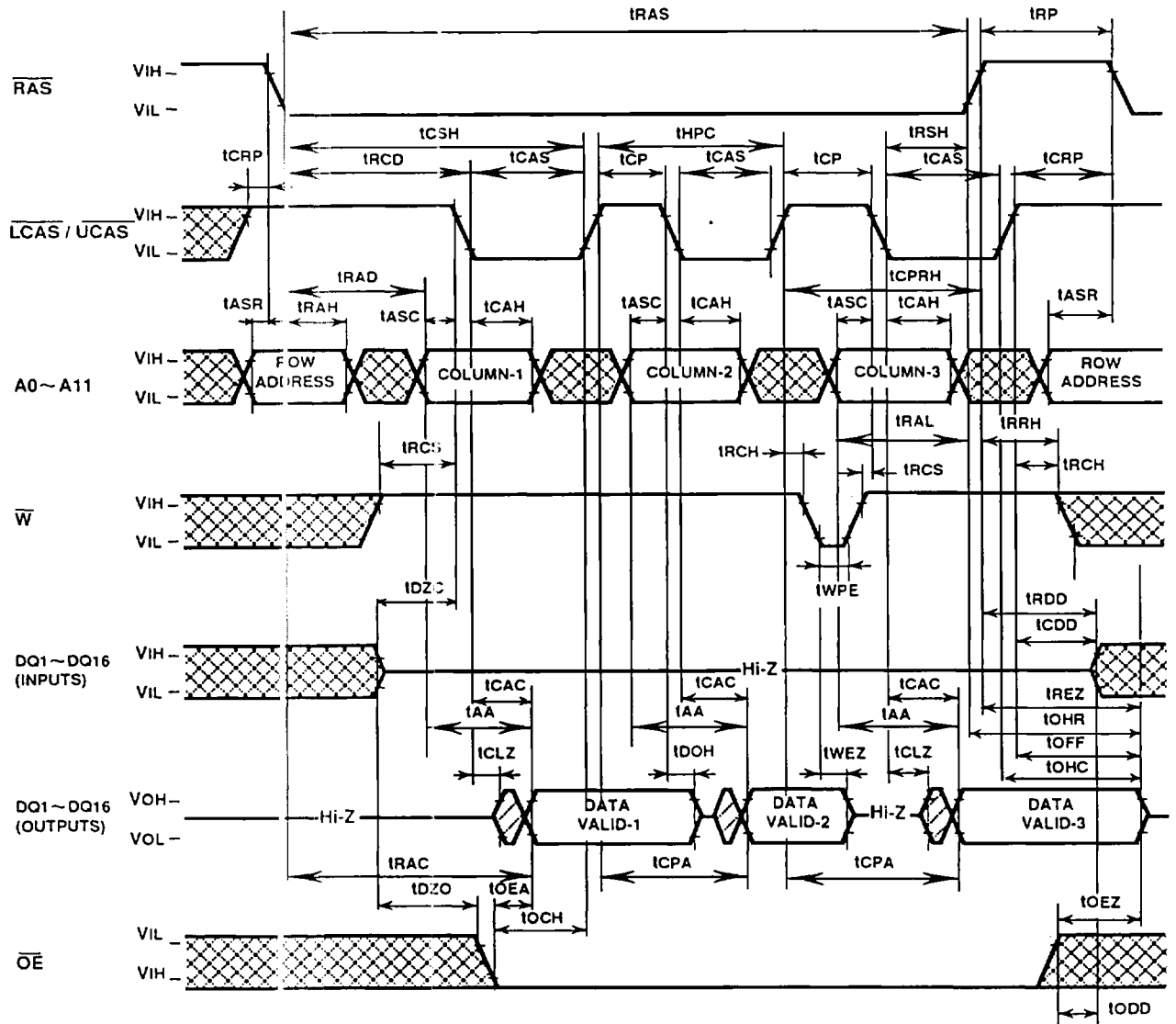




# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

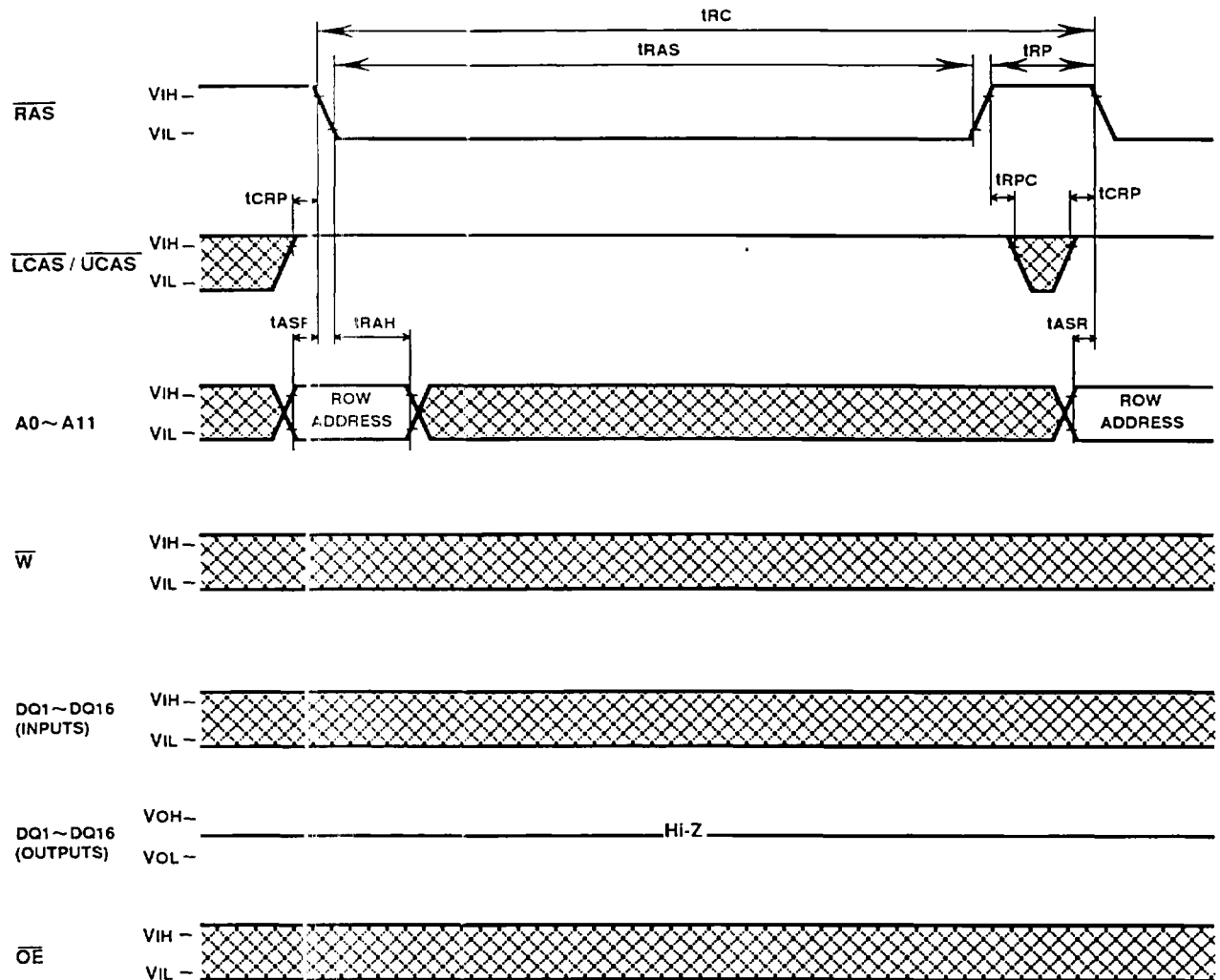
## Hyper Page Mode Read Cycle (Hi-Z control by $\overline{W}$ )



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

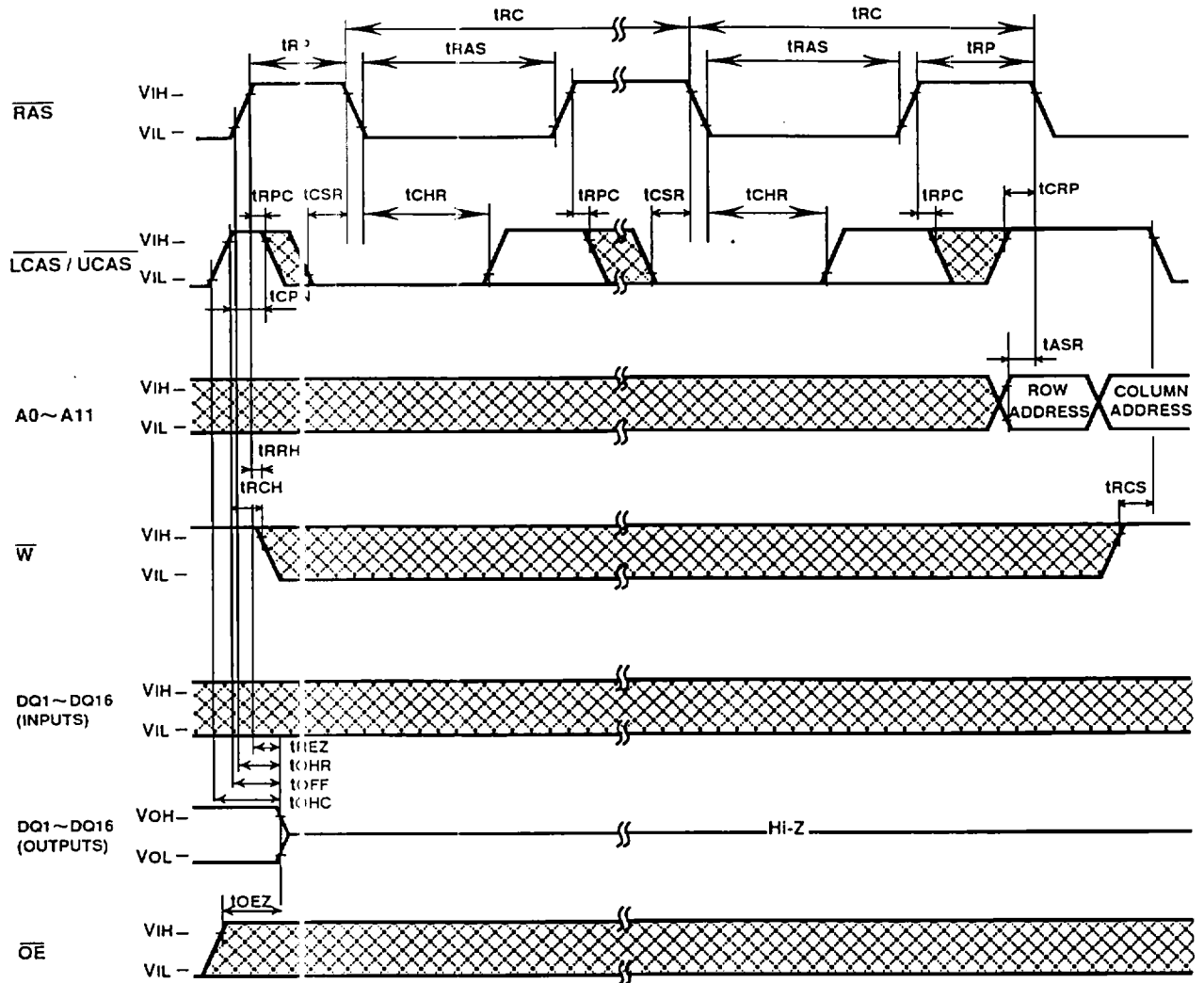
## RAS-only Refresh Cycle



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

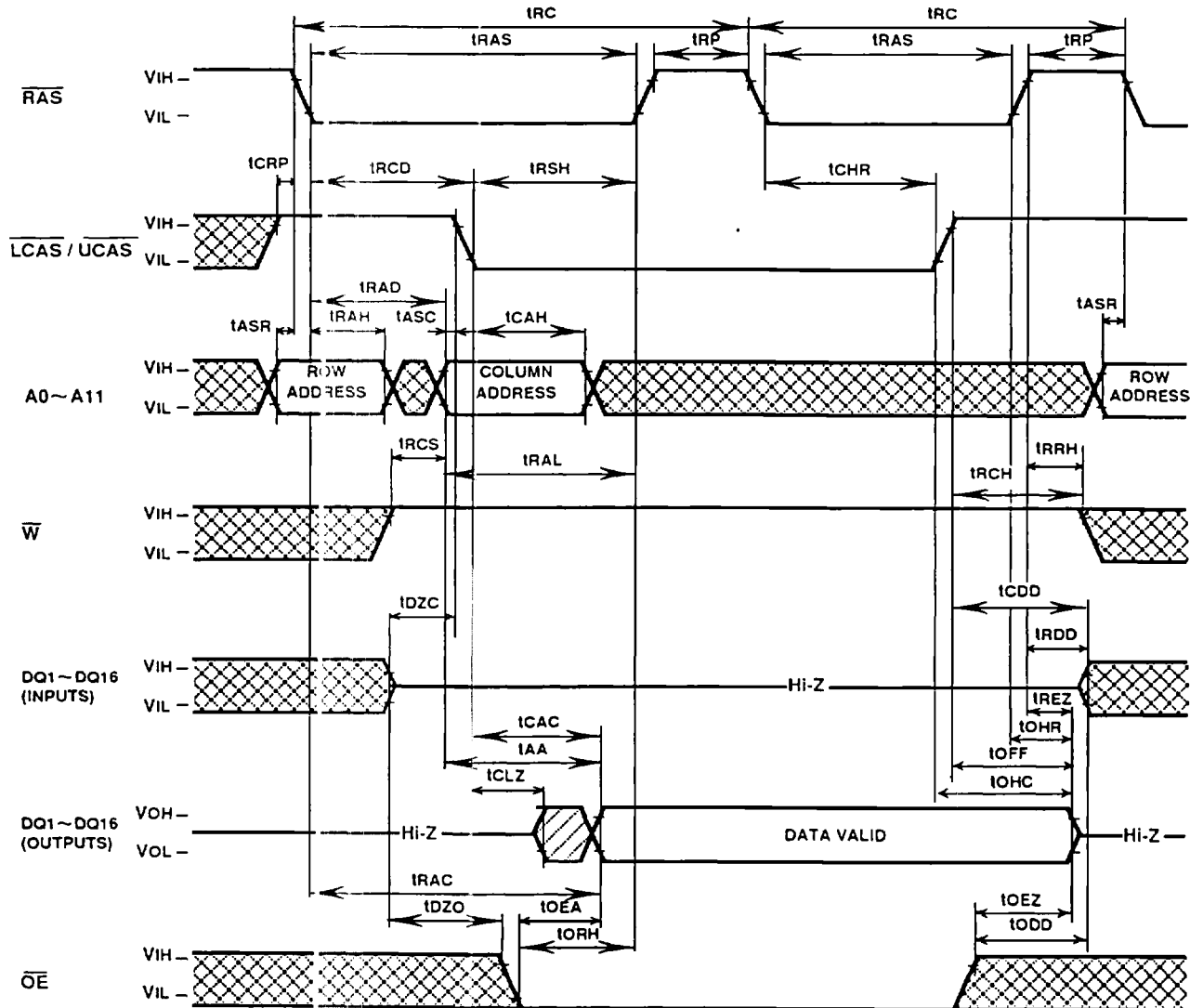
## $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle, Extended Refresh Cycle\*



# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## Hidden Refresh Cycle (Fead) (Note 30)

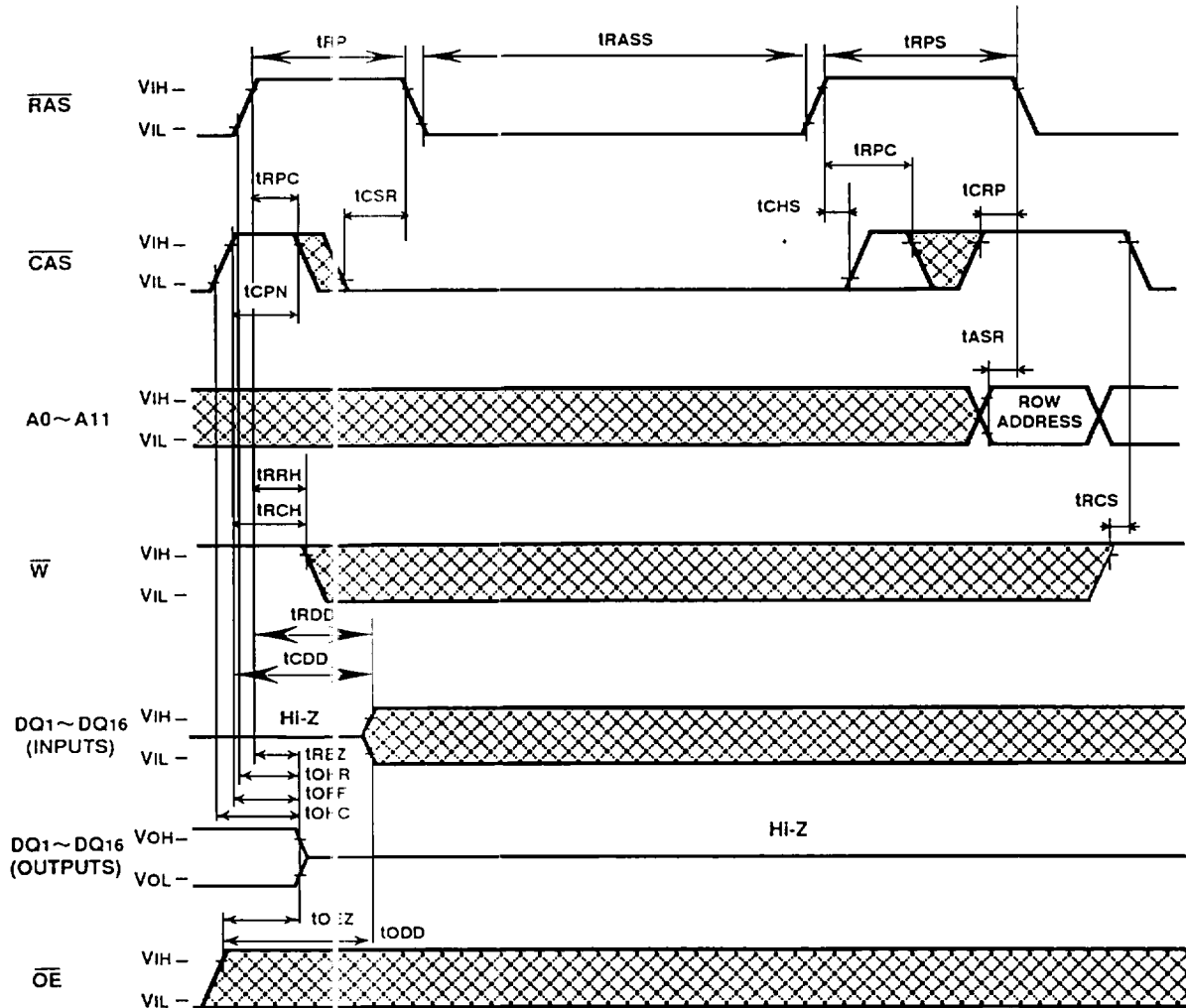


Note 30: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle. Timing requirements and output state are the same as that of each cycle shown above.

# M5M4V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 1677216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## Self Refresh Cycle\* (31)



# M5M4-V16165BJ, TP-6, -7, -8, -6S, -7S, -8S

HYPER PAGE MODE 16777216-BIT ( 1048576-WORD BY 16-BIT ) DYNAMIC RAM

## SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S / -8S. The other characteristics and requirements than the below are same as normal devices.

### ELECTRICAL CHARACTERISTICS (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>CCS</sub> (AV)	Average supply current from V <sub>CC</sub> Self-Refresh cycle	M5M4V16165B ( S ) $\overline{RAS} = \overline{CAS} \leq 0.2V$			200	μA

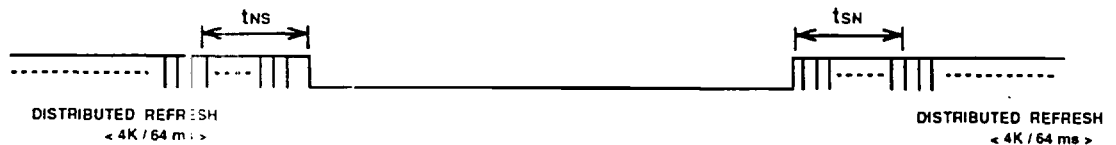
### TIMING REQUIREMENT (Ta=0 ~ 70°C, Vcc=3.3V ± 0.3V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V16165B-6S		M5M4V16165B-7S		M5M4V16165B-8S		
		Min	Max	Min	Max	Min	Max	
t <sub>RASS</sub>	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t <sub>RPS</sub>	Self Refresh $\overline{RAS}$ high precharge time	110		130		150		ns
t <sub>CHS</sub>	Self Refresh $\overline{RAS}$ hold time	-50		-50		-50		ns

## SELF REFRESH ENTRY & EXIT CONDITIONS

### (1) In case of distributed refresh

The last / first full refresh cycles (4K) must be made within t<sub>NS</sub> / t<sub>SN</sub> before / after self refresh, on the condition of t<sub>NS</sub> ≤ 64 ms and t<sub>SN</sub> ≤ 64 ms.



### (2) In case of burst refresh

The last / first full refresh cycles (4K) must be made within t<sub>NS</sub> / t<sub>SN</sub> before / after self refresh, on the condition of t<sub>NS</sub> + t<sub>SN</sub> ≤ 64 ms.

