

**'F550 Octal Registered Transceiver With Status Flags,
Non-Inverting**
**'F551 Octal Registered Transceiver With Status Flags,
Inverting**
Preliminary Specification

FAST Products

FEATURES

- 8-bit bidirectional I/O port with handshake
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags
- 'F550 non-inverting 'F551 inverting
- B outputs sink 64mA

DESCRIPTION

The 'F550 and 'F551 octal transceivers contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own Clock (CPA, CPB) and Clock Enable (\overline{CEA} , \overline{CEB}) inputs as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate Output Enable (\overline{OEA} , \overline{OEB}) for its 3-State buffers. The separate Clocks, Flags and Enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

| TYPE | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|--------|---------------------------|--------------------------------|
| 74F550 | 6.3ns | 130mA |
| 74F551 | 6.3ns | 130mA |

ORDERING INFORMATION

| PACKAGE | COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$; $T_A = 0^\circ C$ to $+70^\circ C$ |
|--------------------|---|
| 28-Pin Plastic DIP | N74F550N, N74F551N |
| 28-Pin Plastic SOL | N74F550D, N74F551D |

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

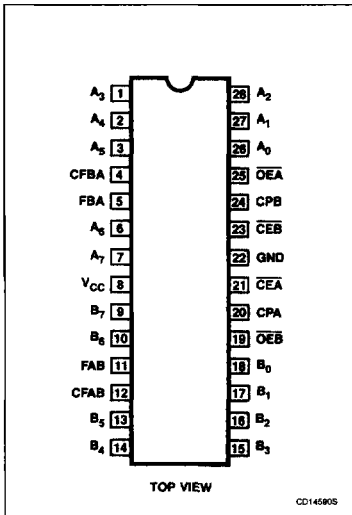
| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---------------------------------|--|------------------------|------------------------|
| A ₀ - A ₇ | A-to-B Data inputs | 3.5/1.0 | 70 μ A/0.6mA |
| B ₀ - B ₇ | B-to-A Data inputs | 3.5/1.0 | 70 μ A/0.6mA |
| CPA | A-to-B Clock input (active rising edge) | 1.0/1.0 | 20 μ A/0.6mA |
| CPB | B-to-A Clock input (active rising edge) | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{CEA} | A-to-B Clock Enable input (active-Low) | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{CEB} | B-to-A Clock Enable input (active-Low) | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{OEA} | A-to-B Output Enable input (active-Low) | 1.0/1.0 | 20 μ A/0.6mA |
| \overline{OEB} | B-to-A Output Enable input (active-Low) | 1.0/1.0 | 20 μ A/0.6mA |
| CFAB | A-to-B Flag Clear input (active rising edge) | 1.0/1.33 | 20 μ A/0.8mA |
| CFBA | B-to-A Flag Clear input (active rising edge) | 1.0/1.33 | 20 μ A/0.8mA |
| A ₀ - A ₇ | A-to-B Data outputs | 150/40 | 3mA/24mA |
| B ₀ - B ₇ | B-to-A Data outputs | 150/40 | 3mA/24mA |
| FAB | A-to-B Status Flag output (active-High) | 50/33.3 | 1mA/20mA |
| FBA | B-to-A Output Enable input (active-High) | 50/33.3 | 1mA/20mA |

NOTE:

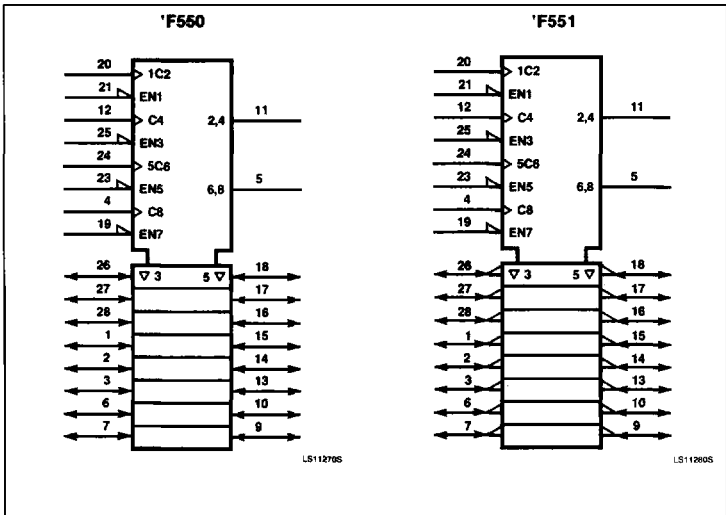
1. One (1.0) FAST Unit Load is defined as: 20 μ A in the High state and 0.6mA in the Low state.

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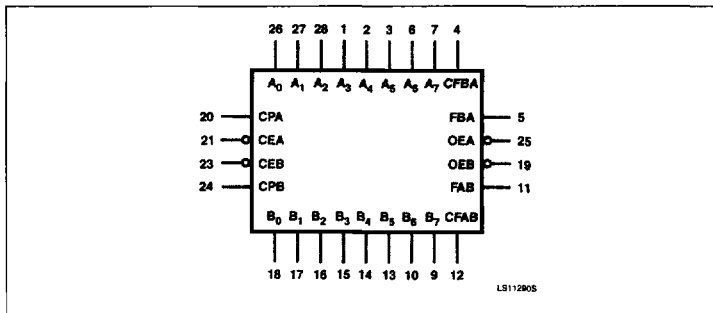
PIN CONFIGURATION



SYMBOL (IEEE/IEC)

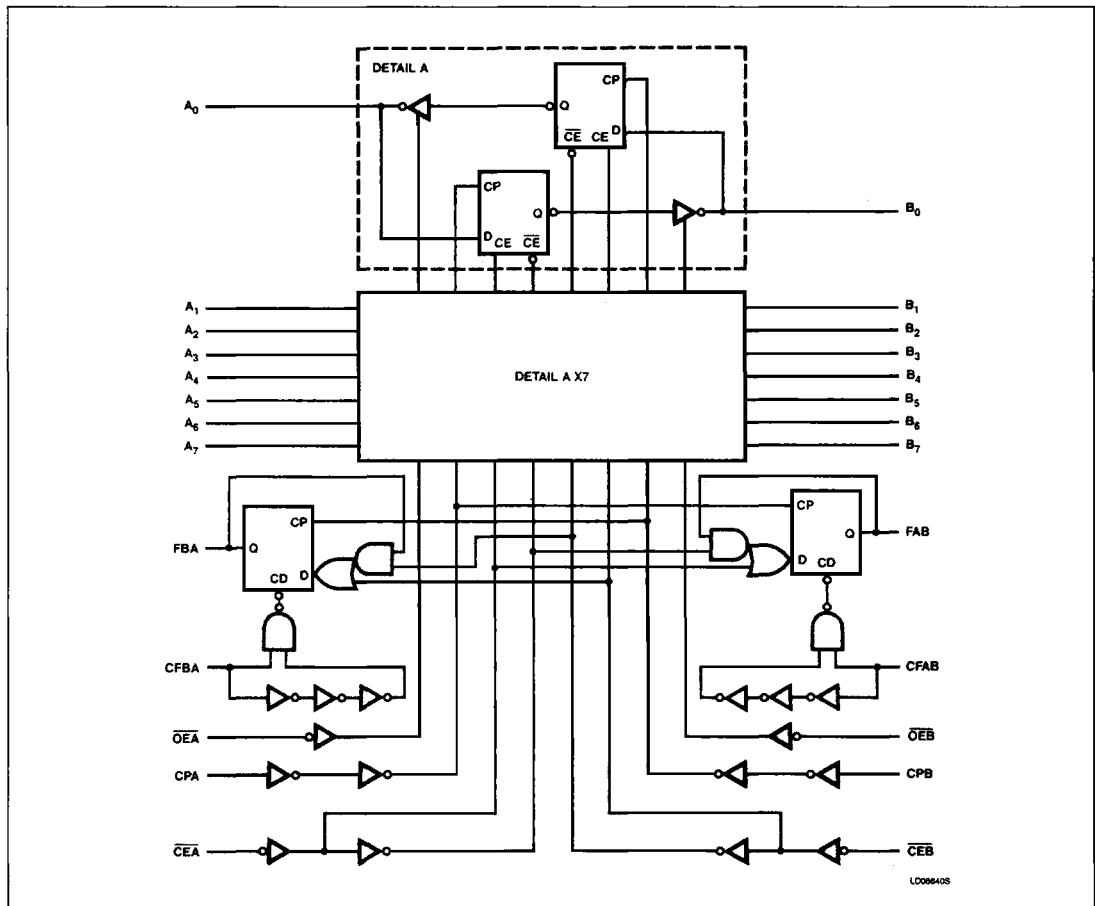


LOGIC SYMBOL



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LOGIC DIAGRAM for 'F550

**FUNCTIONAL DESCRIPTION**

Data applied to the A inputs are entered and stored on the rising edge of the A Clock (CPA), provided that the A Clock Enable ($\overline{\text{CEA}}$) is Low; simultaneously, the status flip-flop is set and the A-to-B Flag (FAB) output goes High. Data entered from the A inputs is present at the inputs to the B output buffers,

but only appears on the B I/O pins when the B Output Enable ($\overline{\text{OEB}}$) signal is made Low. After the B output data is assimilated, the receiving system clears the A-to-B Flag flip-flop by applying a Low-to-High transition to the CFAB input. Optionally, the OEA and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{\text{CEB}}$ and CPB enter the B input data and set the B-to-A Flag (FBA) output High. A Low signal on $\overline{\text{OEA}}$ enables the A output buffers and a Low-to-High transition on CFBA clears the FBA Flag.

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FUNCTION TABLE

| OPERATING MODE | INPUTS | | | INTERNAL Q |
|----------------|--------|----|-----------------|------------|
| | A or B | CP | \overline{CE} | |
| Hold data | X | X | H | No change |
| Load data | L | ↑ | L | L |
| | H | ↑ | L | H |

FLAG FUNCTION TABLE

| OPERATING MODE | INPUTS | | | FLAG OUTPUT |
|----------------|--------|----|-----------------|-------------|
| | CF | CP | \overline{CE} | |
| Hold Flag | ↓ | X | H | No change |
| Clear Flag | ↑ | X | X | L |
| Set Flag | ↓ | ↑ | L | H |

OUTPUT CONTROL TABLE

| OPERATING MODE | \overline{OE} | INTERNAL Q | OUTPUT | |
|-----------------|-----------------|------------|--------|-------|
| | | | 'F550 | 'F551 |
| Disable outputs | H | X | Z | Z |
| Enable outputs | L | L | L | H |
| | L | H | H | L |

H = High Voltage Level

L = Low Voltage Level

X = Don't care

Z = High-Impedance

↑ = Low-to-High Transition

↓ = Doesn't allow Low-to-High Transition

ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RATING | UNIT |
|-----------|--|------------------------|------|
| V_{CC} | Supply voltage | -0.5 to +7.0 | V |
| V_{IN} | Input voltage | -0.5 to +7.0 | V |
| I_{IN} | Input current | -30 to +5 | mA |
| V_{OUT} | Voltage applied to output in High output state | -0.5 to + V_{CC} | V |
| I_{OUT} | Current applied to output in Low output state | FAB, FBA | 40 |
| | | $A_0 - A_7, B_0 - B_7$ | 48 |
| T_A | Operating free-air temperature range | 0 to +70 | °C |

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | LIMITS | | | UNIT |
|-----------------|--------------------------------|---|-----|-----|------|
| | | Min | Nom | Max | |
| V _{CC} | Supply voltage | 4.5 | 5.0 | 5.5 | V |
| V _{IH} | High-level input voltage | 2.0 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| I _{IK} | Input clamp current | | | -18 | V |
| I _{OH} | High-level output current | FAB, FBA | | -1 | mA |
| | | A ₀ -A ₇ , B ₀ -B ₇ | | -3 | |
| I _{OL} | Low-level output current | FAB, FBA | | 20 | mA |
| | | A ₀ -A ₇ , B ₀ -B ₇ | | 24 | |
| T _A | Operating free-air temperature | 0 | | 70 | °C |

DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS ¹ | 74F550, 74F551 | | | UNIT | |
|------------------------------------|---|--|---|------------------|------|------|----|
| | | | Min | Typ ² | Max | | |
| V _{OH} | High-level output voltage | V _{CC} = MIN V _{IL} = MAX I _{OH} = MAX V _{IH} = MIN | ± 10%V _{CC} | 2.5 | | V | |
| | | | ± 5%V _{CC} | 2.7 | 3.4 | V | |
| V _{OL} | Low-level output voltage | V _{CC} = MIN V _{IL} = MAX, I _{OL} = MAX V _{IH} = MIN | ± 10%V _{CC} | | 0.35 | 0.50 | V |
| | | | ± 5%V _{CC} | | 0.35 | 0.50 | V |
| V _{IK} | Input clamp voltage | V _{CC} = MIN, I _I = I _{IK} | | -0.73 | -1.2 | V | |
| I _I | Input current at maximum input voltage | Others | V _{CC} = MAX, V _I = 7.0V | | | 100 | μA |
| | | A ₀ -A ₇ , B ₀ -B ₇ | V _{CC} = 5.5V, V _I = 5.5V | | | 1.0 | mA |
| I _{IH} | High-level input current | except A ₀ -A ₇ B ₀ -B ₇ | V _{CC} = MAX, V _I = 2.7V | | | 20 | μA |
| I _{IL} | Low-level input current | | V _{CC} = MAX, V _I = 0.5V | | | -600 | μA |
| I _{IH} + I _{OZH} | High-level input current | A ₀ -A ₇ B ₀ -B ₇ | V _{CC} = MAX, V _O = 2.7V | | | 70 | μA |
| I _{IL} + I _{OZL} | Low-level input current | | V _{CC} = MAX, V _O = 0.5V | | | -600 | μA |
| I _{OS} | Short-circuit output current ³ | V _{CC} = MAX | | -80 | | -150 | mA |
| I _{CC} | Supply current | V _{CC} = MAX | | | 130 | 190 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value under the recommended operating conditions for the applicable conditions.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} should be performed last.

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AC ELECTRICAL CHARACTERISTICS

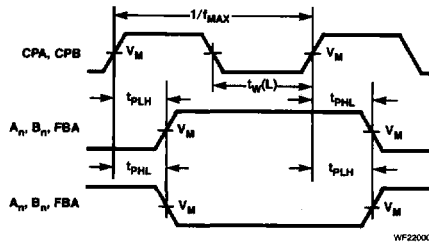
| SYMBOL | PARAMETER | TEST CONDITIONS | 74F550, 74F551 | | | | | UNIT |
|--------------------------------------|---|-----------------|--|------------|------------|--|-------------|------|
| | | | T _A = +25°C V _{CC} = 5.0V C _L = 50pF R _L = 500Ω | | | T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum operating frequency | Waveform 1 | 60 | 70 | | 50 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CPA or CPB to B _n or A _n | Waveform 1 | 3.0 4.0 | 5.5 7.0 | 7.5 9.0 | 2.5 3.5 | 8.5 10.0 | ns |
| t _{PLH} | Propagation delay CPA or CPB to FAB or FBA | Waveform 1 | 3.5 | 6.0 | 6.0 | 3.0 | 9.0 | ns |
| t _{PHL} | Propagation delay CFAB or CFBA to FAB or FBA | Waveform 2 | 5.0 | 9.0 | 11.5 | 4.5 | 13.0 | ns |
| t _{PZH} t _{PZL} | Output enable time OE _A or OE _B to A _n or B _n | Waveform 4, 5 | 2.5 3.5 | 5.5 7.0 | 7.5 9.5 | 2.0 3.0 | 8.5 10.5 | ns |
| t _{PHZ} t _{PLZ} | Output Disable time OE _A or OE _B to A _n or B _n | Waveform 4, 5 | 3.0 2.5 | 6.5 5.5 | 9.0 7.5 | 2.5 2.0 | 10.0 8.5 | ns |

AC SETUP REQUIREMENTS

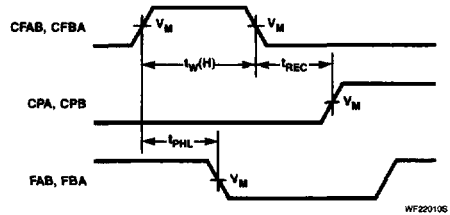
| SYMBOL | PARAMETER | TEST CONDITIONS | 74F550, 74F551 | | | | | UNIT |
|--|---|-----------------|--|-----|-----|--|-----|------|
| | | | T _A = +25°C V _{CC} = 5.0V C _L = 50pF R _L = 500Ω | | | T _A = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF R _L = 500Ω | | |
| | | | Min | Typ | Max | Min | Max | |
| t _s (H) t _s (L) | Setup time, High or Low A _n or B _n to CPA or CPB | Waveform 3 | 4.0 4.0 | | | 4.5 4.5 | | ns |
| t _h (H) t _h (L) | Hold time, High or Low A _n or B _n to CPA or CPB | Waveform 3 | 2.0 2.0 | | | 2.5 2.5 | | ns |
| t _s (H) t _s (L) | Setup time, High or Low CE _A or CE _B to CPA or CPB | Waveform 3 | 4.0 4.0 | | | 4.5 4.5 | | ns |
| t _h (H) t _h (L) | Hold time, High or Low CE _A or CE _B to CPA or CPB | Waveform 3 | 2.0 2.0 | | | 2.5 2.5 | | ns |
| t _w (H) t _w (L) | Pulse width, High or Low CPA or CPB | Waveform 3 | 3.0 3.0 | | | 3.5 3.5 | | ns |
| t _w (H) | Pulse width, High CFAB or CFBA | Waveform 2 | 3.0 | | | 3.5 | | ns |
| t _{rec} | Recovery time CFAB or CFBA to CPA or CPB | Waveform 2 | 9.0 | | | 10.0 | | ns |

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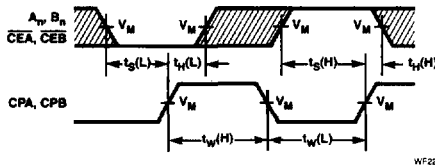
AC WAVEFORMS



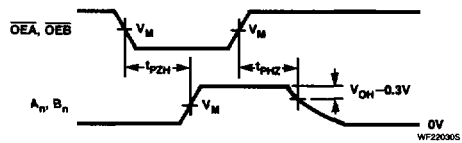
Waveform 1. Propagation Delay, Clock Input to Output



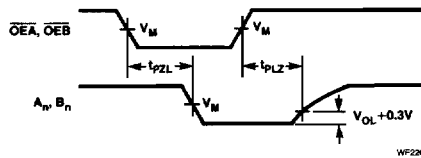
Waveform 2. Propagation Delay, Flag Clear Input to Status Flag Output, Recovery Time Flag Clear Input to Clock Output



Waveform 3. Data Setup Time and Hold Times, and Clock Pulse Widths



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level



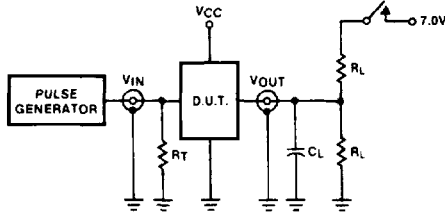
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time From Low Level

NOTE: $V_M = 1.5V$.

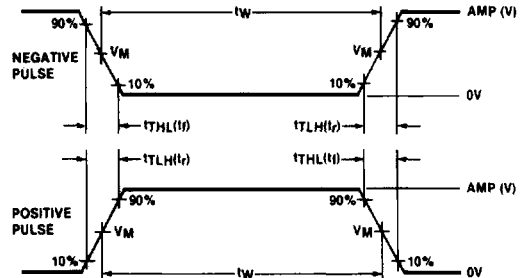
The shaded area indicate when the input is permitted to change for predictable output performance.

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TEST CIRCUIT AND WAVEFORMS



WF064715



WF064505

Test Circuit for 3-State Outputs

SWITCH POSITION

| TEST | SWITCH |
|-----------|--------|
| t_{pLZ} | closed |
| t_{pZL} | closed |
| All other | open |

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.
 C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
 R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

$V_M = 1.5V$
Input Pulse Definition

| FAMILY | INPUT PULSE REQUIREMENTS | | | | |
|--------|--------------------------|-----------|-------------|-----------|-----------|
| | Amplitude | Rep. Rate | Pulse Width | t_{TLH} | t_{THL} |
| 74F | 3.0V | 1MHz | 500ns | 2.5ns | 2.5ns |