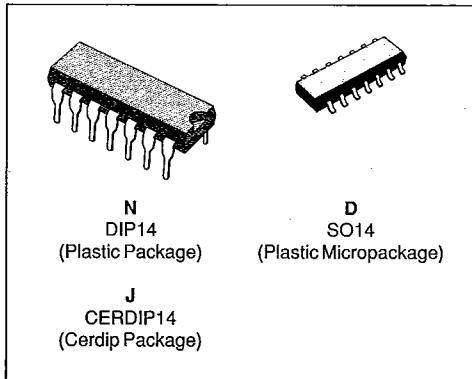


S G S - THOMSON**30E D****LOW POWER QUAD CMOS OP-AMPS**

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMETRICAL OUTPUT CURRENTS
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN TO PIN COMPATIBLE WITH STANDARD QUAD OP-AMPs (TL084 -LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10mV), A (5mV), B (2mV)

**ORDER CODES**

| Part Number | Temperature Range | Package | | |
|---------------|-------------------|---------|---|---|
| | | N | J | D |
| TS27M4C/AC/BC | 0°C to + 70°C | • | • | • |
| TS27M4I/AI/BI | - 40°C to + 105°C | • | • | • |
| TS27M4M/AM/BM | - 55°C to + 125°C | • | • | • |

Example : TS27M4ACN

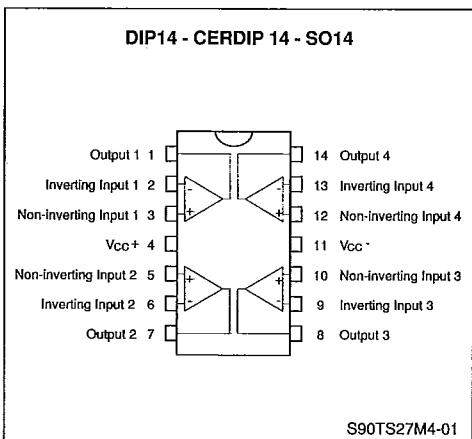
DESCRIPTION

The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio :

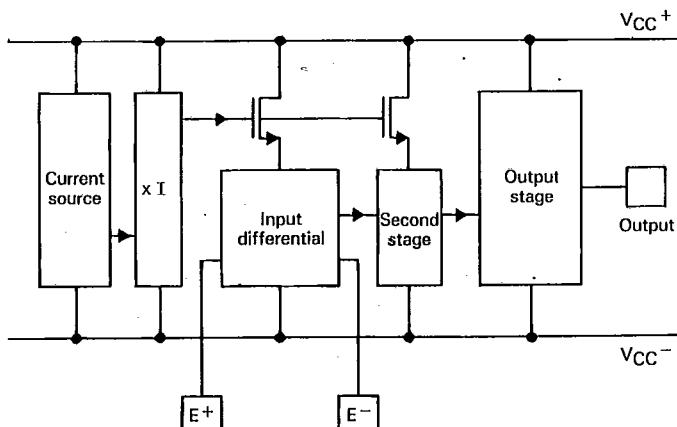
- Icc= 10µA/amp. : TS27L4 (very low power)
- Icc= 150µA/amp. : TS27M4 (low power)
- Icc= 1mA/amp. : TS274 (high speed)

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

PIN CONNECTIONS (Top view)

BLOCK DIAGRAM

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S90TS27M4-02

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|------------------------------|---|---|---|
| V _{CC} ⁺ | Supply Voltage (Note 1) | 18 | V |
| V _{Id} | Differential Input Voltage (Note 2) | ± 18 | V |
| V _i | Input Voltage (Note 3) | - 0.3 to 18 | V |
| I _o | Output Current for V _{CC} ⁺ ≥ 15V | ± 30 | mA |
| T _{oper} | Operating Free-Air Temperature Range | TS27M4C/AC/BC TS27M4I/AI/BI TS27M4M/AM/BM | 0 to + 70 - 40 to + 105 - 55 to + 125 |
| T _{stg} | Storage Temperature Range | - 65 to + 150 | °C |

- Notes :
1. All voltage values, except differential voltage, are with respect to network ground terminal.
 2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
 3. The magnitude of the input and the output voltages must never exceed the magnitude of the positive supply voltage.

OPERATING CONDITIONS

| Symbol | Parameter | Value | Unit |
|------------------------------|---------------------------------|---|------|
| V _{CC} ⁺ | Supply Voltage | 3* to 16 | V |
| V _{ic} | Common Mode Input Voltage Range | 0 to V _{CC} ⁺ - 1.5 | V |

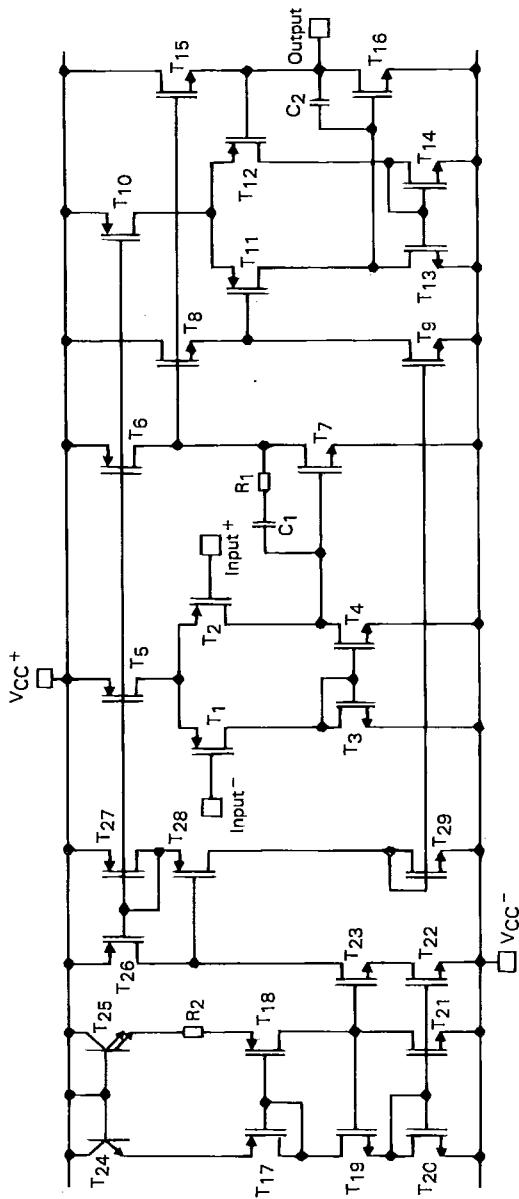
* Selected devices only.

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SCHEMATIC DIAGRAM (for 1/4 TS27M4)

T-79-08



S90TS27M4-03

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ELECTRICAL CHARACTERISTICS $V_{CC^+} = +10V, V_{CC^-} = 0V, T_{AMB} = 25^\circ C$ (unless otherwise specified)

| Symbol | Parameter | TS27M4C/AC/BC | | | TS27M4I/AI/BI TS27M4M/AM/BM | | | Unit |
|-----------------|---|---|-------------|------------|---|-------------|------------|------------------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| V_{IO} | Input Offset Voltage $V_o = 1.4V, V_i = 0V$ | TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM | 1.1 | 10 | TS27M4C/I/M TS27M4AC/AI/AM TS27M4BC/BI/BM | 1.1 | 10 | mV |
| | $T_{MIN} \leq T_{AMB} \leq T_{MAX}$ | | 0.9 0.25 | 5 2 | | 0.9 0.25 | 5 2 | |
| DV_{IO} | Input Offset Voltage Drift | | 2 | | | 2 | | $\mu V/^\circ C$ |
| I_{IO} | Input Offset Current $V_i = 5V, V_o = 5V$ | | 1 | 100 | | 1 | 200 | pA |
| I_{IB} | Input Bias Current $V_i = 5V, V_o = 5V$ | | 1 | 150 | | 1 | 300 | pA |
| V_{OH} | High Level Output Voltage $V_i = 10mV, R_L = 100k\Omega$ | 8.7 8.6 | 8.9 | | 8.7 8.5 | 8.9 | | V |
| V_{OL} | Low Level Output Voltage $V_i = -10mV$ | | | 50 | | | 50 | mV |
| A_{vd} | Large Signal Voltage Gain $V_o = 1V$ to $6V, R_L = 100k\Omega, V_i = 5V$ | 30 20 | 50 | | 30 10 | 50 | | V/mV |
| GBP | Gain Bandwidth Product $A_v = 40dB, R_L = 100k\Omega, C_L = 100pF$ $f_{in} = 100 kHz$ | | 1 | | | 1 | | MHz |
| CMR | Common Mode Rejection Ratio $V_o = 1.4V, V_i = 1V$ to $7.4V$ | 65 | 80 | | 65 | 80 | | dB |
| SVR | Supply Voltage Rejection Ratio $V_{CC^+} = 5V$ to $10V, V_o = 1.4V$ | 60 | 80 | | 60 | 80 | | dB |
| I_{CC} | Supply Current (per amplifier) $A_v = 1$, no load, $V_o = 5V$ | | 150 | 200 250 | | 150 | 200 300 | μA |
| I_o | Output Short Circuit Current $V_i = 10mV, V_o = 0V$ | 45 | 60 | 85 | 45 | 60 | 85 | mA |
| I_{sink} | Output Sink Current $V_i = -10mV, V_o = V_{CC}$ | 35 | 45 | 65 | 35 | 45 | 65 | mA |
| S_{vo} | Slew-Rate at Unity Gain $R_L = 100k\Omega, C_L = 100pF$ | | | 0.6 | | | 0.6 | $V/\mu s$ |
| $\emptyset m$ | Phase Margin at Unity Gain $A_v = 40 dB, R_L = 100k\Omega, C_L = 100pF$ | | 45 | | | 45 | | degrees |
| K_{ov} | Overshoot Factor | | 30 | | | 30 | | % |
| V_n | Equivalent Input Noise Voltage $f = 1kHz, R_S = 10\Omega$ | | 38 | | | 38 | | nV/\sqrt{Hz} |
| V_{O1}/V_{O2} | Cross Talk Attenuation | | 120 | | | 120 | | dB |

TYPICAL CHARACTERISTICS

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Figure 1 : Supply Current (each amplifier) versus Supply Voltage.

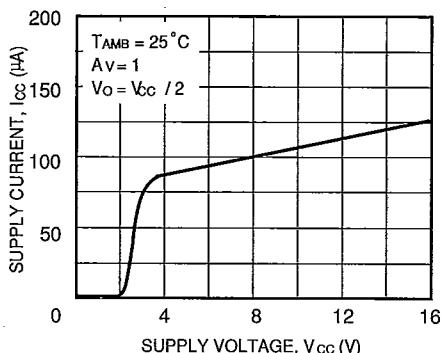


Figure 3a : High Level Output Voltage versus High Level Output Current.

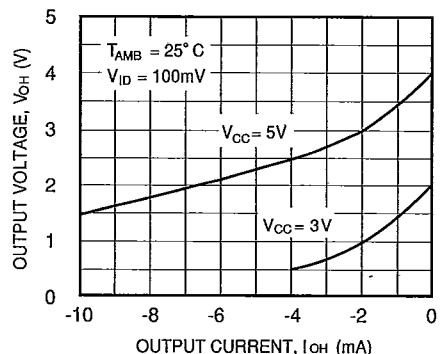


Figure 4a : Low Level Output Voltage versus Low Level Output Current.

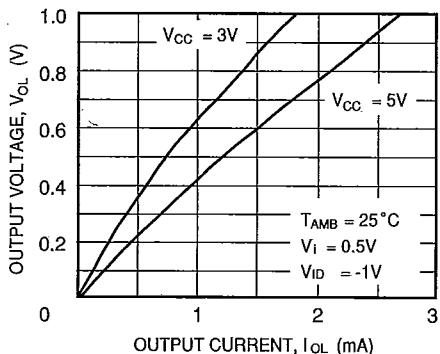


Figure 2 : Input Bias Current versus Free Air Temperature.

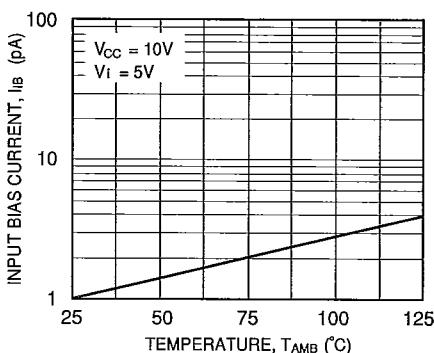


Figure 3b : High Level Output Voltage versus High Level Output Current.

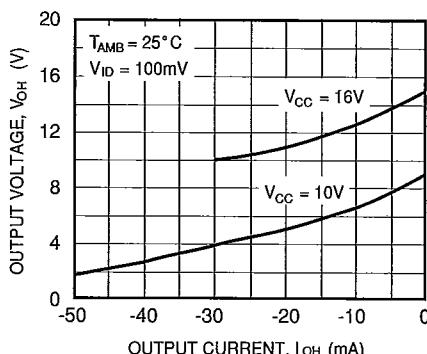
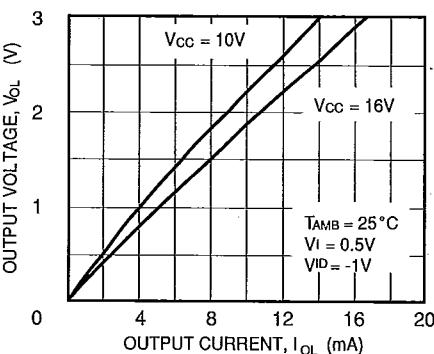


Figure 4b : Low Level Output Voltage versus Low Level Output Current.



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TYPICAL CHARACTERISTICS (continued)

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Figure 5 : Open Loop Frequency Response and Phase Shift.

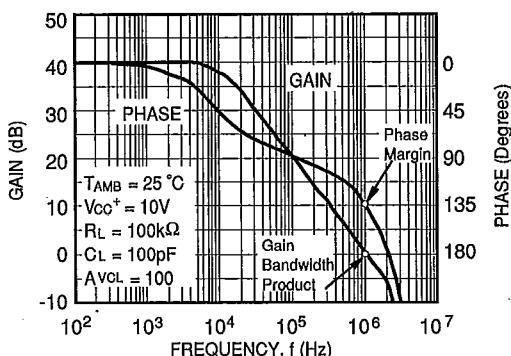


Figure 6 : Gain Bandwidth Product versus Supply Voltage.

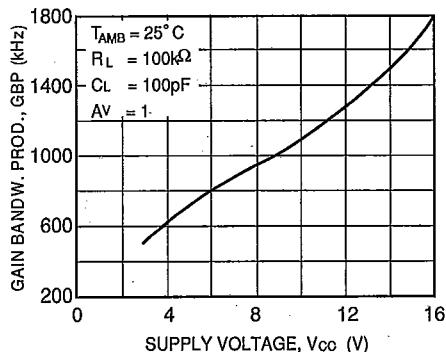


Figure 8 : Phase Margin versus Capacitive Load.

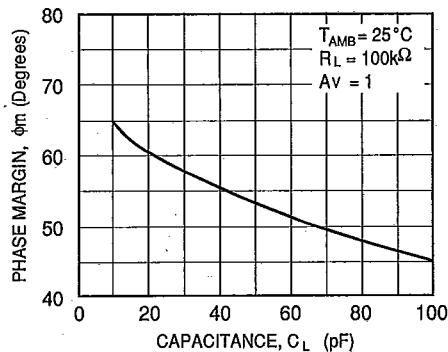


Figure 7 : Phase Margin versus Supply Voltage.

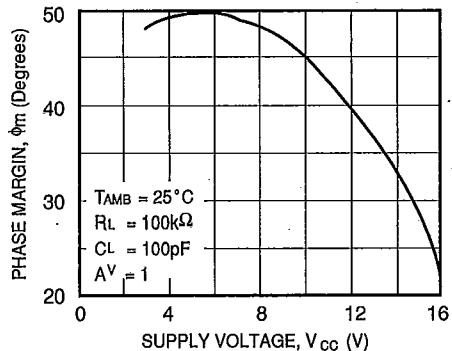
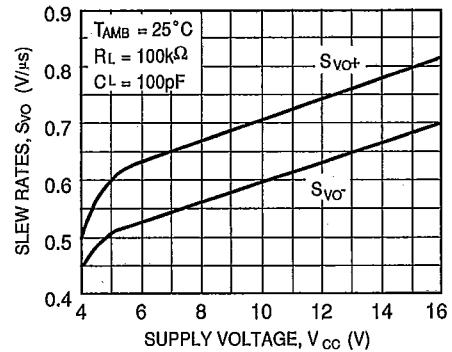


Figure 9 : Slew Rates versus Supply Voltage.

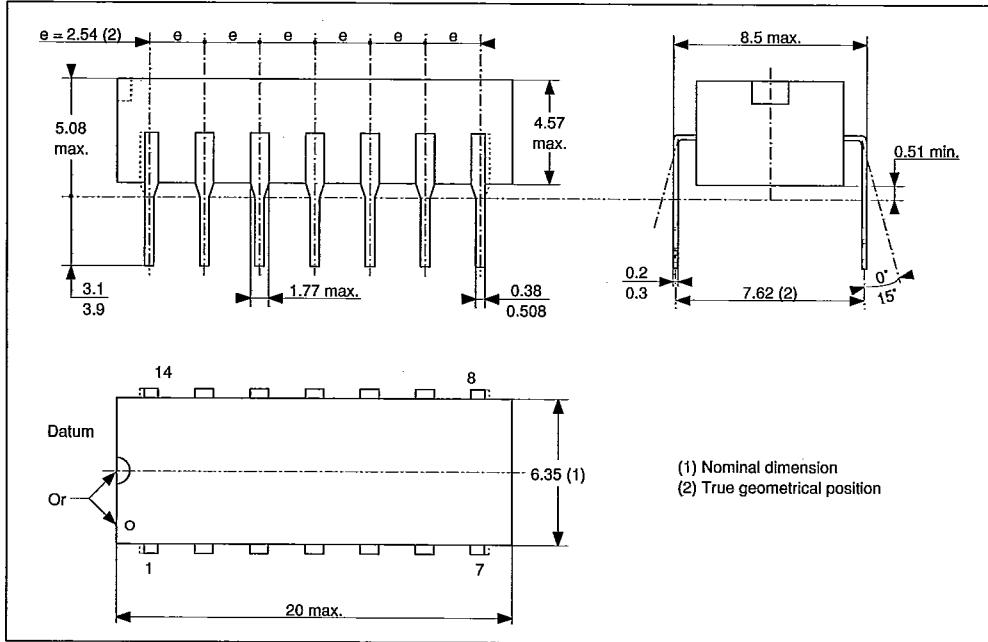


PACKAGE MECHANICAL DATA

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14 PINS - PLASTIC DIP OR CERDIP



14 PINS - PLASTIC MICROPACKAGE (SO)

