



Integrated Device Technology, Inc.

LOW SKEW PLL-BASED CMOS CLOCK DRIVER

IDT54/74FCT88915
55/70/100/133
PRELIMINARY

FEATURES:

- 0.5 MICRON CMOS Technology
- Input frequency range: 2.5MHz – f_{2Q} Max. spec
- Max. output frequency: 133MHz
- Pin and function compatible with MC88915
- 5 non-inverting outputs, one inverted output, one 2x output, one +2 output; all outputs are TTL-compatible
- Output skew < 500ps (max.)
- Duty cycle distortion < 500ps (max.)
- Part-to-part skew: 0.55ns (from t_{PD} max. spec)
- 36/-36mA drive at CMOS output voltage levels
- Available in 28 pin PLCC, LCC and SSOP packages

DESCRIPTION:

The IDT54/74FCT88915 uses phase-lock loop technology to lock the frequency and phase of outputs to the input reference clock. It provides low skew clock distribution for high performance PCs and workstations. One of the outputs

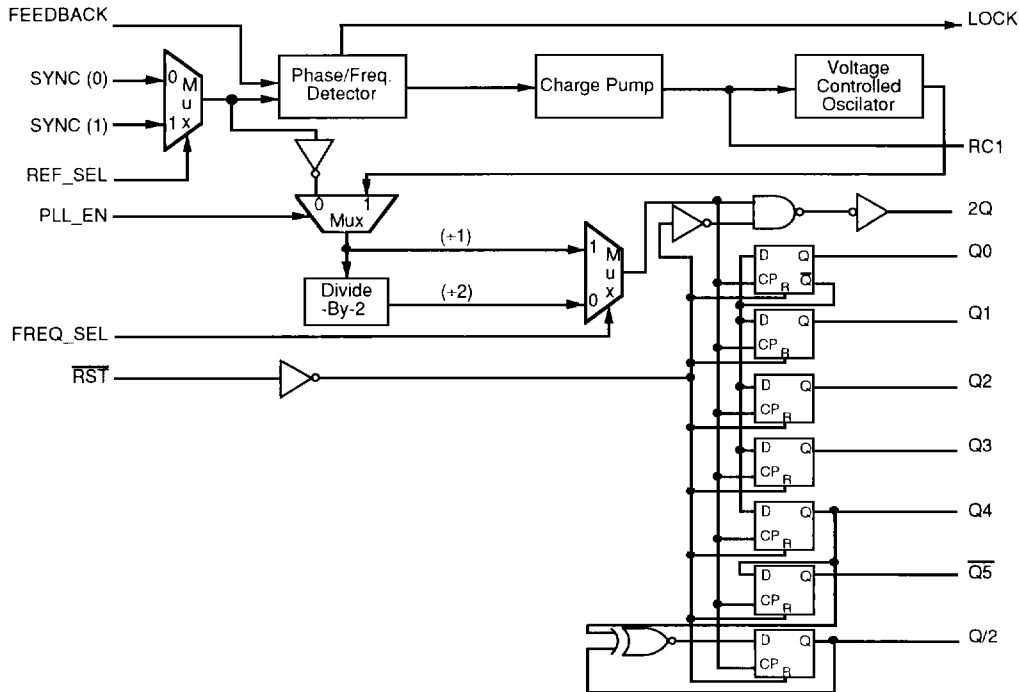
is fed back to the PLL at the FEEDBACK input resulting in essentially zero delay across the device. The PLL consists of the phase/frequency detector, charge pump, loop filter and VCO. The VCO is designed to run optimally between 20 MHz and f_{2Q} Max.

The IDT54/74FCT88915 provides 8 outputs with 500ps skew. The Q₅ output is inverted from the Q outputs. The 2Q runs at twice the Q frequency and Q/2 runs at half the Q frequency.

The FREQ_SEL control provides an additional +2 option in the output path. PLL_EN allows bypassing of the PLL, which is useful in static test modes. When PLL_EN is low, SYNC input may be used as a test clock. In this test mode, the input frequency is not limited to the specified range and the polarity of outputs is complementary to that in normal operation (PLL_EN = 1). The LOCK output attains logic HIGH when the PLL is in steady-state phase and frequency lock.

The IDT54/74FCT88915 requires external loop filter components as recommended in Figure 5.

FUNCTIONAL BLOCK DIAGRAM



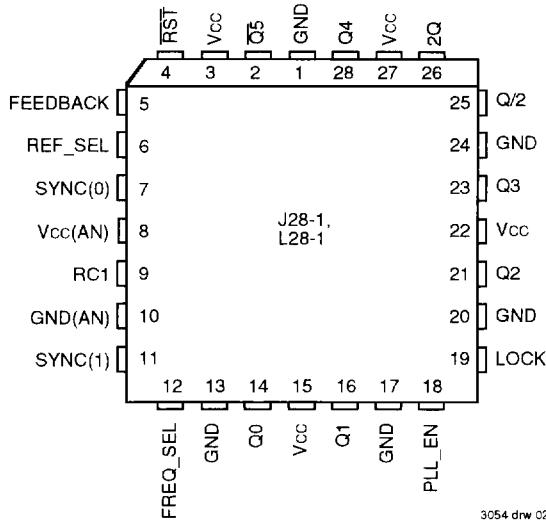
3054 drw 01

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

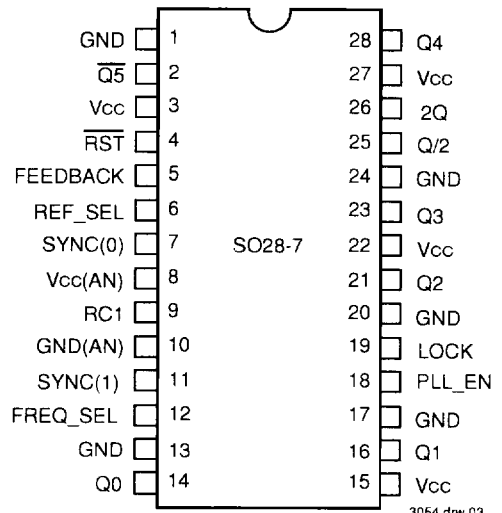
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PIN CONFIGURATIONS



PLCC/LCC
TOP VIEW

3054 drw 02



SSOP
TOP VIEW

3054 drw 03

PIN DESCRIPTION

Pin Name	I/O	Description
SYNC(0)	I	Reference clock input.
SYNC(1)	I	Reference clock input.
REF_SEL	I	Chooses reference between SYNC (0) & SYNC (1). (Refer to functional block diagram).
FREQ_SEL	I	Selects between + 1 or + 2 frequency options. (Refer to functional block diagram).
FEEDBACK	I	Feedback input to phase detector.
RC1	I	Input for external RC network (loop filter connection).
Q0-Q4	O	Clock outputs.
Q5	O	Inverted clock output.
2Q	O	Clock output (2 x Q frequency).
Q/2	O	Clock output (Q frequency + 2).
LOCK	O	Indicates phase lock has been achieved (HIGH when locked).
RST	I	Asynchronous reset (Active LOW).
PLL_EN	I	Disables phase-lock for low frequency testing. (Refer to functional block diagram).

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	-0.5 to V _{CC} +0.5	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	-60 to +120	mA

NOTES: 3054 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals.
- Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

NOTE: 3054 lmk 03

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _I = V _{CC} V _I = GND	—	—	±1	μA
I _{IL}	Input LOW Current		—	—	±1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = Max., V _{OH} = 3.85V ⁽³⁾	-88	—	—	mA
I _{ODL}	Output LOW Current	V _{CC} = Max., V _{OL} = 1.0V ⁽³⁾	88	—	—	mA
V _H	Input Hysteresis	—	—	100	—	mV
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -36mA	V _{CC} - 75	4.55	—	V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 36mA	—	0.27	0.44	V
I _{CC1}	Quiescent Power Supply Current	V _{CC} = Max., V _{IN} = GND or V _{CC} (Test mode, RC1 connected to GND)	—	2.0	4.0	mA
I _{CC2}						

NOTES: 3054 tbl 04

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.



POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = V_{CC} - 2.1V^{(3)}$		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ All Outputs Open	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.5	0.7	mA/ MHz
CPD	Power Dissipation Capacitance	50% Duty Cycle		—	25	40	pF
I_C	Total Power Supply Current ^(5,6)	$V_{CC} = \text{Max.}$ PLL_EN = 1, LOCK = 1, FEEDBACK = Q4 SYNC frequency = 50MHz. Q4 loaded with 50pF All other outputs open		—	65	80	mA
		$V_{CC} = \text{Max.}$ PLL_EN = 1, LOCK = 1, FEEDBACK = Q4 SYNC frequency = 50MHz. Q4 loaded with 50 Ω Thevenin termination. All other outputs open		—			mA
P _{D1}	Power Dissipation	50 Ω Thevenin termination @ 33MHz		—	120	—	mW
P _{D2}	Power Dissipation	50 Ω parallel termination to GND @ 33MHz		—	300	—	mW

3054 tbl 05

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
- Typical values are at $V_{CC} = 5.0V$, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations. It is derived with Q frequency as the reference.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot DH_{NT} + I_{CCD}(f) + I_{LOAD}$
 $I_{CC} = \text{Quiescent Current (} I_{CC1}, I_{CC2} \text{ and } I_{CC3} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $DH = \text{Duty Cycle for TTL Inputs High}$
 $NT = \text{Number of TTL Inputs at DH}$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f = 2Q \text{ frequency}$
 $I_{LOAD} = \text{Dynamic Current due to load.}$

SYNC INPUT TIMING REQUIREMENTS

Symbol	Parameter	Min.	Max.	Unit
$T_{RISE/FALL}$	Rise/Fall Times, SYNC inputs (0.8V to 2.0V)	—	3.0	ns
Frequency	Input Frequency, SYNC Inputs	2.5 ⁽¹⁾	2Q f _{max}	MHz
Duty Cycle	Input Duty Cycle, SYNC Inputs	25%	75%	—

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OUTPUT FREQUENCY SPECIFICATIONS

Symbol	Parameter	Min.	Max. ⁽²⁾				Unit
			55	70	100	133	
f _{2Q}	Operating frequency 2Q Output	10	55	70	100	133	MHz
f _Q	Operating frequency Q0-Q4, Q5 Outputs	5	27.5	35	50	66.7	MHz
f _{Q/2}	Operating frequency Q/2 Output	2.5	13.75	17.5	25	33.3	MHz

NOTES:

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- Note 8 in "General AC Specification Notes" and Figure 5 describes this specification and its actual limits depending on the feedback connection.
- Maximum operating frequency is guaranteed with the part in a phase locked condition and all outputs loaded with 50pF.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

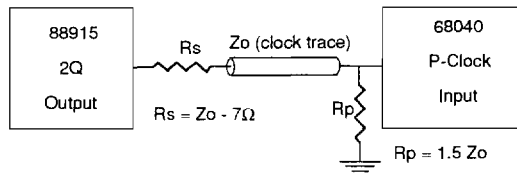
Symbol	Parameter	Condition ⁽¹⁾	Min.	Max.	Unit
tRISE/FALL All Outputs	Rise/Fall Time (between 0.2 V _{CC} and 0.8 V _{CC})	C _L = 50pF R _L = 500Ω	1.0 ⁽²⁾	2.5	ns
tRISE/FALL 2Q Output ⁽³⁾	Rise/Fall Time (between 0.8V and 2.0 V)	C _L = 20pF & termination ⁽⁷⁾	0.5 ⁽²⁾	1.6	ns
tPULSE WIDTH Q, Q̄, Q/2 Outputs ⁽³⁾	Output Pulse Width Q0-Q4, Q̄5, Q/2 @ V _{CC} /2	C _L = 50pF	0.5t _{CYCLE} -0.5 ⁽⁵⁾	0.5t _{CYCLE} +0.5 ⁽⁵⁾	ns
tPULSE WIDTH 2Q Output ⁽³⁾	Output Pulse Width 2Q Output @ V _{CC} /2	C _L = 50pF	0.5t _{CYCLE} -1.0 ⁽⁵⁾	0.5t _{CYCLE} +1.0 ⁽⁵⁾	ns
tPULSE WIDTH 2Q Output ⁽³⁾	Output Pulse Width 2Q @ 1.5V	Termination as in note 7	0.5t _{CYCLE} -0.5 ⁽⁵⁾	0.5t _{CYCLE} +0.5 ⁽⁵⁾	ns
tPD SYNC-FEEDBACK ⁽³⁾	SYNC input to FEEDBACK delay (measured at SYNC0 or 1 and FEEDBACK input pins)	With 1MΩ from RC1 to Analog V _{CC} ⁽⁹⁾	-1.05	-0.50	ns
		With 1MΩ from RC1 to Analog GND ⁽⁹⁾	1.25	3.25	ns
tSKEW _r (rising) ^(3,4)	Output to Output Skew between outputs 2Q, Q0-Q4, Q/2 (rising edges only)	C _L = 50pF	—	500	ps
tSKEW _f (falling) ^(3,4)	Output to Output Skew between outputs 2Q, Q0-Q4, (falling edges only)		—	500	ps
tSKEW _{all} ^(3,4)	Output to Output Skew 2Q, Q/2, Q0-Q4 rising, Q̄5 falling		—	500	ps
t _{LOCK} ⁽⁶⁾	Time required to acquire Phase-Lock from time SYNC input signal is received		t ⁽²⁾	10	ms
t _{RST} Reset - Q	Propagation Delay, RST (High-to-Low) to any Output (High-to-Low)		1.5 ⁽²⁾	8.0	ns
t _{REC} ⁽¹⁰⁾	Reset Recovery Time Rising RST edge to falling SYNC edge		9.0	—	ns
t _w ⁽¹⁰⁾	Minimum Pulse Width RST input LOW		5.0	—	ns

GENERAL AC SPECIFICATION NOTES:

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- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested.
- These specifications are guaranteed but not production tested.
- Under equally loaded conditions, C_L = 50pF (±2pF), and at a fixed temperature and voltage.
- t_{CYCLE} = 1/frequency at which each output (Q, Q̄, Q/2 or 2Q) is expected to run.
- With V_{CC} fully powered-on and an output properly connected to the FEEDBACK pin, t_{LOCK} Max. is with C₁ = 0.1μF, t_{LOCK} Min. is with C₁ = 0.01μF. (Where C₁ is loop filter capacitor shown in Figure 4).

7. These two specs ($t_{RISE/FALL}$ and $t_{PULSE\ WIDTH\ 2Q\ output}$) guarantee that the FCT88915 meets the 68040 P-Clock input specification. For these two specs to be guaranteed by IDT, the termination scheme shown in the figure below must be used.



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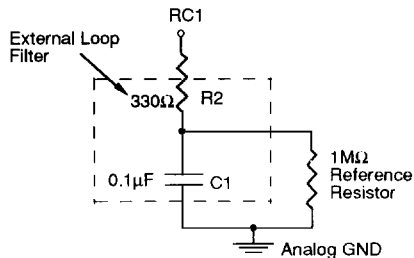
Figure 1. MC68040 P-Clock Input Termination Scheme

8. The wiring diagrams and written explanations in Figure 5 demonstrate the input and output frequency relationships for various possible feedback configurations. The allowable SYNC input range to stay in the phase-locked condition is also indicated. There are two allowable SYNC frequency ranges, depending on whether $FREQ_SEL$ is high or low. Also it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the Q outputs. The table below summarizes the allowable SYNC frequency range for each possible configuration.

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHz)	Corresponding VCO Frequency Range	Phase Relationship of the Q Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2Q fMAX Spec)/4	20 to (2Q fMAX Spec)	0°
HIGH	Any Q (Q0-Q4)	10 to (2Q fMAX Spec)/2	20 to (2Q fMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2Q fMAX Spec)/2	20 to (2Q fMAX Spec)	180°
HIGH	2Q	20 to (2Q fMAX Spec)	20 to (2Q fMAX Spec)	0°
LOW	Q/2	2.5 to (2Q fMAX Spec)/8	20 to (2Q fMAX Spec)	0°
LOW	Any Q (Q0-Q4)	5 to (2Q fMAX Spec)/4	20 to (2Q fMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2Q fMAX Spec)/4	20 to (2Q fMAX Spec)	180°
LOW	2Q	10 to (2Q fMAX Spec)/2	20 to (2Q fMAX Spec)	0°

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9. A 1MΩ resistor tied to either Analog Vcc or Analog GND as shown below may be included to adjust SYNC to FEEDBACK delay. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature and voltage. Measurements were made with a 10MHz SYNC input and the Q/2 output fed back. The phase measurements were made at 1.5V. The Q/2 output was terminated at the FEEDBACK input with 100Ω to V_{cc} and 100Ω to ground.

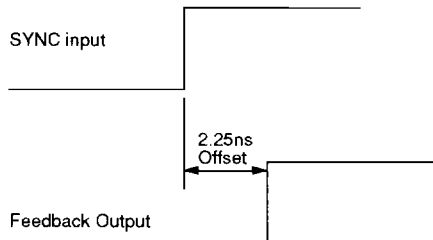


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Figure 2a. Resistor To Analog GND Connection

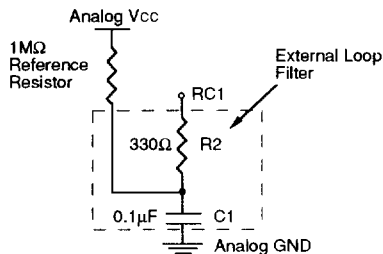
With the resistor tied to Analog GND, the t_{PD} specification measured at the input pins is:

$$t_{PD} = 2.25\text{ns} \pm 1.0\text{ns} (1\text{M}\Omega)$$



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Figure 2b. SYNC To Feedback Offset Resulting From Connection Shown In Fig 2a

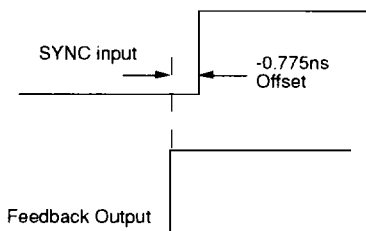


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Figure 3a. Resistor To Analog Vcc Connection

With the resistor tied to Analog Vcc, the t_{PD} specification measured at the input pins is:

$$t_{PD} = -0.775\text{ns} \pm 0.275\text{ns} (1\text{M}\Omega)$$



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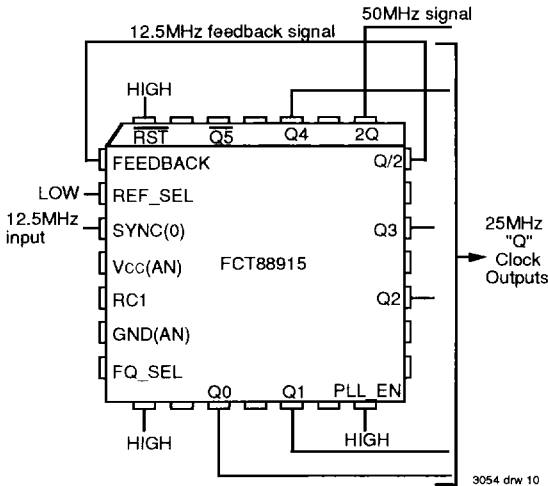
Figure 3b. SYNC To Feedback Offset Resulting From Connection Shown In Fig 3a

10. These specs are valid only when PLL_EN is LOW (in test mode).

The frequency relationship shown here is applicable to all Q outputs (Q0, Q1, Q2, Q3 and Q4).

1:2 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The Q outputs (Q0-Q4, Q5) will always run at 2X the Q/2 frequency, and the 2Q output will run at 4X the Q/2 frequency.

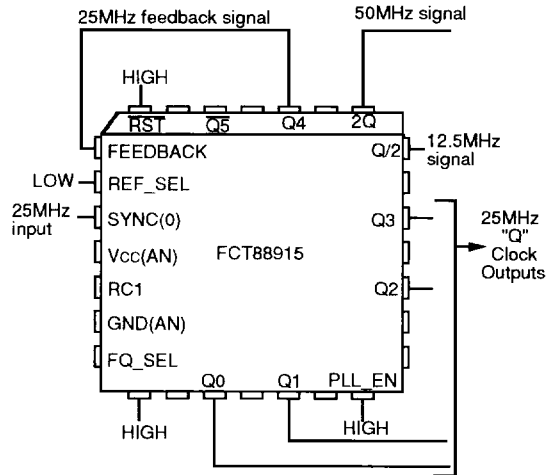


Allowable Input Frequency Range:
 5MHz to (f2Q MAX Spec)/4 (for FREQ_SEL HIGH)
 2.5MHz to (f2Q MAX Spec) /8 (for FREQ_SEL LOW)

Figure 5a. Wiring Diagram and Frequency Relationships With Q/2 Output Feedback

1:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the Q frequency, and the 2Q output will run at 2X the Q frequency.

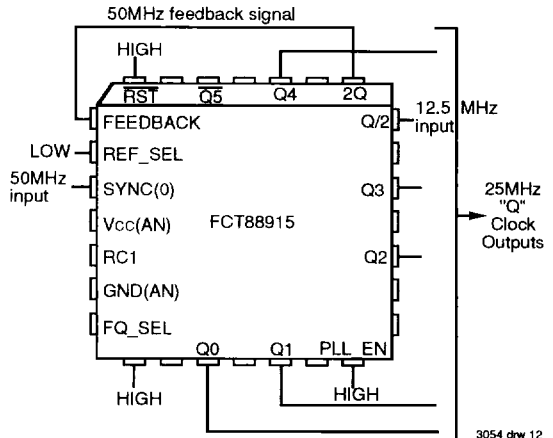


Allowable Input Frequency Range:
 10MHz to (f2Q MAX Spec) /2 (for FREQ_SEL HIGH)
 5MHz to (f2Q MAX Spec)/4 (for FREQ_SEL LOW)

Figure 5b. Wiring Diagram and Frequency Relationships With Q4 Output Feedback

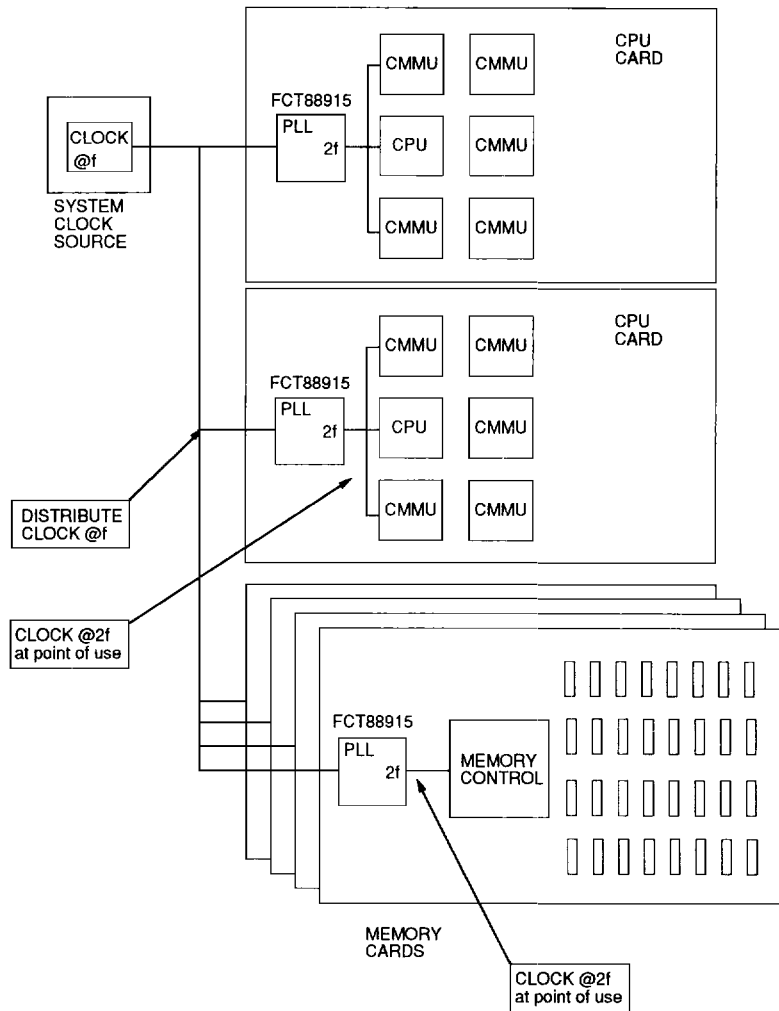
2:1 INPUT TO "Q" OUTPUT FREQUENCY RELATIONSHIP

In this application, the 2Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2Q and SYNC, thus the 2Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/4 the 2Q frequency, and the Q output will run at 1/2 the 2Q frequency.



Allowable Input Frequency Range:
 20MHz to (f2Q MAX Spec) (for FREQ_SEL HIGH)
 10MHz to (f2Q MAX Spec)/2 (for FREQ_SEL LOW)

Figure 5c. Wiring Diagram and Frequency Relationships With 2Q Output Feedback



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Figure 6. Multiprocessing Application Using the FCT88915 for Frequency Multiplication and Low Board-to-Board skew

FCT88915 System Level Testing

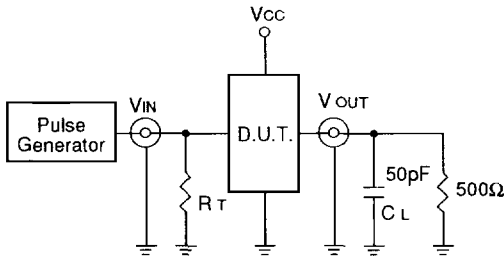
When the PLL_EN pin is LOW, the PLL is bypassed and the FCT88915 is in low frequency "test mode". In test mode (with FREQ_SEL HIGH), the 2Q output is inverted from the selected SYNC input, and the Q outputs are divide-by-2 (negative edge triggered) of the SYNC input, and the Q/2 output is divide-by-4 (negative edge triggered). With FREQ_SEL LOW the 2Q output is divide-by-2 of the SYNC, the Q outputs divide-by-4, and the Q/2 output divide-by-8. These relationships can be seen in the block diagram. A

recommended test configuration would be to use SYNC0 or SYNC1 as the test clock input, and tie PLL_EN and REF_SEL together and connect them to the test select logic.

This functionality is needed since most board-level testers run at 1 MHz or below, and the FCT88915 cannot lock onto that low of an input frequency. In the test mode described above, any test frequency can be used.

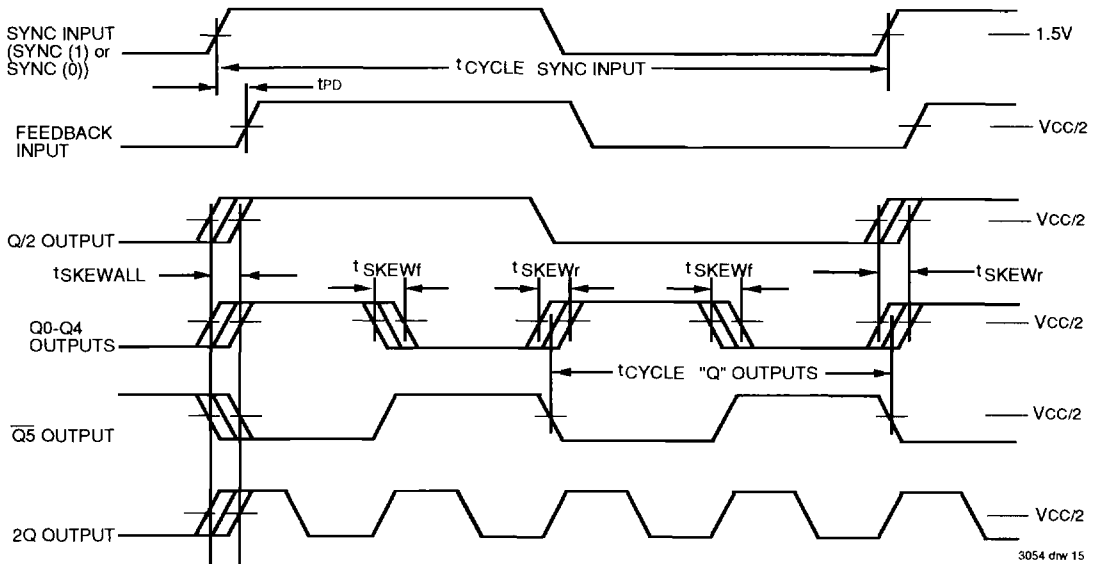
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR ALL OUTPUTS



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PROPAGATION DELAY, OUTPUT SKEW



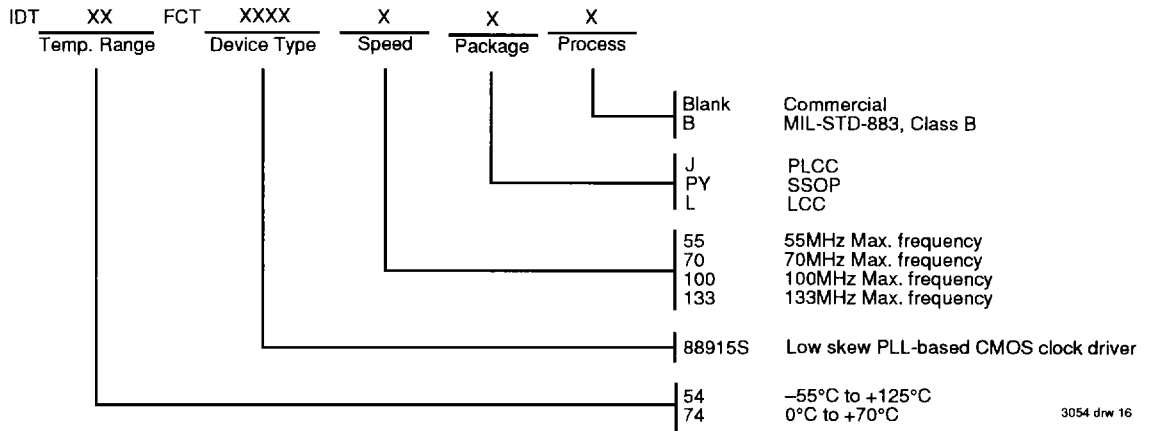
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(These waveforms represent the configuration shown in Figure 6a)

NOTES:

1. The FCT88915 aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the Vcc/2 crossing point of the appropriate output edges. All skews are specified as "windows", not as \pm deviation around a center point.
3. If a Q output is connected to the FEEDBACK input (this situation is not shown), the Q output frequency would match the SYNC input frequency, the 2Q output would run at twice the SYNC frequency and the Q/2 output would run at half the SYNC frequency.

ORDERING INFORMATION



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