

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

MM74HCT08

Quad 2-Input AND Gate

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH} , t_{PHL} = 12ns (typ.)
- Low power: 10 μ W at DC
- High fan-out, 10 LS-TTL loads

General Description


The MM74HCT08 is a logic function fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic and pinout compatible with standard 74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Ordering Information

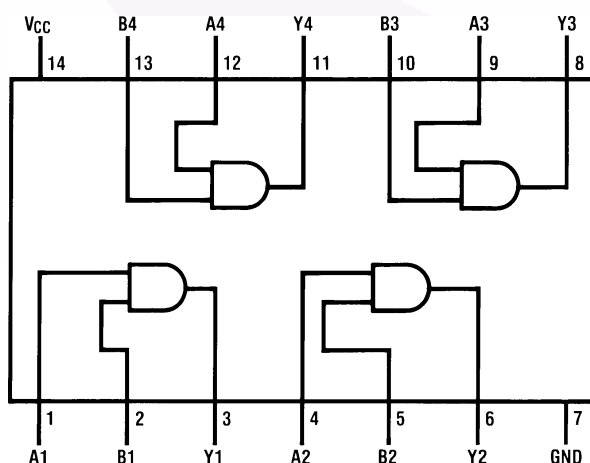
Order Number	Package Number	Package Description
MM74HCT08M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HCT08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HCT08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HCT08N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

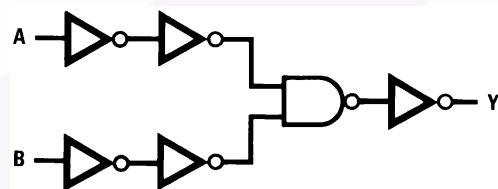
 All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Logic Diagram



Absolute Maximum Ratings⁽¹⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	-0.5 to +7.0V
V_{IN}	DC Input Voltage	-1.5 to $V_{CC}+1.5V$
V_{OUT}	DC Output Voltage	-0.5 to $V_{CC}+0.5V$
I_{IK}, I_{OK}	Clamp Diode Current	$\pm 20mA$
I_{OUT}	DC Output Current, per pin	$\pm 25mA$
I_{CC}	DC V_{CC} or GND Current, per pin	$\pm 50mA$
T_{STG}	Storage Temperature Range	-65°C to +150°C
P_D	Power Dissipation Note 2	600mW
	S.O. Package only	500mW
T_L	Lead Temperature (Soldering 10 seconds)	260°C

Notes:

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating — plastic "N" package: -12mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-40	+85	°C
t_r, t_f	Input Rise or Fall Times		500	ns

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25^\circ\text{C}$		$T_A = -40^\circ\text{C}$	$T_A = -55^\circ\text{C}$	Units
			Typ.	Guaranteed Limits		to 85°C	
V_{IH}	Minimum HIGH Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum LOW Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} , $ I_{OUT} = 20\mu\text{A}$	V_{CC}	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$	V
		$V_{IN} = V_{IH}$ or V_{IL} , $ I_{OUT} = 4.0\text{mA}$, $V_{CC} = 4.5\text{V}$	4.2	3.98	3.84	3.7	
		$V_{IN} = V_{IH}$ or V_{IL} , $ I_{OUT} = 4.8\text{mA}$, $V_{CC} = 5.5\text{V}$	5.2	4.98	4.84	4.7	
V_{OL}	Maximum LOW Level Voltage	$V_{IN} = V_{IH}$, $ I_{OUT} = 20\mu\text{A}$	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$, $ I_{OUT} = 4.0\text{mA}$, $V_{CC} = 4.5\text{V}$	0.2	0.26	0.33	0.4	
		$V_{IN} = V_{IH}$, $ I_{OUT} = 4.8\text{mA}$, $V_{CC} = 5.5\text{V}$	0.2	0.26	0.33	0.4	
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND, V_{IH} or V_{IL}		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0\mu\text{A}$		2.0	20	40	μA
		$V_{IN} = 2.4\text{V}$ or $0.5\text{V}^{(3)}$		1.2	1.4	1.5	mA

Note:3. This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC} = 5.0V$, $t_r = t_f = 6ns$, $C_L = 15pF$, $T_A = 25^\circ C$

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Units
t_{PLH} , t_{PHL}	Maximum Propagation Delay		9	15	ns

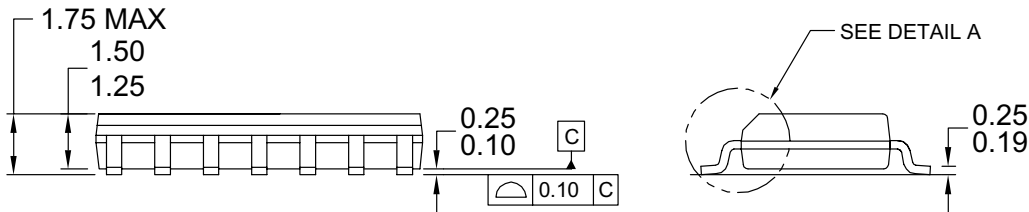
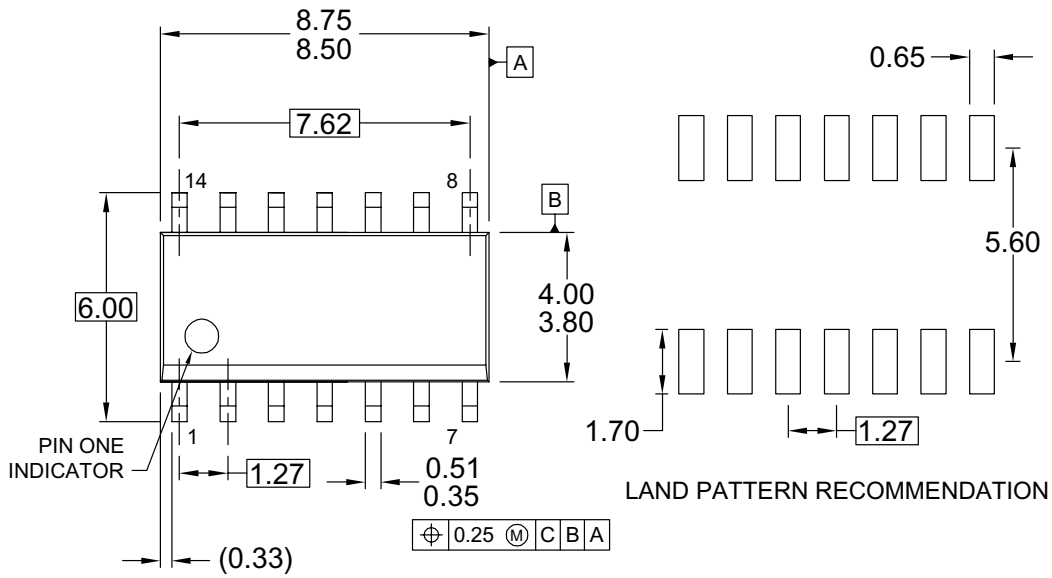
AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6ns$, $C_L = 50pF$

Symbol	Parameter	Conditions	$T_A = 25^\circ C$		$T_A = -40^\circ C$ to $85^\circ C$	$T_A = -55^\circ C$ to $125^\circ C$	Units
			Typ.	Guaranteed Limits			
t_{PLH} , t_{PHL}	Maximum Propagation Delay		11	18	23	27	ns
t_{THL} , t_{TLH}	Maximum Output Rise and Fall Time		7	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(4)	38				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

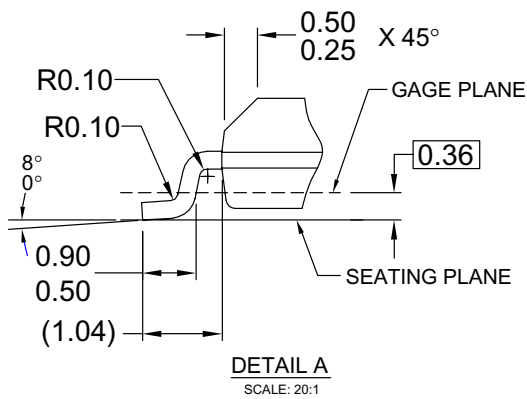
Note:

4. C_{PD} determines the no load dynamic power consumption. $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

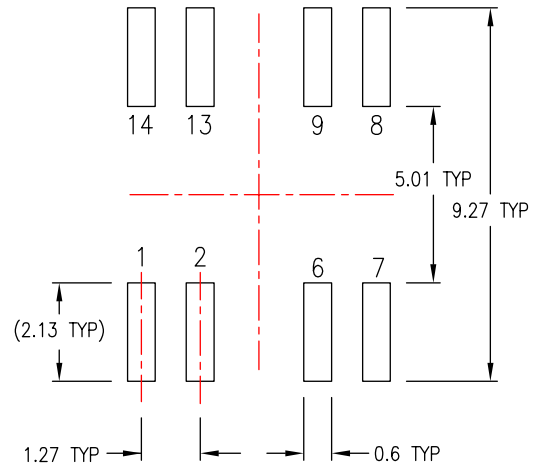
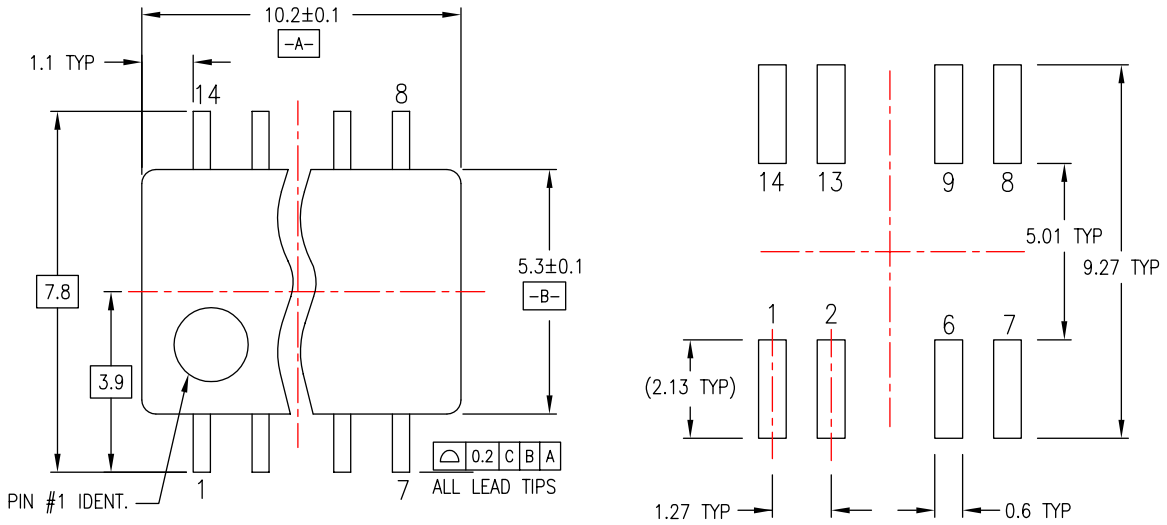
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

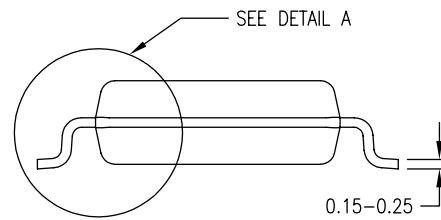
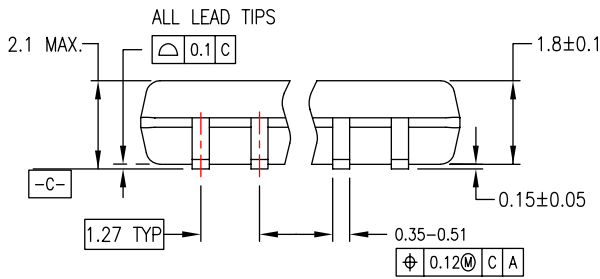
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Physical Dimensions (Continued)



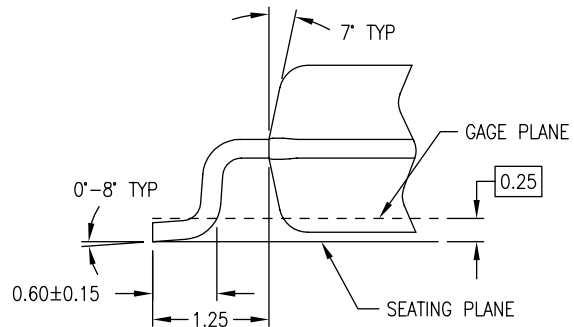
LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.



DETAIL A

M14DREVC

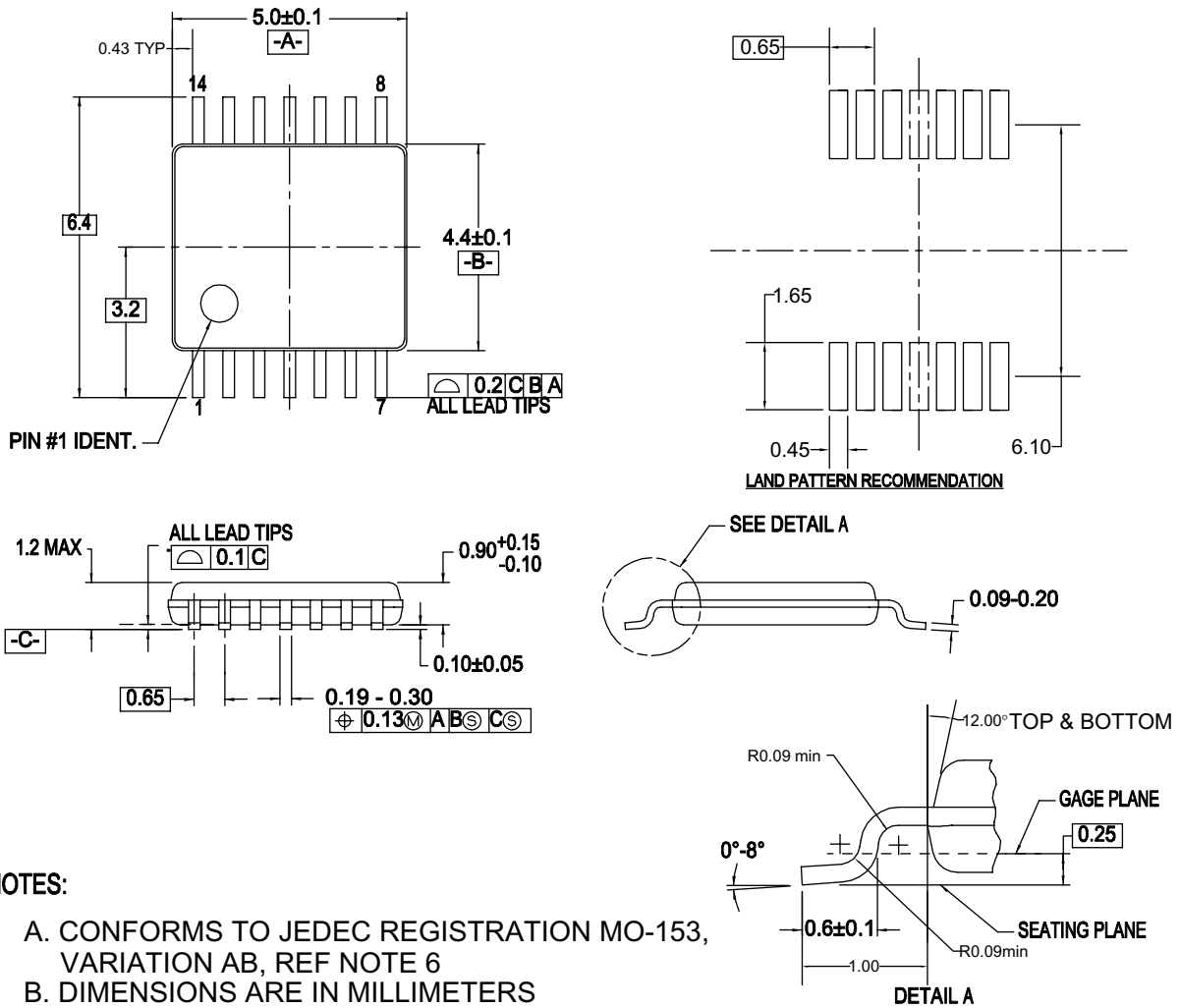
Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

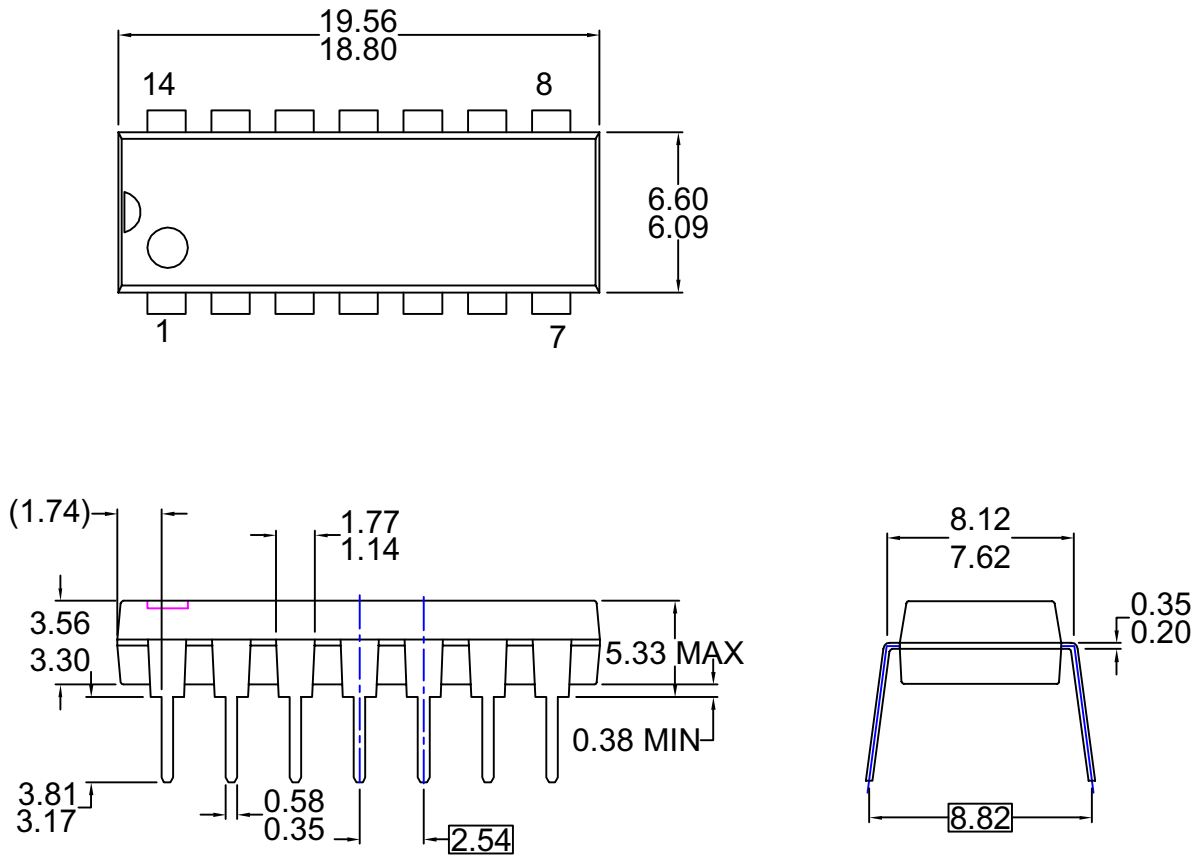
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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Physical Dimensions (Continued)



- NOTES: UNLESS OTHERWISE SPECIFIED**
THIS PACKAGE CONFORMS TO
 A) JEDEC MS-001 VARIATION BA
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
 MOLD FLASH, AND TIE BAR EXTRUSIONS.
 D) DIMENSIONS AND TOLERANCES PER
 ASME Y14.5-1994
 E) DRAWING FILE NAME: MKT-N14AREV7

Figure 4. 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

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Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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