![Texas Instruments]

TL072-EP, TL074-EP
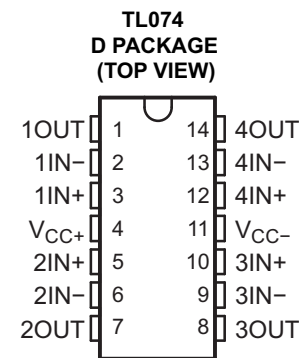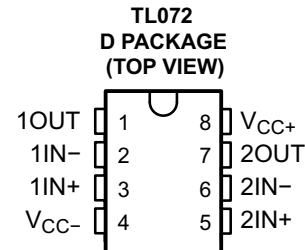
LOW-NOISE JFET-INPUT OPERATIONAL AMPLIFIER

Check for Samples: **TL072-EP**, **TL074-EP**

FEATURES

- **Low Power Consumption**
- **Wide Common-Mode and Differential Voltage Ranges**
- **Low Input Bias and Offset Currents**
- **Output Short-Circuit Protection**
- **Low Total Harmonic Distortion: 0.003% Typ**
- **Low Noise**
  V_n = 18 nV/$\sqrt{\text{Hz}}$ **Typ at f = 1 kHz**
- **High Input Impedance: JFET Input Stage**
- **Internal Frequency Compensation**
- **Latch-Up-Free Operation**
- **High Slew Rate: 13 V/µs Typ**
- **Common-Mode Input Voltage Range Includes V_{CC+}**

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- **Controlled Baseline**
- **One Assembly and Test Site**
- **One Fabrication Site**
- **Available in Extended (–40°C to 125°C) or Military (–55°C to 125°C) Temperature Range**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**

TL072
D PACKAGE
(TOP VIEW)

1OUT	1	8	V_{CC+}
1IN−	2	7	2OUT
1IN+	3	6	2IN−
V_{CC-}	4	5	2IN+

TL074
D PACKAGE
(TOP VIEW)

1OUT	1	14	4OUT
1IN−	2	13	4IN−
1IN+	3	12	4IN+
V_{CC+}	4	11	V_{CC-}
2IN+	5	10	3IN+
2IN−	6	9	3IN−
2OUT	7	8	3OUT

DESCRIPTION/ORDERING INFORMATION

The JFET-input operational amplifiers in the TL07x is similar to the TL08x series, with low input bias and offset currents and fast slew rate. The low harmonic distortion and low noise make the TL07x ideally suited for high-fidelity and audio preamplifier applications. Each amplifier features JFET inputs (for high input impedance) coupled with bipolar output stages integrated on a single monolithic chip.

The TL07x is characterized for operation over the extended temperature range of –40°C to 125°C or military temperature range of –55°C to 125°C.

ORDERING INFORMATION[1]

T_A	V_{IO}maX AT 25°C	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 125°C	6 mV	SOIC – D	Reel of 2500	TL072QDREP	TL072Q	V62/12604-01XE
				TL074QDREP	TL074Q	V62/11621-01XE
–55°C to 125°C	6 mV	SOIC – D	Reel of 2500	TL074MDREP	TL074M	V62/11621-02XE
			Tube of 75	TL074MDEP	TL074M	V62/11621-02XE-T

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
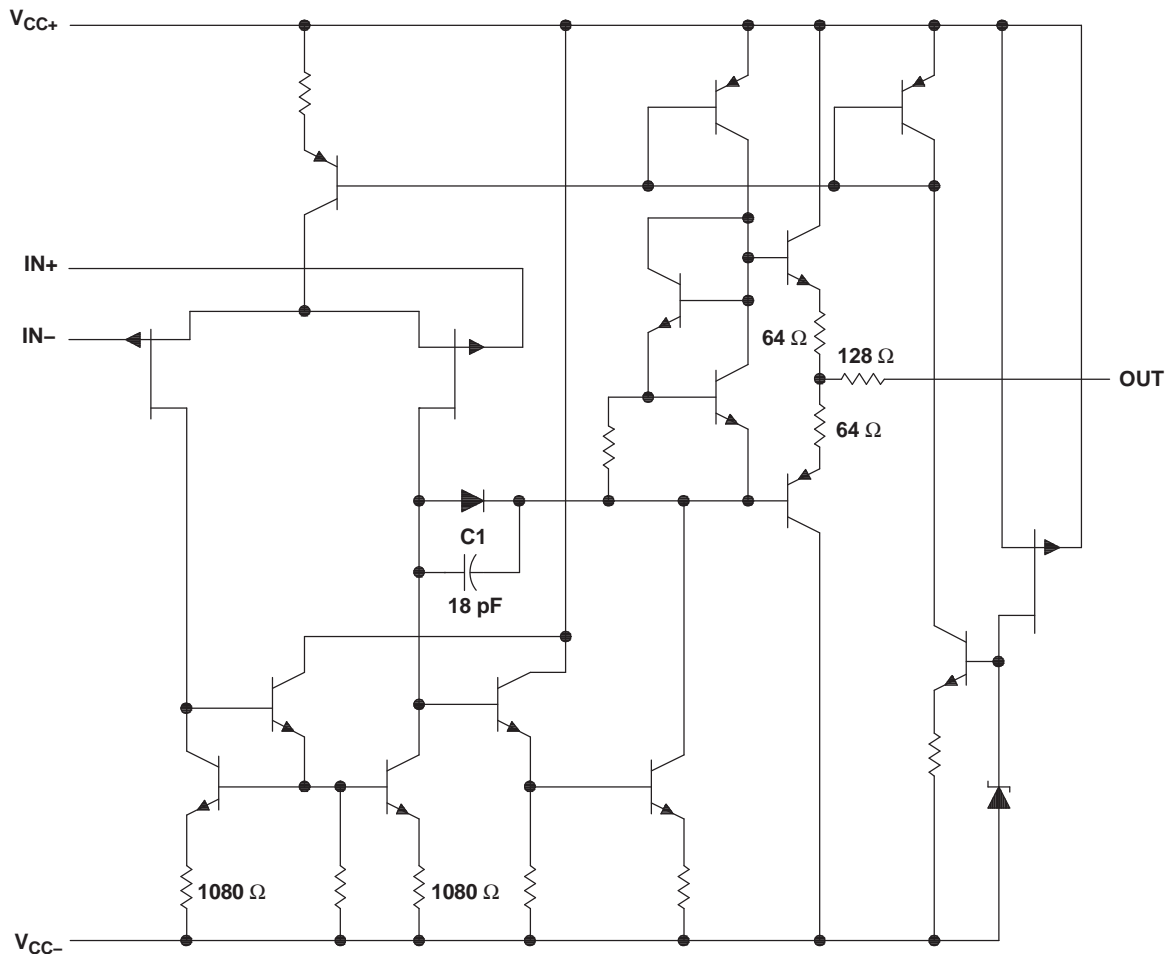
⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TL072 and TL074 SYMBOL (EACH AMPLIFIER)
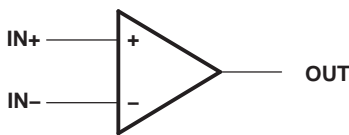
SCHEMATIC (EACH AMPLIFIER)

All component values shown are nominal.

COMPONENT COUNT[1]		
COMPONENT TYPE	TL072	TL074
Resistors	22	44
Transistors	28	56
JFET	4	6
Diodes	2	4
Capacitors	2	4
epi-FET	2	4

(1)   Includes bias and trim circuitry

Product Folder Links: *TL072-EP TL074-EP*

TEXAS INSTRUMENTS

TL072-EP, TL074-EP

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage[2]			18	V
V_{CC-}				18	
V_{ID}	Differential input voltage[3]			±30	V
V_I	Input voltage[2] [4]			±15	V
	Duration of output short circuit[5]		Unlimited		
θ_{JA}	Thermal resistance, junction-to-ambient[6] [7]	TL072		97.5	°C/W
		TL074		86	
θ_{JC}	Thermal resistance, junction-to-case[7]	TL072		38.3	°C/W
		TL074		51.5	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) Differential voltages are at IN+, with respect to IN−.
(4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
(5) The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(6) Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

Product Folder Links: *TL072-EP TL074-EP*

ELECTRICAL CHARACTERISTICS

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

	PARAMETER	TEST CONDITIONS[1]	T_A [2]	TL072 MIN	TL072 TYP	TL072 MAX	TL074 MIN	TL074 TYP	TL074 MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 50 Ω	25°C		3	6		3	6	mV
			Full range			8			8	
α_{VIO}	Temperature coefficient of input offset voltage	V_O = 0, R_S = 50 Ω	Full range		18			18		µV/°C
I_{IO}	Input offset current	V_O = 0	25°C		5	100		5	100	pA
			125°C			2			2	nA
I_{IB}	Input bias current	V_O = 0	25°C		65	200		65	200	pA
			125°C			20			20	nA
V_{ICR}	Common-mode input voltage range		25°C	±11	−12 to 15		±11	−12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L = 10 kΩ	25°C	±12	±13.5		±12	±13.5		V
		R_L ≥ 10 kΩ	Full range	±12			±12			
		R_L ≥ 2 kΩ		±10			±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V, R_L ≥ 2 kΩ	25°C	35	200		35	200		V/mV
			Full range	15			15			
B_1	Unity-gain bandwidth		25°C		3			3		MHz
r_i	Input resistance		25°C		10^{12}			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$min, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V, V_O = 0, R_S = 50 Ω	25°C	80	86		80	86		dB
I_{CC}	Supply current (each amplifier)	V_O = 0, No load	25°C		1.4	2.5		1.4	2.5	mA
V_{O1}/V_{O2}	Crosstalk attenuation	A_{VD} = 100	25°C		120			120		dB

(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 3. Pulse techniques must be used that will maintain the junction temperature as close to the ambient temperature as possible.

(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = −40°C to 125°C for TL07xQ and T_A = -55°C to 125°C for TL07xM.

OPERATING CHARACTERISTICS

$V_{CC\pm}$ = ±15 V, T_A = 25°C

|	PARAMETER	TEST CONDITIONS		TL072 MIN	TL072 TYP	TL072 MAX	TL074 MIN	TL074 TYP	TL074 MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1	8	13		8	13		V/µs
t_r	Rise-time overshoot factor	V_I = 20 V, C_L = 100 pF,	R_L = 2 kΩ, See Figure 1		0.1			0.1		µs
					20			20		%
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18			18		nV/√Hz
			f = 10 Hz to 10 kHz		4			4		µV
I_n	Equivalent input noise current	R_S = 20 Ω,	f = 1 kHz		0.01			0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V, R_L ≥ 2 kΩ, f = 1 kHz,	A_{VD} = 1, RS ≤ 1 kΩ,		0.003			0.003		%

PARAMETER MEASUREMENT INFORMATION
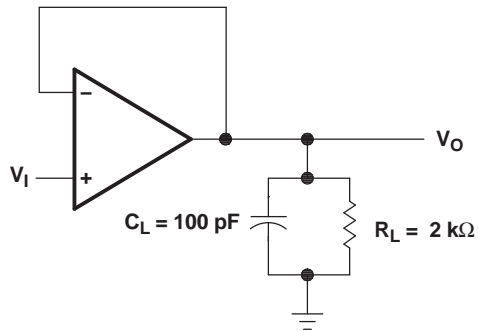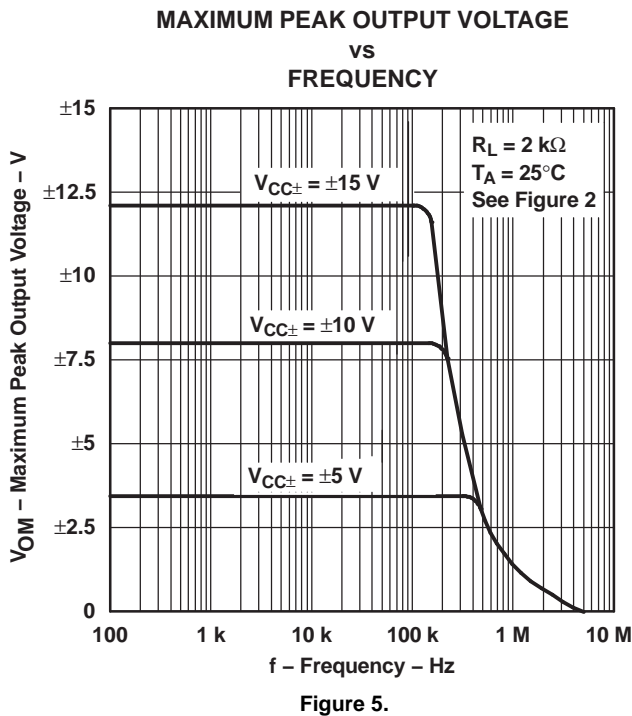

Figure 1. Unity-Gain Amplifier
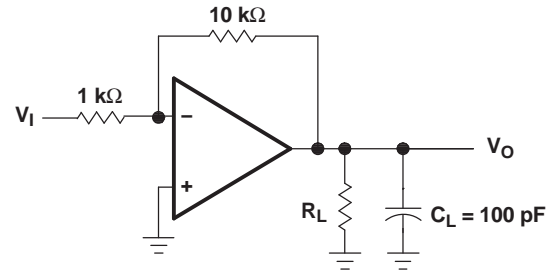
Figure 2. Gain-of-10 Inverting Amplifier

Product Folder Links: *TL072-EP TL074-EP*

TL072-EP, TL074-EP

TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

INPUT BIAS CURRENT
vs
FREE-AIR TEMPERATURE

$V_{CC\pm} = \pm15$ V

Figure 3.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

$V_{CC\pm} = \pm15$ V
$V_{CC\pm} = \pm10$ V
$V_{CC\pm} = \pm5$ V

$R_L = 10$ kΩ
$T_A = 25°C$
See Figure 2

Figure 4.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

$R_L = 2$ kΩ
$T_A = 25°C$
See Figure 2

$V_{CC\pm} = \pm15$ V
$V_{CC\pm} = \pm10$ V
$V_{CC\pm} = \pm5$ V

Figure 5.

MAXIMUM PEAK OUTPUT VOLTAGE
vs
FREQUENCY

$V_{CC\pm} = \pm15$ V
$R_L = 2$ kΩ
See Figure 2

$T_A = 25°C$
$T_A = -55°C$
$T_A = 125°C$

Figure 6.

Product Folder Links: *TL072-EP TL074-EP*

TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
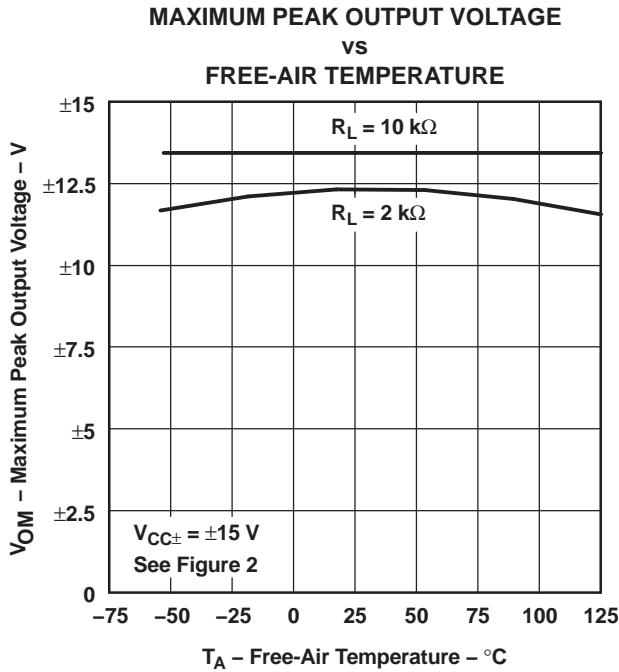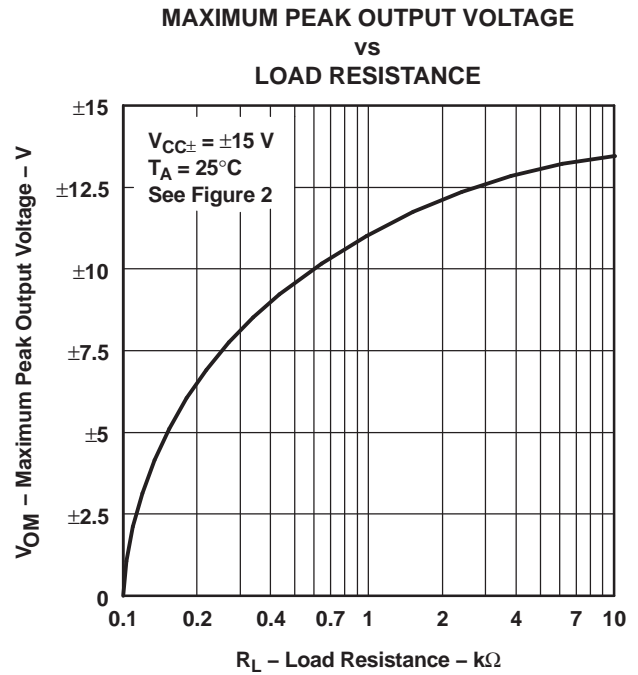
**MAXIMUM PEAK OUTPUT VOLTAGE
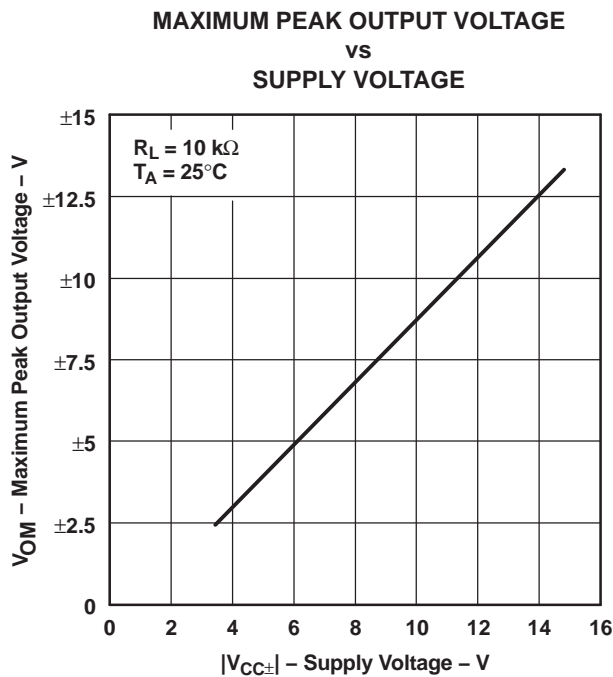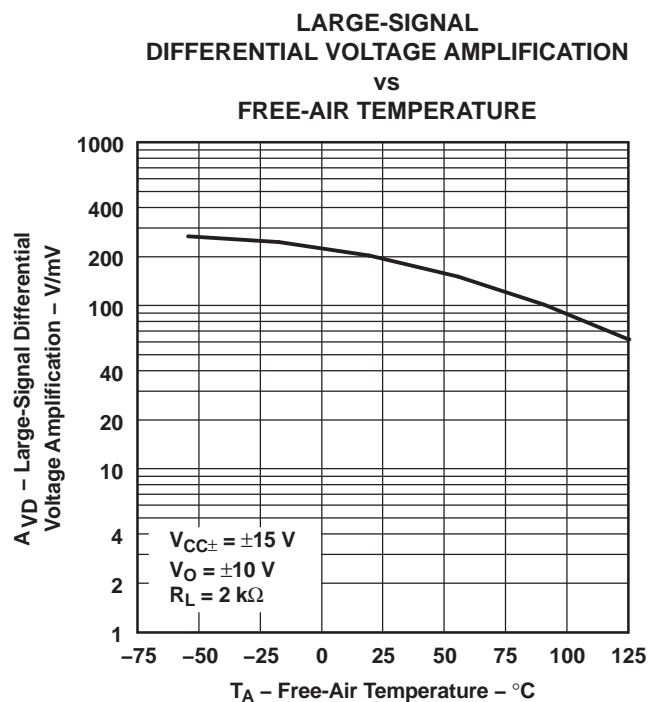vs
FREE-AIR TEMPERATURE**

Figure 7.

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
LOAD RESISTANCE**

Figure 8.

**MAXIMUM PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE**

Figure 9.

**LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE**

Figure 10.

Product Folder Links: *TL072-EP TL074-EP*

TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
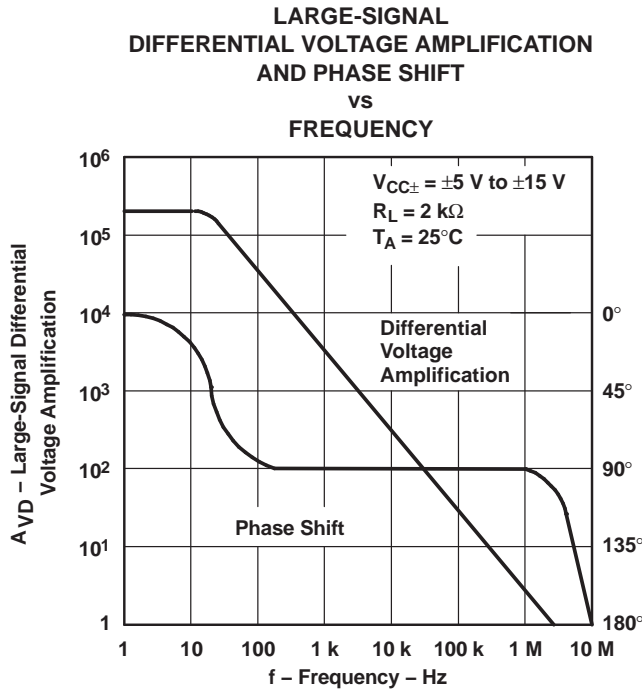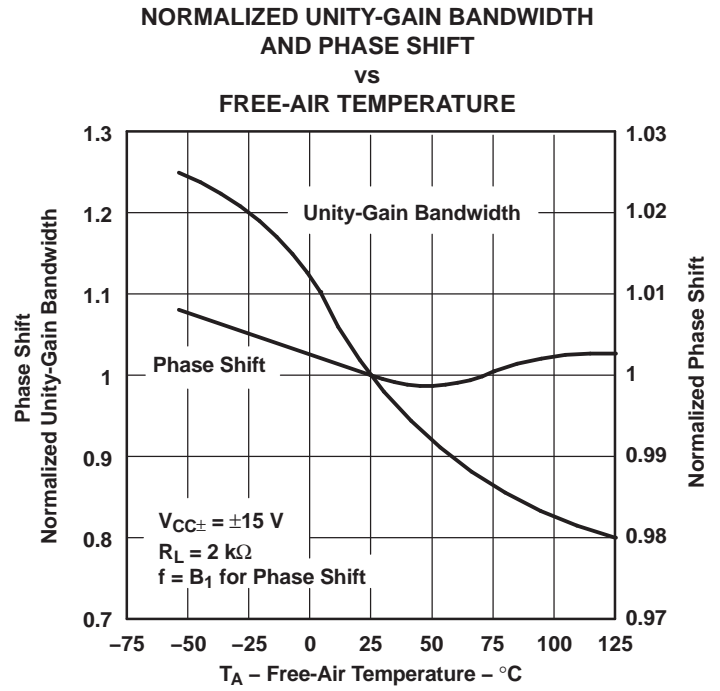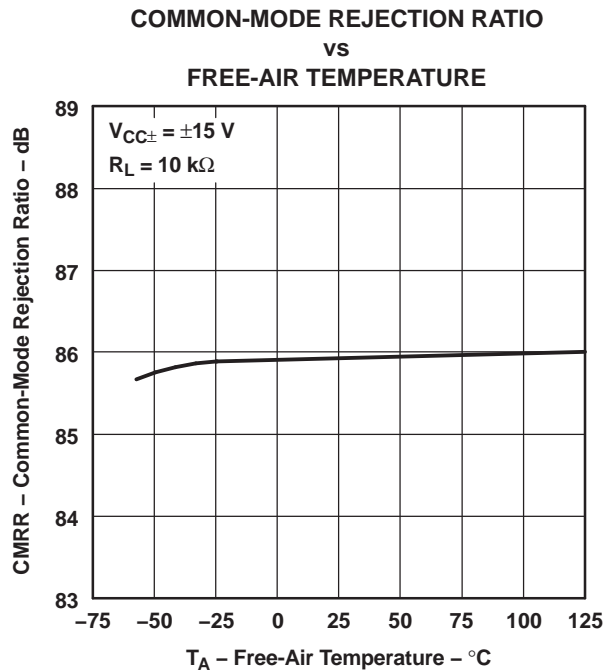
LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
vs
FREQUENCY

$V_{CC\pm}$ = ±5 V to ±15 V
R_L = 2 kΩ
T_A = 25°C

Differential Voltage Amplification

Phase Shift

Figure 11.

NORMALIZED UNITY-GAIN BANDWIDTH
AND PHASE SHIFT
vs
FREE-AIR TEMPERATURE

Unity-Gain Bandwidth

Phase Shift

$V_{CC\pm}$ = ±15 V
R_L = 2 kΩ
f = B_1 for Phase Shift

Figure 12.

COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE

$V_{CC\pm}$ = ±15 V
R_L = 10 kΩ

Figure 13.

SUPPLY CURRENT PER AMPLIFIER
vs
SUPPLY VOLTAGE

T_A = 25°C
No Signal
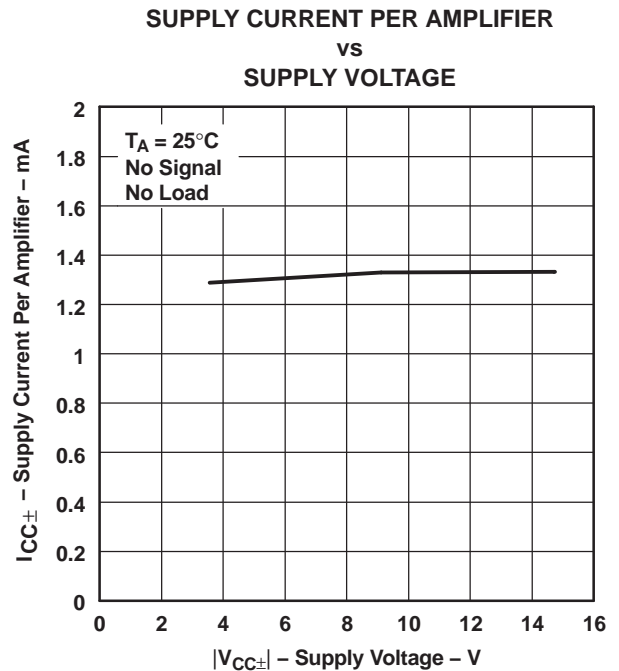No Load

Figure 14.

Product Folder Links: *TL072-EP TL074-EP*

TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
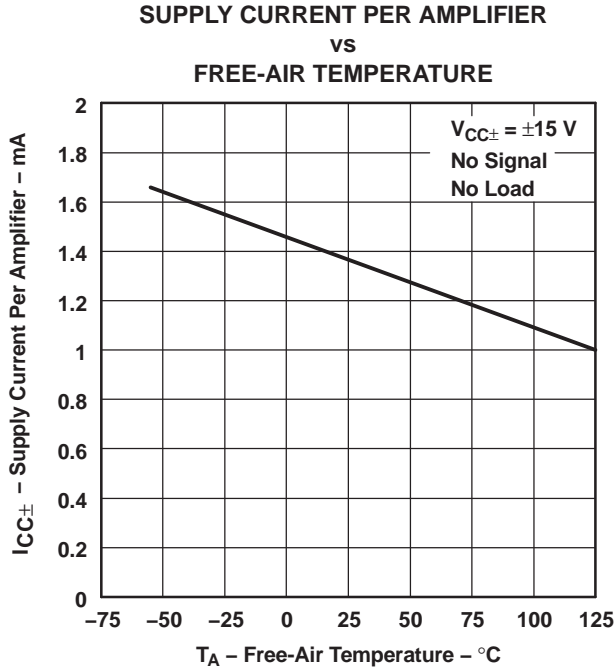
**SUPPLY CURRENT PER AMPLIFIER
vs
FREE-AIR TEMPERATURE**

Figure 15.

**TOTAL POWER DISSIPATION
vs
FREE-AIR TEMPERATURE**

Figure 16.

**NORMALIZED SLEW RATE
vs
FREE-AIR TEMPERATURE**

Figure 17.

**EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY**

Figure 18.

Product Folder Links: *TL072-EP TL074-EP*

TYPICAL CHARACTERISTICS (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
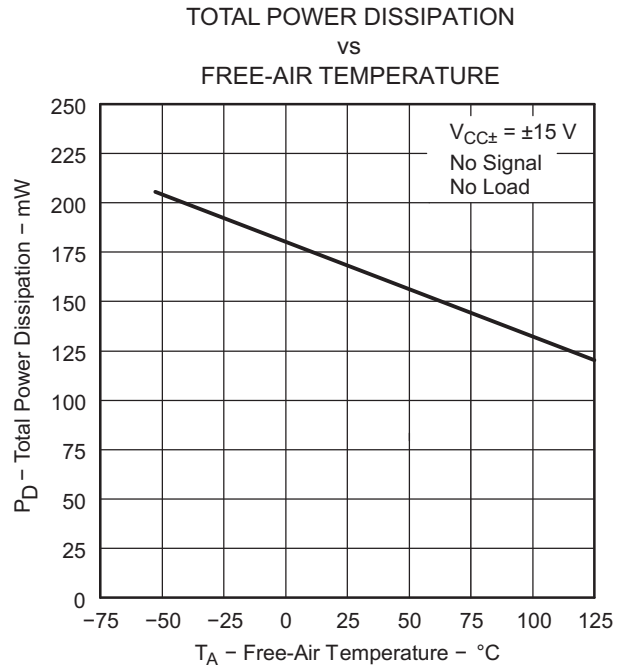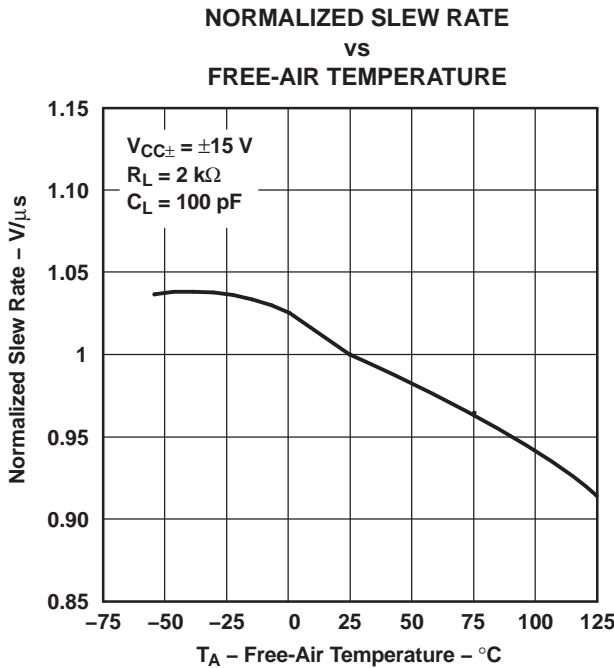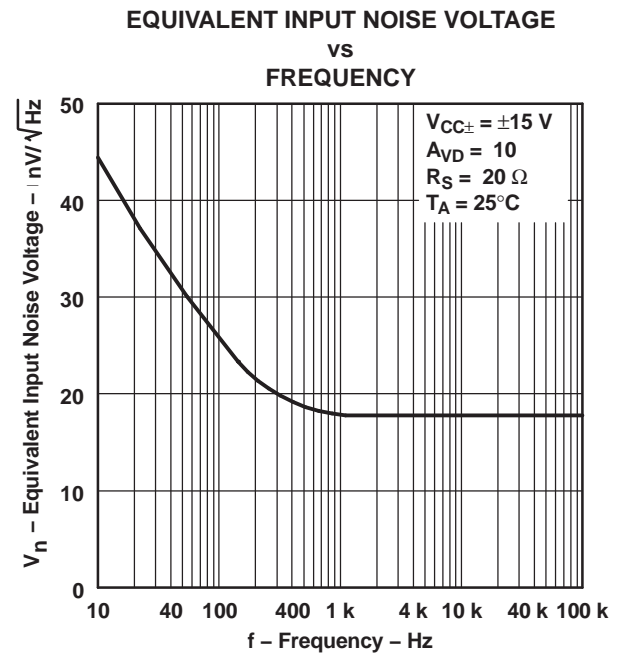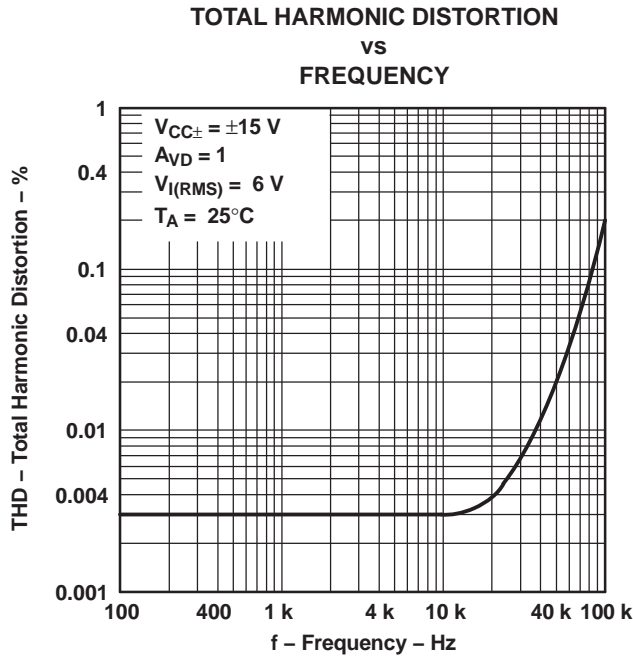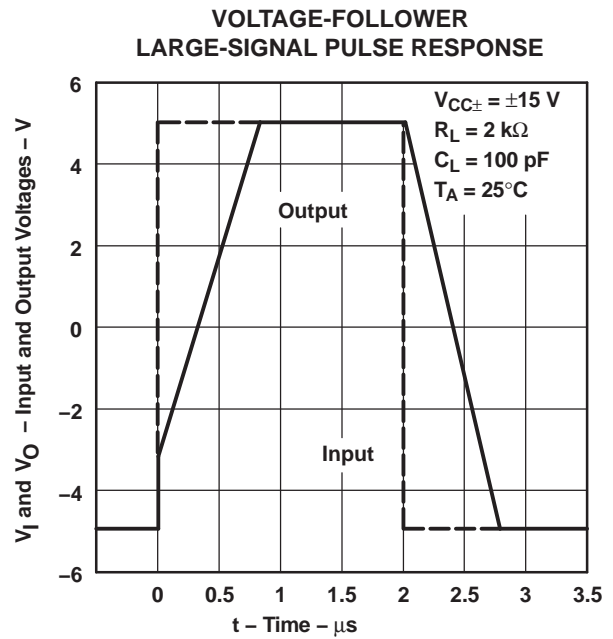
TOTAL HARMONIC DISTORTION vs FREQUENCY

$V_{CC\pm} = \pm15$ V
$A_{VD} = 1$
$V_{I(RMS)} = 6$ V
$T_A = 25°C$

THD – Total Harmonic Distortion – %
f – Frequency – Hz

Figure 19.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

$V_{CC\pm} = \pm15$ V
$R_L = 2$ kΩ
$C_L = 100$ pF
$T_A = 25°C$

Output
Input

V_I and V_O – Input and Output Voltages – V
t – Time – µs

Figure 20.

OUTPUT VOLTAGE vs ELAPSED TIME

Overshoot
90%
10%
t_r

$V_{CC\pm} = \pm15$ V
$R_L = 2$ kΩ
$T_A = 25°C$

V_O – Output Voltage – mV
t – Elapsed Time – µs
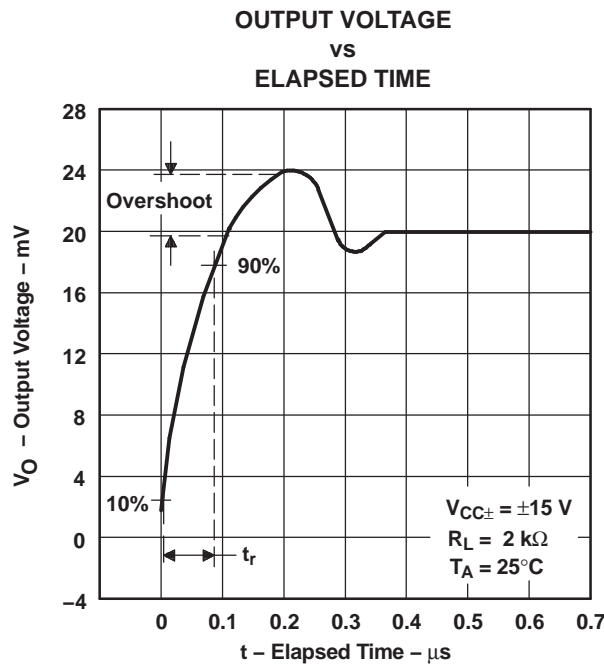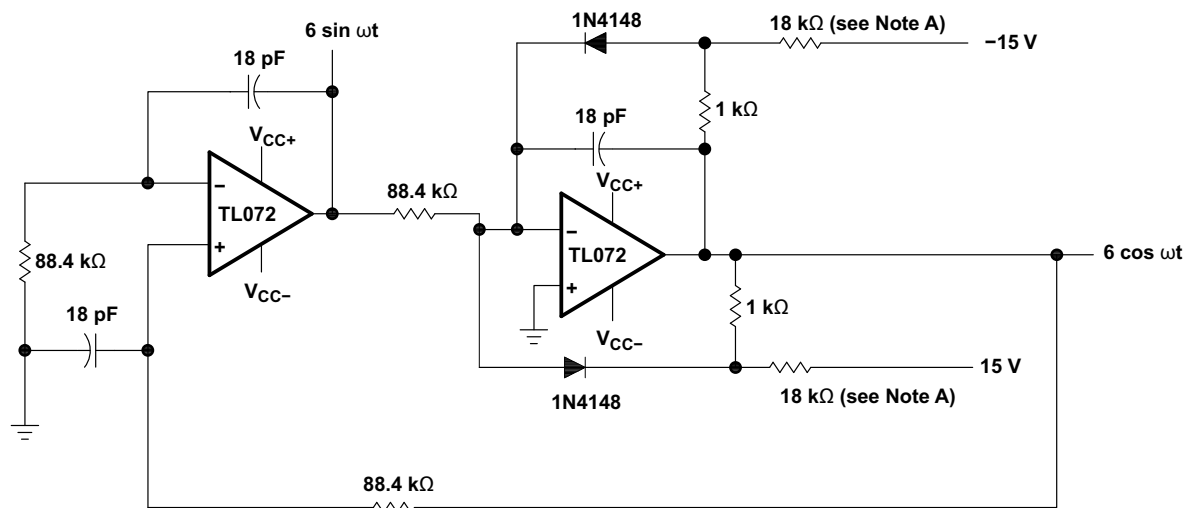
Figure 21.

Product Folder Links: *TL072-EP TL074-EP*

APPLICATION INFORMATION

NOTE A: These resistor values may be adjusted for a symmetrical output.
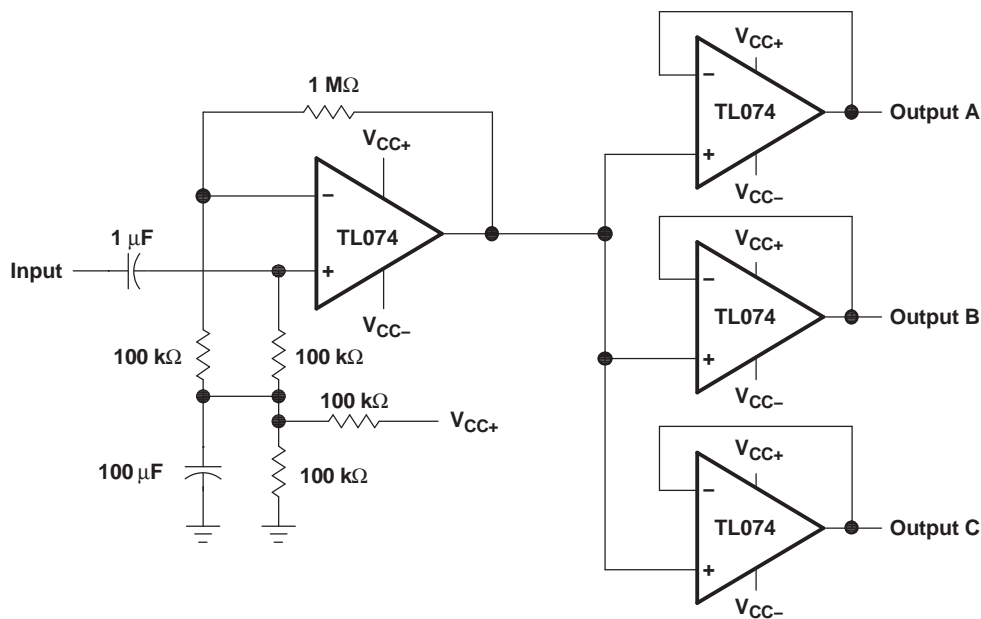
Figure 22. 100-kHz Quadrature Oscillator

Figure 23. Audio-Distribution Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072QDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072Q	Samples
TL074MDEP	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TL074M	Samples
TL074MDREP	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TL074M	Samples
TL074QDREP	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074Q	Samples
V62/11621-01XE	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074Q	Samples
V62/11621-02XE	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TL074M	Samples
V62/11621-02XE-T	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	TL074M	Samples
V62/12604-01XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL072-EP, TL074-EP :

● Catalog : TL072, TL074

● Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

 ● Catalog - TI's standard catalog product

 ● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL072QDREP	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TL074MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074QDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072QDREP	SOIC	D	8	2500	340.5	338.1	20.6
TL074MDREP	SOIC	D	14	2500	340.5	336.1	32.0
TL074QDREP	SOIC	D	14	2500	340.5	336.1	32.0

PACKAGE MATERIALS INFORMATION

TUBE

T - Tube height
L - Tube length
W - Tube width
B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL074MDEP	D	SOIC	14	50	507	8	3940	4.32
V62/11621-02XE-T	D	SOIC	14	50	507	8	3940	4.32

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
C

14   8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   D

1   7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0.006 (0,15) each side.
         D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E. Reference JEDEC MS−012 variation AB.

TEXAS
INSTRUMENTS
www.ti.com

D (R−PDSO−G14)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)

12x1,27

14x0,55

12x1,27

14x1,50

5,40

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283−3/E 08/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

TEXAS INSTRUMENTS
www.ti.com

.228-.244 TYP
[5.80-6.19]

PIN 1 ID AREA

6X .050
[1.27]

2X
.150
[3.81]

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

.189-.197
[4.81-5.00]
NOTE 3

.150-.157
[3.81-3.98]
NOTE 4

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010 TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
₵

SEE
DETAILS

1

8

8X (.024)
[0.6]

SYMM
₵

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

SYMM

1

8X (.024)
[0.6]

SYMM

8

(R.002) TYP
[0.05]

4

5

6X (.050)
[1.27]

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C   02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER