HYBRID
MEMORY PRODUCTS LIMITED

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32K x 8 SRAM

MSM832-025/35/45/55/70

Issue 2.1 : August 1994

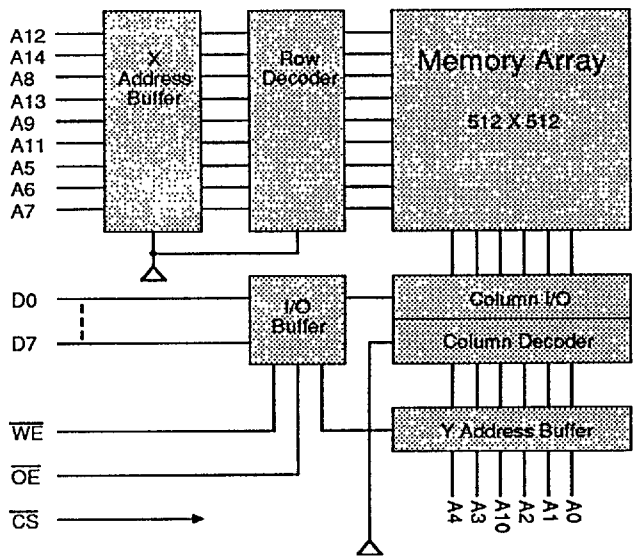
PRELIMINARY

32,768 x 8 CMOS High Speed Static RAM

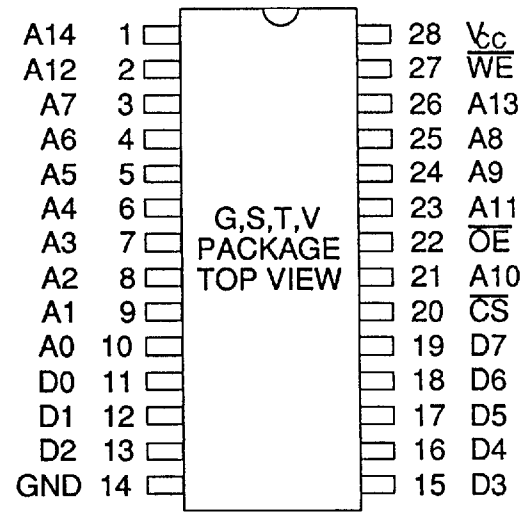
Features

- Fast Access Times of 35 to 70 ns. (25ns in development)
- JEDEC Standard 28 pin DIL footprint.
- Available in 28 pin VIL™ and FlatPack packages.
- Operating Power 300 mW (typical)
  Low Power Standby 30 µW (typical) -L version.
- Completely Static Operation.
- 2.0V Battery back-up Capability.
- Directly TTL compatible.
- Common Data Inputs and Outputs.
- May be Screened in accordance with MIL-STD-883.

Block Diagram



Pin Definition



Pin Functions

A0~A14	Address inputs
D0~D7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{cc}	Power (+5V)
GND	Ground

Package Details Package dimensions and outlines are shown on pages 6&7.

Pin Count	Description	Package Type	Material	Pin Out
28	0.6" Dual-in-Line (DIP)	S	Ceramic	JEDEC
28	0.3" Dual-in-Line (DIP)	T	Ceramic	JEDEC
28	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
28	Bottom Brazed FlatPack	G	Ceramic	JEDEC

VIL™ is a trademark of Mosaic Semiconductor Inc. (US Patent Des. 316,251) which with Hybrid Memory Products Ltd. is part of the Implex plc group.

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 2.5V for less than 10ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (Suffix **I**)
	T_{AM}	-55	-	125	°C (Suffix **M, MB)**

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN} = 0V to V_{CC}	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC}	-	-	2	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0 mA	-	-	100	mA
Average Supply Current	I_{CC1}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA, Min. Cycle, Duty = 100%	-	60	130	mA
Standby Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, I/P's static	-	15	30	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC}-0.2V, 0.2V ≥ V_{IN} ≥ V_{CC}-0.2V	-	0.02	2	mA
-L Version	I_{SB2}	As above	-	2	400	µA
Output Voltage	V_{OL}	I_{OL}= 8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}= -4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V,T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%,T_A=25°C)

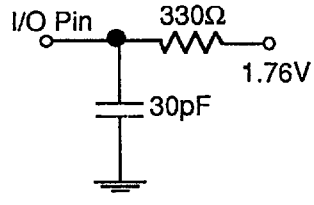
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN} = 0V	-	6	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$= 0V	-	10	pF

Note: This parameter is sampled and not 100% tested.

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load

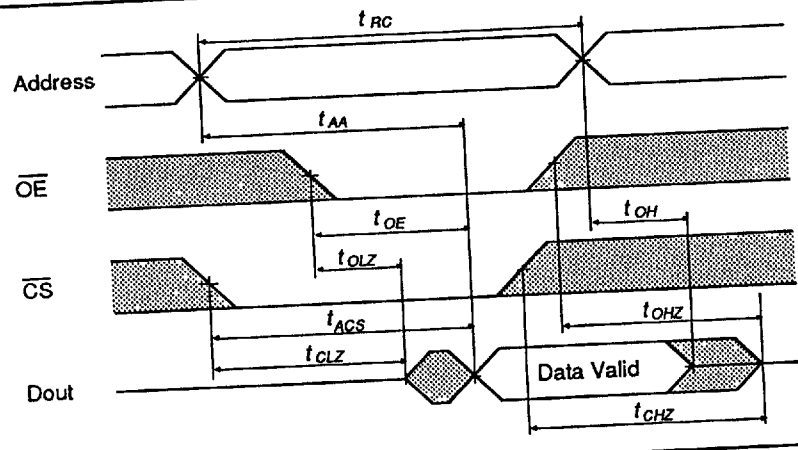


Electrical Characteristics & Recommended AC Operating Conditions

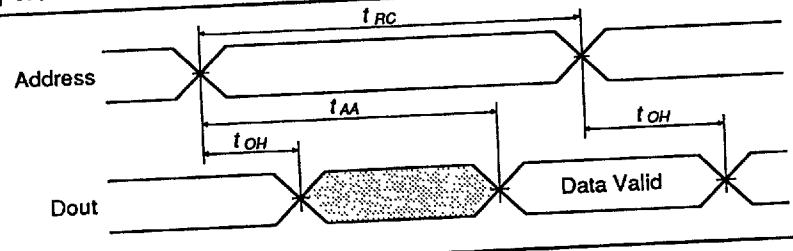
Read Cycle

Parameter	Symbol	-35 min	-35 max	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit
Read Cycle Time	t_{RC}	35	-	45	-	55	-	70	-	ns
Address Access Time	t_{AA}	-	35	-	45	-	55	-	70	ns
Chip Select Access Time	t_{ACS}	-	35	-	45	-	55	-	60	ns
Output Enable to Output Valid	t_{OE}	-	15	-	20	-	25	-	30	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z(5)	t_{CLZ}	5	-	5	-	5	-	5	-	ns
Output Enable to Output in Low Z(5)	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z(5)	t_{CHZ}	0	15	0	20	0	25	0	30	ns
Output Disable to Output in High Z(5)	t_{OHZ}	0	15	0	20	0	25	0	30	ns

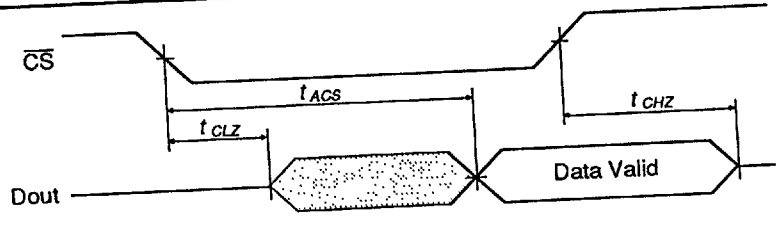
Read Cycle 1 Timing Waveform (1)



Read Cycle 2 Timing Waveform (1) (2) (4)



Read Cycle 3 Timing Waveform (1) (3) (4)



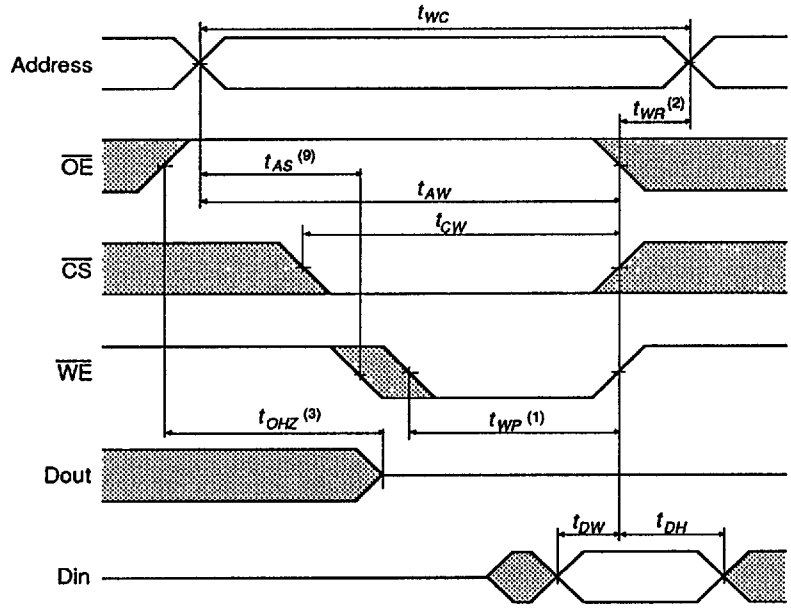
Notes: (1) $\overline{WE}$ is High for Read Cycle.
(2) Device is continuously selected, $\overline{CS}=V_{IL}$.
(3) Address valid prior to or coincident with $\overline{CS}$ transition Low.
(4) $\overline{OE}=V_{IL}$.
(5) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle

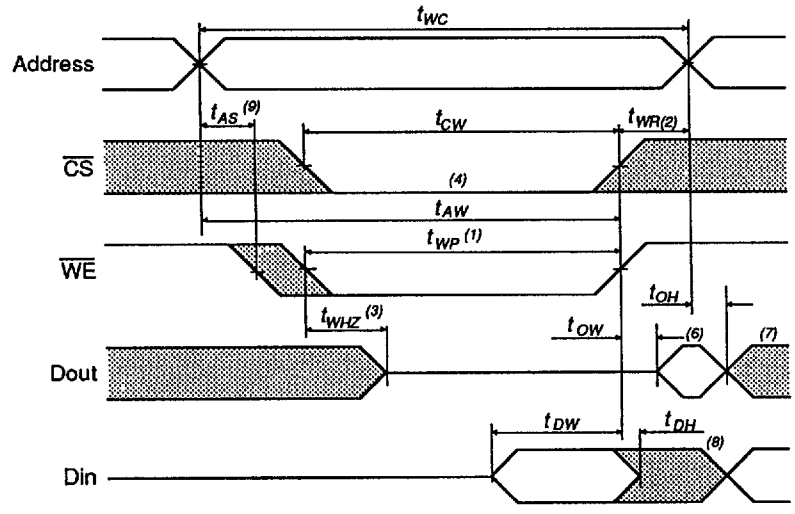
Parameter	Symbol	-35 min.	-35 max	-45 min.	-45 max	-55 min.	-55 max	-70 min.	-70 max	Unit
Write Cycle Time	t_{WC}	35	-	45	-	55	-	70	-	ns
Chip Selection to End of Write	t_{CW}	30	-	40	-	40	-	45	-	ns
Address Valid to End of Write	t_{AW}	30	-	40	-	40	-	45	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	20	-	25	-	25	-	25	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z[9]	t_{WHZ}	0	15	0	20	0	20	0	20	ns
Data to Write Time Overlap	t_{DW}	15	-	20	-	20	-	20	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW} *	5	-	5	-	5	-	5	-	ns

Note: t_{OW} * is 'guaranteed by design' only.

Write Cycle 1 Timing Waveform ($\overline{OE}$ Clock)



Write Cycle 2 Timing Waveform ($\overline{OE}$ Low Fixed)



AC Write Characteristics Notes

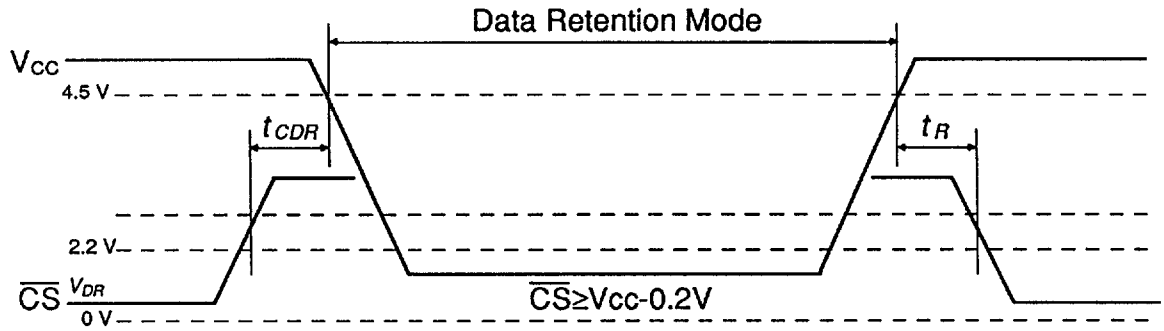
(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) $\overline{WE}$ must be high during all address transitions except when the device is deselected with $\overline{CS}$.
(10) t_{WHZ} is defined as the time at which the outputs achieve the open circuit conditions and is not referenced to output voltage levels. This parameter is sampled and not 100% tested.
(11) t_{OW} is 'guaranteed by design' only.

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$≥V_{CC}-0.2V	2.0	-	-	V
Data Retention Current		V_{CC}=3.0V,$\overline{CS}$≥ 2.8V				
	I_{CCDR1}	T_{OP}=T_A	-	1	50	µA
	I_{CCDR2}	T_{OP}=T_{AI}		**TBA**		µA
	I_{CCDR3}	T_{OP}=T_{AM}	-	-	200	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC}(1)	-	-	ns

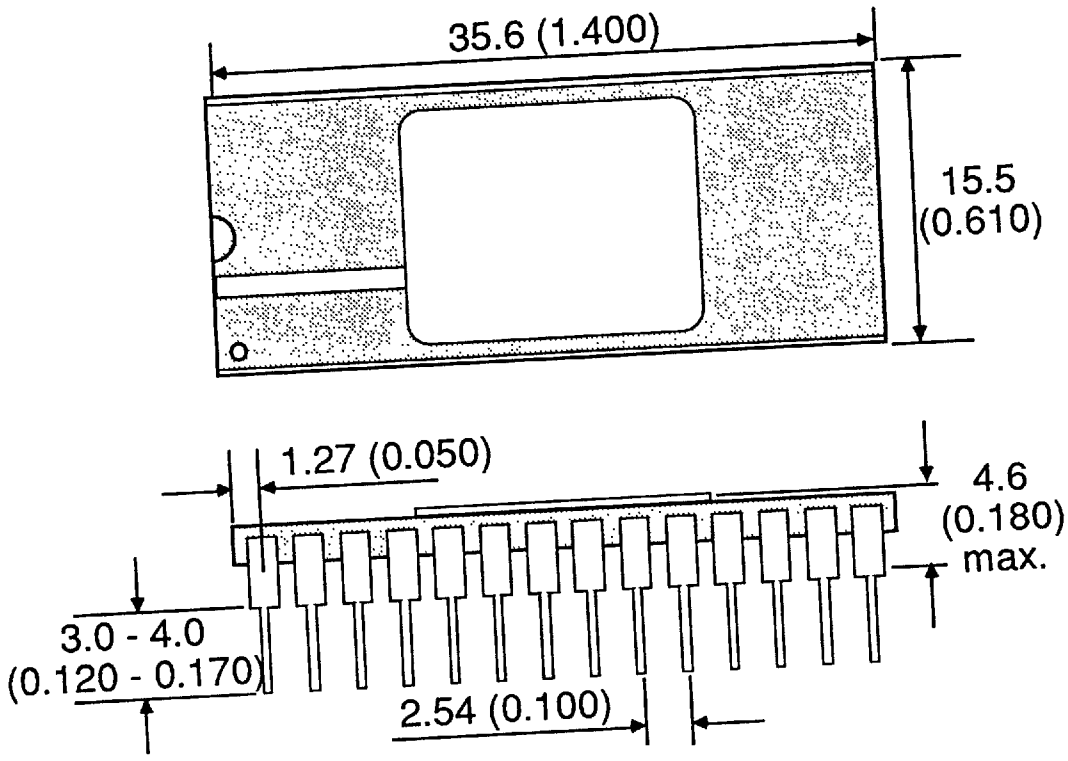
Notes (1) t_{RC}=Read Cycle Time

Data Retention Waveform

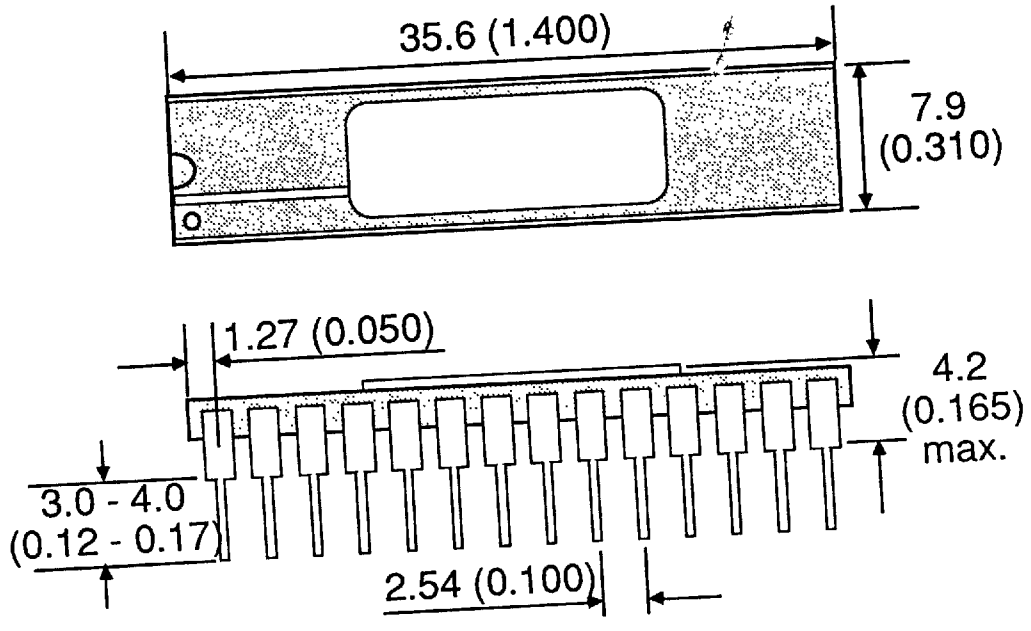


Package Details dimensions in mm (inches)

28 pin 0.6" Dual-In-Line (DIL) - 'S' Package



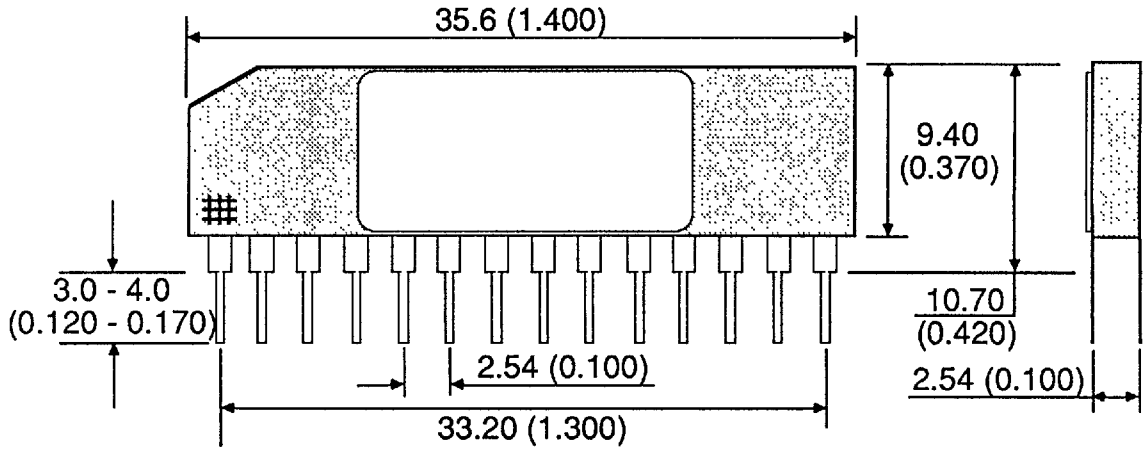
28 pin 0.3" Dual-In-Line (DIL) - 'T' Package



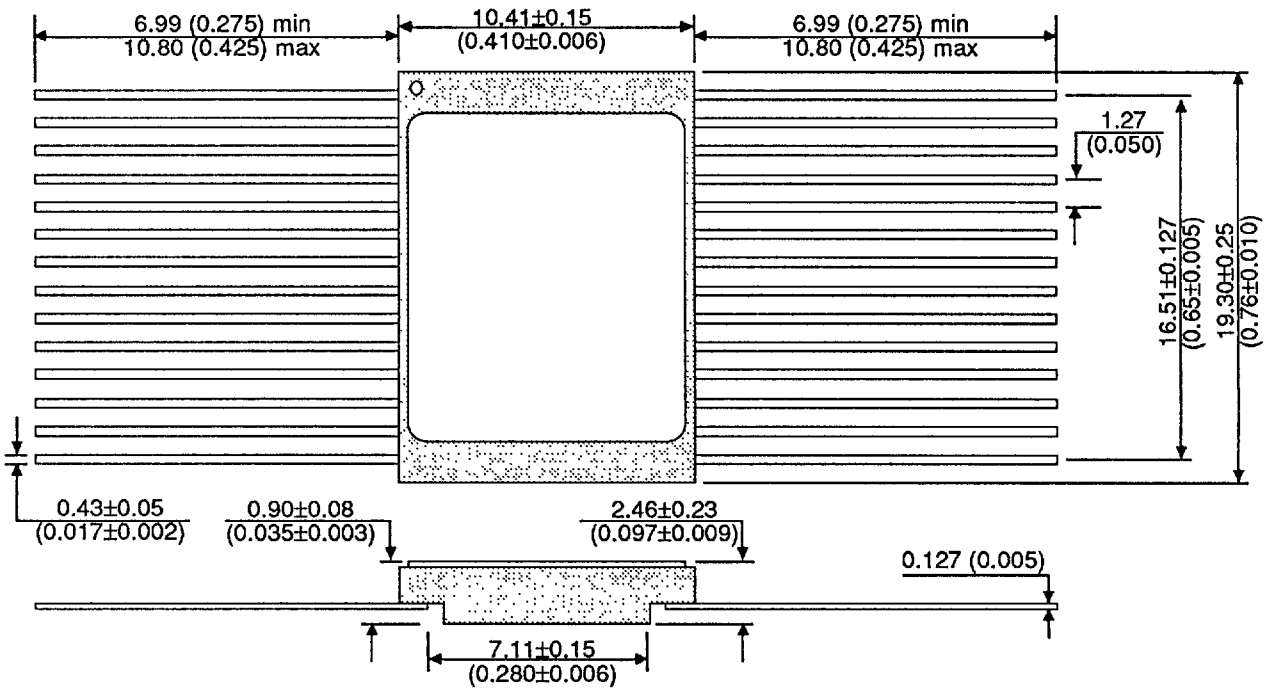
Tolerance on all dimensions ±0.254 (0.01)

Package Details dimensions in mm (inches)

28 pin 0.1" Vertical-In-Line (VIL) - 'V' Package



28 Lead FlatPack - 'G' Package



Tolerance on all dimensions ±0.254 (0.01)

Military Screening Procedure

Component Screening Flow for high reliability product is in accordance with Mil-883C method 5004 .

MB COMPONENT SCREENING FLOW		
SCREEN	***TEST METHOD***	***LEVEL***
Visual and Mechanical		
Internal visual	2010 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles,-65°C to +150°C)	100%
Constant acceleration	2001 Condition E (Y, only) (30,000g)	100%
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C,160hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post-burn-in at T_A=+25°C	5%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

MSM832SLMB-45

Speed
- 025 = Under development
- 35 = 35 ns
- 45 = 45 ns
- 55 = 55 ns
- 70 = 70 ns

Temp. range/screening
- Blank = Commercial
- I = Industrial
- M = Military
- MB = May be secreened in accordance with MIL-STD-883.

Power Consumption
- Blank = Standard Power
- L = Low Power

Package
- S = 28 pin 0.6" DIL
- T = 28 pin 0.3" DIL
- V = 28 pin 0.1" VIL
- G = 28 lead FlatPack

4651092 0000834 279

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