STK14C88

32K x 8 *AutoStore*™ nvSRAM High Performance CMOS Nonvolatile Static RAM

ADVANCE

FEATURES

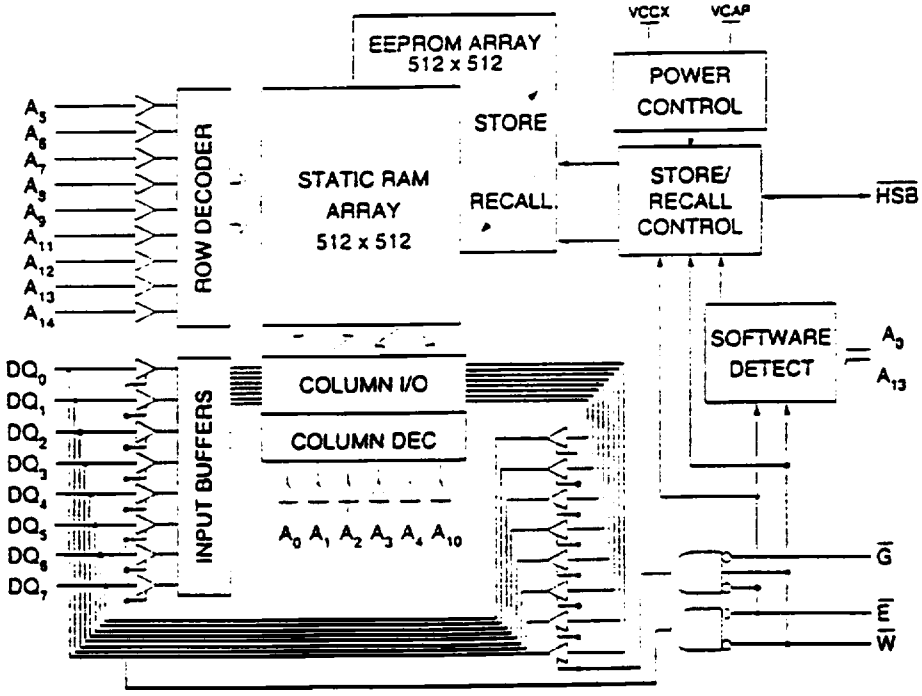
- 25ns, 35ns and 45ns SRAM Access Times
- "Hands-off" Store with 100µF Capacitor on Power Down
- Store to EEPROM Initiated by Hardware, Software or *AutoStore*™ on Power Down
- Recall to SRAM Initiated by Software or Power Restore
- 15mA I_{CC} at 200ns Cycle Time
- Unlimited Recalls from EEPROM to SRAM
- 100,000 Store Cycles to EEPROM
- 10 Year Data Retention in EEPROM
- Single 5V ± 10% Operation
- Commercial and Industrial Temperatures
- 32 Pin SOIC and 32 Pin 300 mil DIP Packages

DESCRIPTION

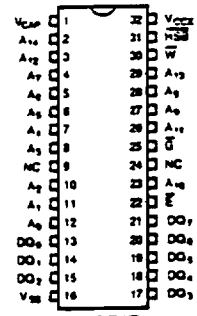
The Simtek STK14C88 is a fast static RAM with a nonvolatile, electrically-erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent, nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation) can take place automatically on power down. Transfers from the EEPROM to the SRAM (the *RECALL* operation) take place automatically on restoration of power. Initiation of STORE and RECALL cycles can also be software controlled by entering specific read sequences. A Hardware *STORE* may be initiated with a single pin.

MIL-STD-883 device also available (STK14C38-M).

LOGIC BLOCK DIAGRAM



PACKAGE DIAGRAMS



32 - 300 PDIP
32 - 300 SOIC

PIN NAMES

A_0 - A_{14}	Address Inputs
DQ_0 -DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{HSB}$	Hardware Store Busy (I/O)
V_{CCX}	Power (+5V)
V_{CAP}	Capacitor
V_{SS}	Ground

STK14C88

This is advance information on a new product now in development. Details are subject to change without notice.
Revision 2 - September 1996

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on input relative to V_{SS} ..... –0.5V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} or $\overline{HSB}$ ..... –0.5V to (V_{CC} + 0.5V)
Temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C
Power dissipation 1W
DC output current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)[e]

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		100 85 70		110 95 85	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns
I_{CC_2}[c]	Average V_{CC} Current During STORE		7		7	mA	All Inputs Don't Care
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns		15		15	mA	$\overline{W} \geq (V_{CC} - 0.2V)$ All others cycling, CMOS levels
I_{CC_4}[c]	Average V_{CAP} Current During *AutoStore*™ Cycle		4		4	mA	All Inputs Don't Care
I_{SB_1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		35 32 30		35 32 30	mA mA mA	t_{AVAV} = 25ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 35ns, $\overline{E} \geq V_{IH}$ t_{AVAV} = 45ns, $\overline{E} \geq V_{IH}$
I_{SB_2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		3		3	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±1		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}, $\overline{E}$ or $\overline{G} \geq V_{IH}$
V_{IH}	Input Logic "1" Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic "1" Voltage	2.4		2.4		V	I_{OUT} = –4mA except $\overline{HSB}$
V_{OL}	Output Logic "0" Voltage		0.4		0.4	V	I_{OUT} = 8mA except $\overline{HSB}$
V_{BL}	Logic "0" Voltage on $\overline{HSB}$ Output		0.4		0.4	V	I_{OUT} = 3mA
T_A	Operating Temperature	0	70	-40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC_2} and I_{CC_4} are the average currents required for the duration of the respective *STORE* cycles (t_{STORE}).
Note d: $\overline{E} \geq V_{IH}$ will not produce standby current levels until any nonvolatile cycle in progress has timed out.
Note e: V_{CC} reference levels throughout this datasheet refer to V_{CCX} if that is where the power supply connection is made, or V_{CAP} if V_{CCX} is connected to ground.

AC TEST CONDITIONS

Input pulse levels ..... 0V to 3V
Input rise and fall times ..... ≤ 5ns
Input and output timing reference levels 1.5V
Output load ..... See Figure 1

CAPACITANCE[f] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output capacitance	7	pF	ΔV = 0 to 3V

Note f: These parameters are guaranteed but not tested.

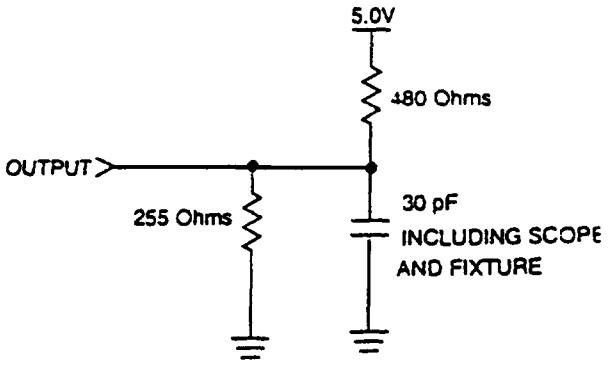


Figure 1: AC Output Loading

SRAM MEMORY OPERATION

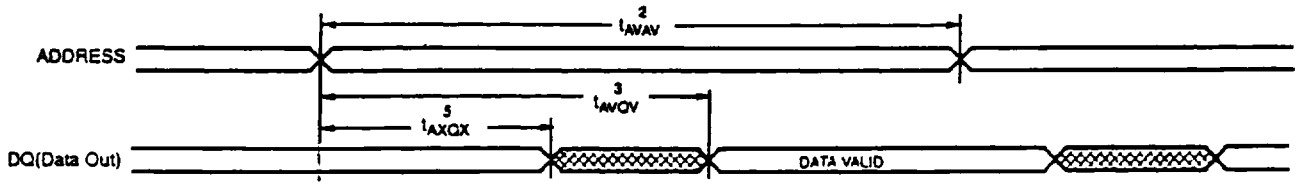
READ CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

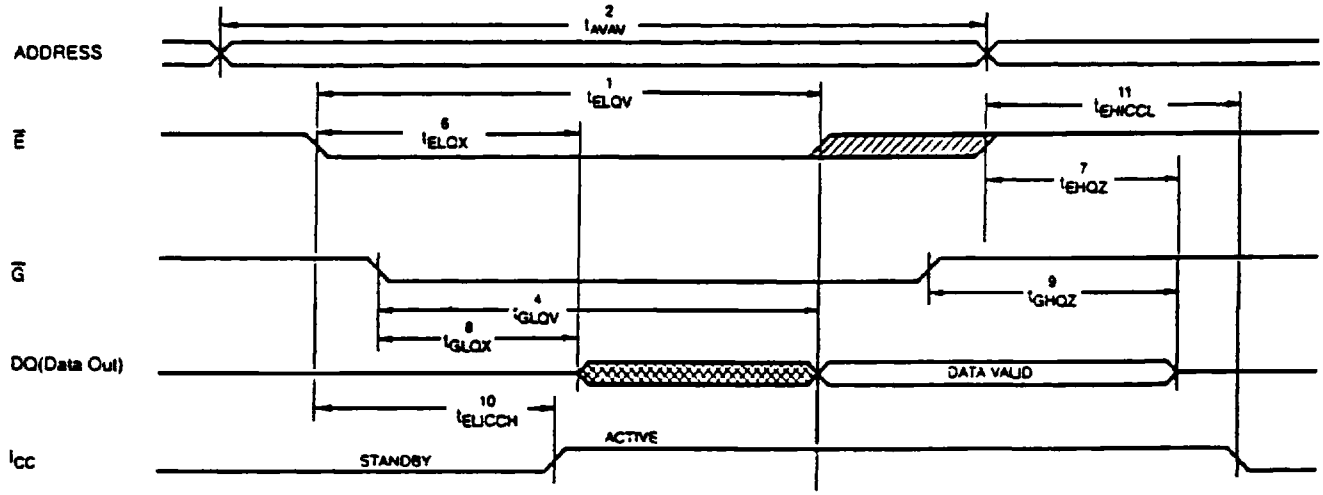
NO.	SYMBOLS		PARAMETER	STK14C88-25		STK14C88-35		STK14C88-45		UNITS
	#1, #2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns
2	t_{AVAV}[g]	t_{RC}	Read Cycle Time	25		35		45		ns
3	t_{AVQV}[h]	t_{AA}	Address Access Time		25		35		45	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		10		15		20	ns
5	t_{AXQX}[h]	t_{OH}	Output Hold after Address Change	5		5		5		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns
7	t_{EHQZ}[i]	t_{HZ}	Chip Disable to Output Inactive		10		13		15	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
9	t_{GHQZ}[i]	t_{OHZ}	Output Disable to Output Inactive		10		13		15	ns
10	t_{ELICCH}[f]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
11	t_{EHICCL}[f]	t_{PS}	Chip Disable to Power Standby		25		35		45	ns

Note g: $\overline{W}$ and $\overline{HSB}$ must be high during SRAM read cycles.
Note h: Device is continuously selected with $\overline{E}$ and $\overline{G}$ both low.
Note i: Measured ± 200mV from steady state output voltage.

READ CYCLE #1: Address Controlled[g, h]



READ CYCLE #2: $\overline{E}$ Controlled[g]



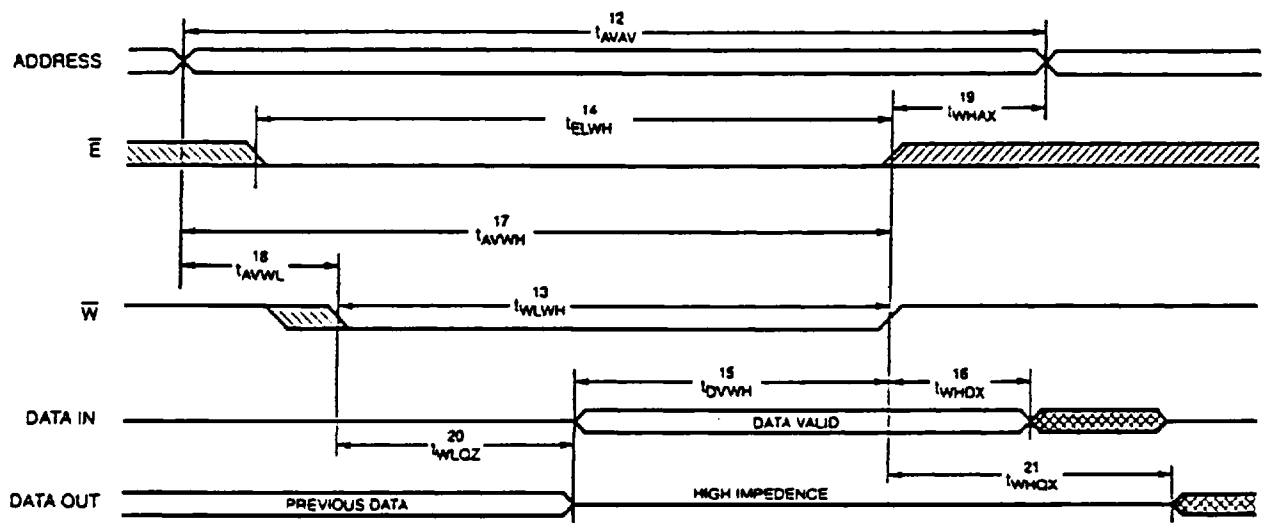
WRITE CYCLES #1 & #2

(V_{CC} = 5.0V ± 10%)

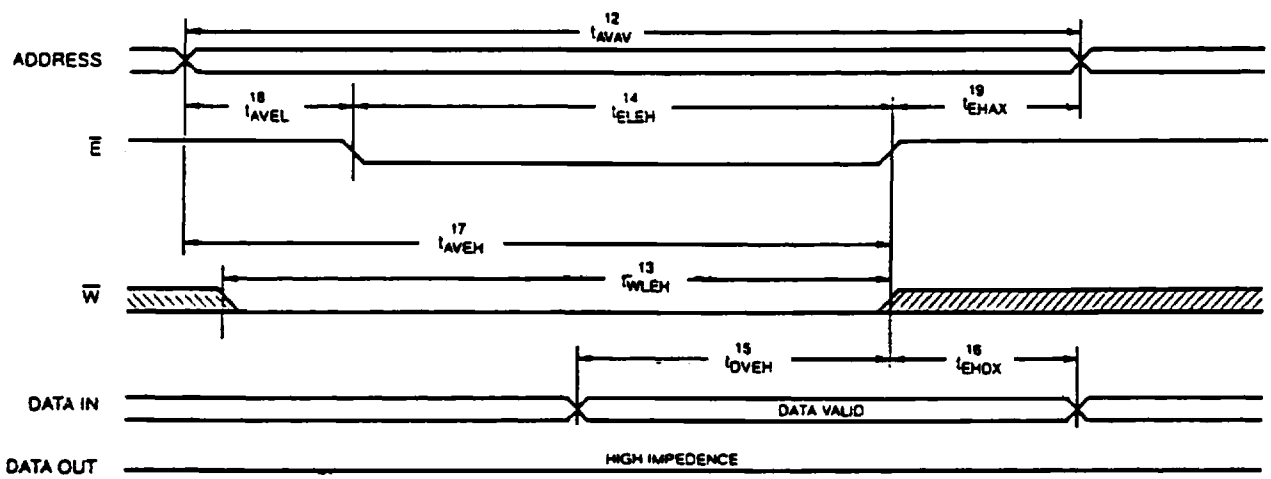
NO.	SYMBOLS			PARAMETER	STK14C88-25		STK14C88-35		STK14C88-45		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		12		15		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns
20	t_{WLQZ}[i, j]		t_{WZ}	Write Enable to Output Disable		10		13		15	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		5		ns

Note j: If $\overline{W}$ is low when $\overline{E}$ goes low the outputs remain in the high impedance state.
Note k: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note l: $\overline{HSB}$ must be high during SRAM Write cycles.

WRITE CYCLE #1: $\overline{W}$ Controlled[k, l]



WRITE CYCLE #2: $\overline{E}$ Controlled[k, l]



NONVOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{HSB}$	A_{13} - A_0 (hex)	MODE	I/O	POWER	NOTES
H	X	H	X	Not Selected	Output High Z	Standby	
L	H	H	X	Read SRAM	Output Data	Active	p
L	L	H	X	Write SRAM	Input Data	Active	
X	X	L	X	Nonvolatile *STORE*	Output High Z	I_{CC2}	m
L	H	H	0E38	Read SRAM	Output Data	Active	n, o, p
			31C7	Read SRAM	Output Data		
			03E0	Read SRAM	Output Data		
			3C1F	Read SRAM	Output Data		
			303F	Read SRAM	Output Data		
			0FC0	Nonvolatile *STORE*	Output High Z	I_{CC2}	
L	H	H	0E38	Read SRAM	Output Data	Active	n, o, p
			31C7	Read SRAM	Output Data		
			03E0	Read SRAM	Output Data		
			3C1F	Read SRAM	Output Data		
			303F	Read SRAM	Output Data		
			0C63	Nonvolatile *RECALL*	Output High Z		

Note m: $\overline{HSB}$ store operation occurs only if an SRAM write has been done since the last nonvolatile cycle. After the store (if any) completes, the part will go into standby mode inhibiting all operations until $\overline{HSB}$ rises.
Note n: The six consecutive addresses must be in order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note o: While there are 15 addresses on the STK14C88, only the lower 14 are used to control software modes.
Note p: I/O state assumes $\overline{G} \leq V_{IL}$. Activation of nonvolatile cycles does not depend on the state of $\overline{G}$.

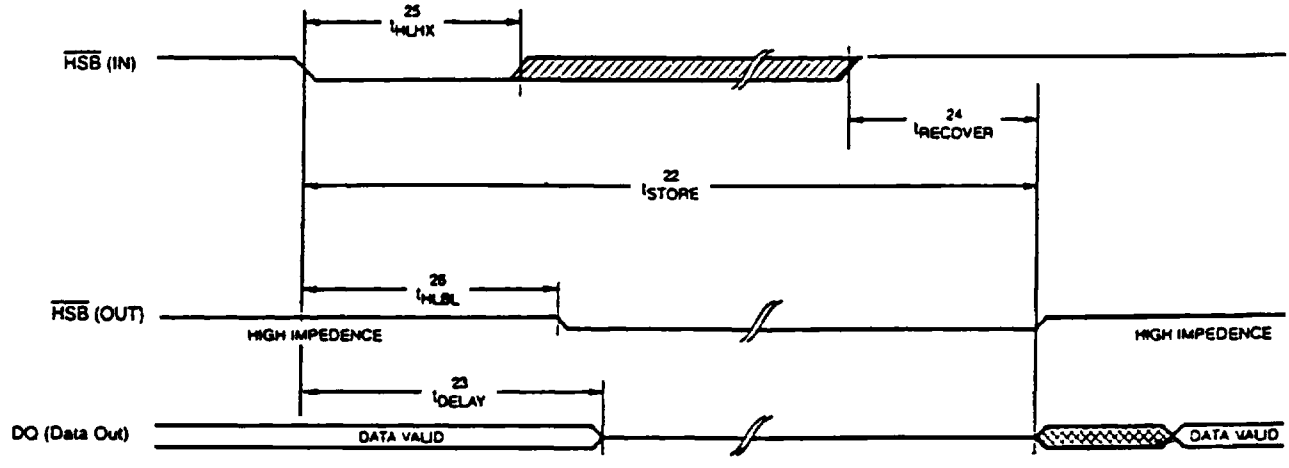
HARDWARE STORE CYCLE

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK14C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
22	t_{HLHZ}	t_{STORE}	STORE Cycle Duration		10	ms	i, q
23	t_{HLQZ}	t_{DELAY}	Time Allowed to Complete SRAM Cycle	1		µs	i, q
24	t_{HHQX}	$t_{RECOVER}$	Hardware Store High to Inhibit Off		600	ns	q, r
25	t_{HLHX}		Hardware Store Pulse Width	20		ns	
26	t_{HLBL}		Hardware Store Low to Store Busy		300	ns	

Note q: $\overline{E}$ and $\overline{G}$ low and $\overline{W}$ high for output behavior.
Note r: $t_{RECOVER}$ is only applicable after t_{STORE} is complete.

HARDWARE STORE CYCLE



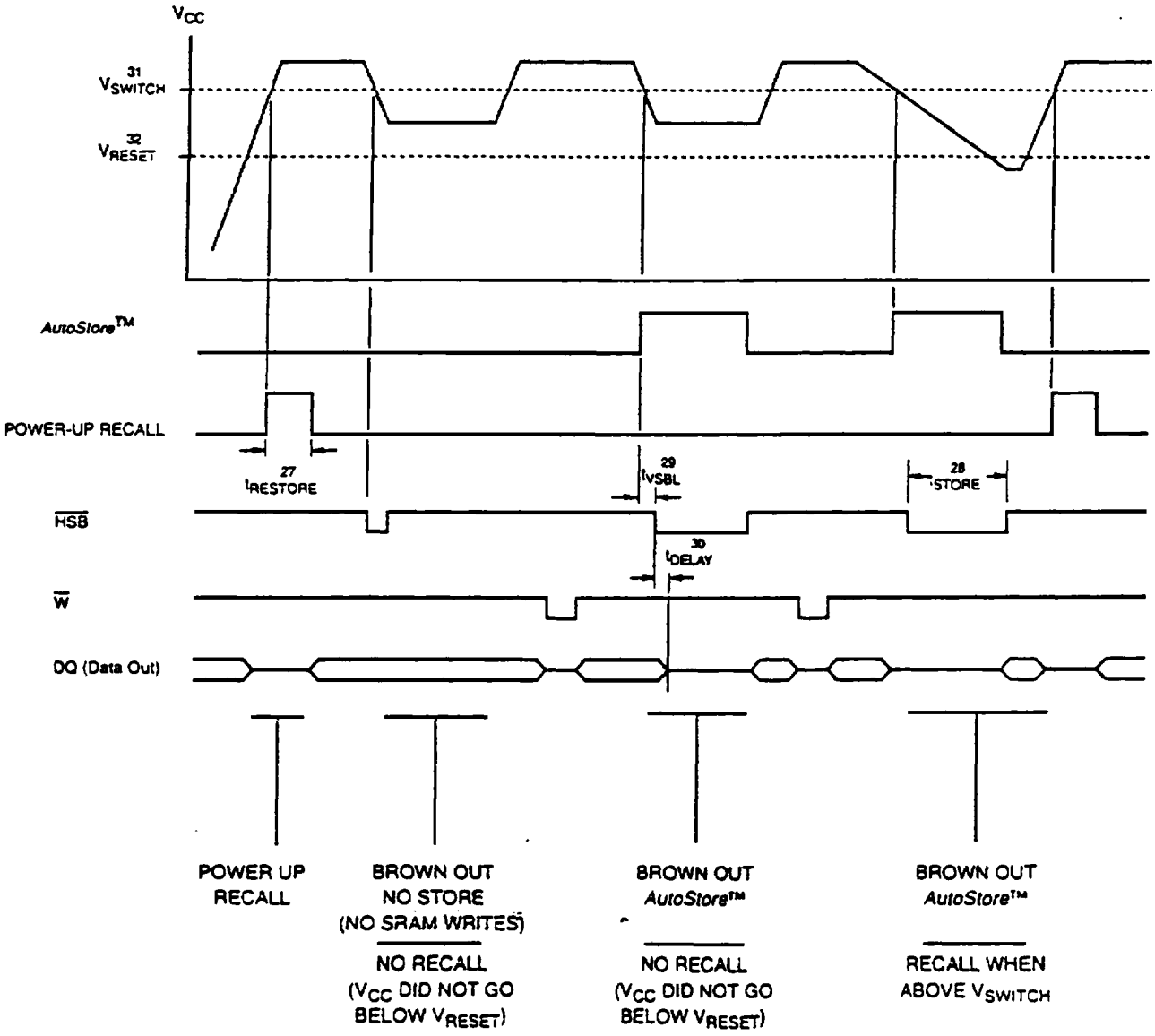
AutoStore™ / POWER-UP RECALL

(V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK14C88		UNITS	NOTES
	Standard	Alternate		MIN	MAX		
27	$t_{RESTORE}$		Power Up RECALL Duration		550	µs	s
28	t_{STORE}	t_{HLHZ}	STORE Cycle Duration		10	ms	q, t
29	t_{VSBL}		Low Voltage Trigger (V_{SWITCH}) to $\overline{HSB}$ Low		300	ns	l
30	t_{DELAY}	t_{BLQZ}	Time Allowed to Complete SRAM Cycle	1		µs	q
31	V_{SWITCH}		Low Voltage Trigger Level	4.0	4.5	V	
32	V_{RESET}		Low Voltage Reset Level		3.8	V	f

Note s: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.
Note t: $\overline{HSB}$ is asserted low for 1µs when V_{CAP} drops through V_{SWITCH}. If an SRAM Write has not taken place since the last nonvolatile cycle, $\overline{HSB}$ will be released and no STORE will take place.

AutoStore™ / POWER-UP RECALL



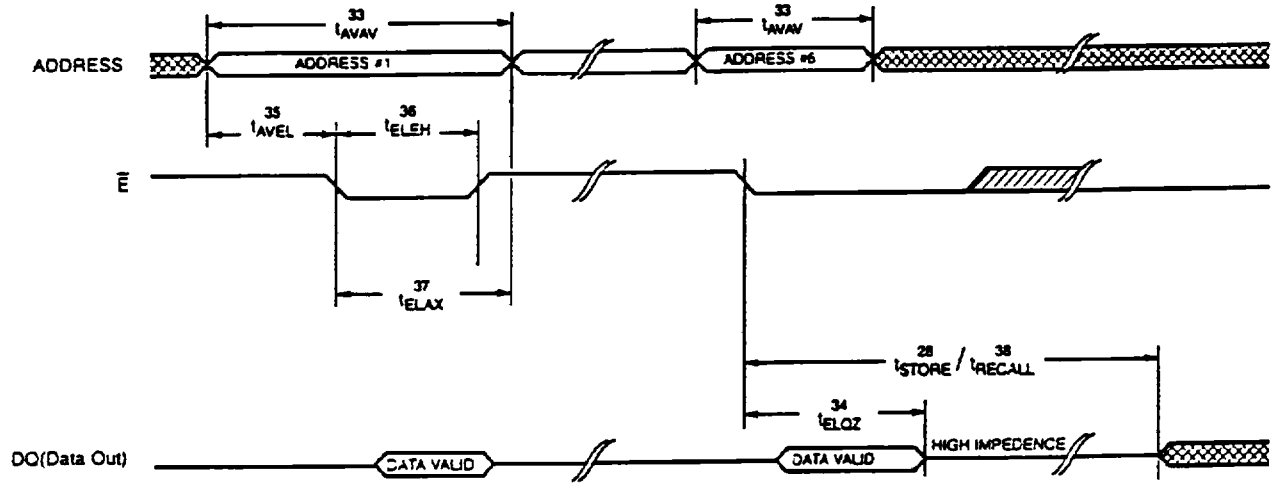
SOFTWARE CONTROLLED STORE AND RECALL CYCLES[v] (V_{CC} = 5.0V ± 10%)

NO.	SYMBOLS		PARAMETER	STK14C88-25		STK14C88-35		STK14C88-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
33	t_{AVAV}	t_{RC}	*STORE/RECALL* Initiation Cycle Time	25		35		45		ns	q
34	t_{ELQZ}		End of Sequence to Outputs Inactive		600		600		600	ns	q, u
35	t_{AVEL}	t_{AS}	Address Set-up Time	0		0		0		ns	u
36	t_{ELEH}	t_{CW}	Clock Pulse Width	20		25		30		ns	u
37	t_{ELAX}		Address Hold Time	15		15		15		ns	u
38	t_{RECALL}		Recall Duration		20		20		20	µs	

Note u: The software sequence is clocked with $\overline{E}$ controlled reads.

Note v: The six consecutive addresses must be in the order listed in the MODE SELECTION table - (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a STORE cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a RECALL cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE CYCLE: $\overline{E}$ Controlled[v]



DEVICE OPERATION

The STK14C88 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the *STORE* operation) or from EEPROM to SRAM (the *RECALL* operation). In this mode SRAM functions are disabled.

NOISE CONSIDERATIONS

The STK14C88 is a high speed memory and so must have a high frequency bypass capacitor of approximately 0.1µF connected between DUT V_{CAP} and V_{SS}, using leads and traces that are as short as possible. As with all high speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK14C88 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ and $\overline{HSB}$ are high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ CYCLE #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ CYCLE #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high, or $\overline{W}$ or $\overline{HSB}$ is brought low.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low and $\overline{HSB}$ is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

POWER UP RECALL

During power up, or after any low power condition (V_{CAP} < V_{RESET}),an internal recall request will be latched. When V_{CAP} once again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

SOFTWARE NONVOLATILE STORE

The STK14C88 software STORE cycle is initiated by executing sequential $\overline{E}$ controlled READ cycles from six specific address locations. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0FC0 (hex)	Initiate STORE cycle

The software sequence must be clocked with $\overline{E}$ controlled reads.

Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE RECALL

A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle,

the following sequence of $\overline{E}$ controlled READ operations must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0C63 (hex)	Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

AutoStore™ OPERATION

The STK14C88 can be powered in one of three modes.

During normal *AutoStore*™ operation, the STK14C88 will draw current from V_{CCX} to charge a capacitor connected to the V_{CAP} pin. This stored charge will be used by the chip to perform a single STORE operation. After power up, when the voltage on the V_{CAP} pin drops below V_{SWITCH}, the part will automatically disconnect the V_{CAP} pin from V_{CCX} and initiate a STORE operation.

Figure 2 shows the proper connection of capacitors for automatic store operation. A charge storage capacitor having a capacity of at least 100µf (± 20%) rated at 6V should be provided.

In system power mode (Figure 4) both V_{CCX} and V_{CAP} are connected to the +5V power supply without the 100µF capacitor. In this mode the *AutoStore*™ function of the STK14C88 will operate on the stored system charge as power goes down. The user must however guarantee that V_{CCX} does not drop below 3.6V during the 10ms store cycle.

If an automatic STORE on power loss is not required, then V_{CCX} can be tied to ground and +5V applied to V_{CAP} (Figure 3). This is the "AutoStore™ Inhibit" mode in which the *AutoStore*™ function is disabled. If the STK14C88 is operated in this configuration, references to V_{CCX} should be changed to V_{CAP} throughout this data sheet. In this mode, STORE operations may be triggered through software control or the $\overline{HSB}$ pin. It is not permissable to change between these three options "on the fly".

In order to prevent unneeded STORE operations, automatic STOREs as well as those initiated by externally driving $\overline{HSB}$ low will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. An optional pull up resistor is shown connected to $\overline{HSB}$. This can be used to signal the system that the *AutoStore*™ cycle is in progress.

$\overline{HSB}$ OPERATION

The STK14C88 provides the $\overline{HSB}$ pin for controlling and acknowledging the STORE operations. The $\overline{HSB}$ pin is used to request a hardware STORE cycle. When the $\overline{HSB}$ pin is driven low, the STK14C88 will conditionally initiate a STORE operation after t_{DELAY}: an actual STORE cycle will only begin if a WRITE to the SRAM took place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin acts as an open drain

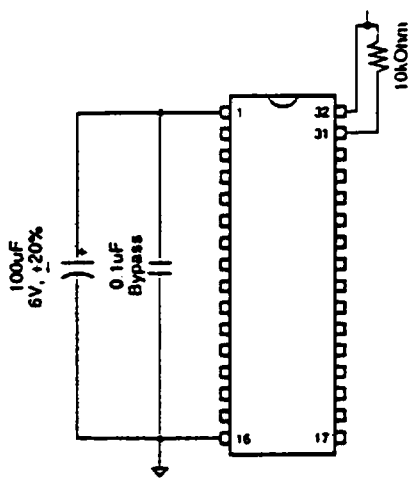


Figure 2: AutoStore Mode

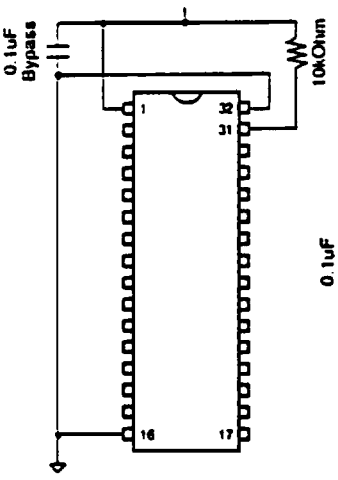


Figure 3: AutoStore Inhibit Mode

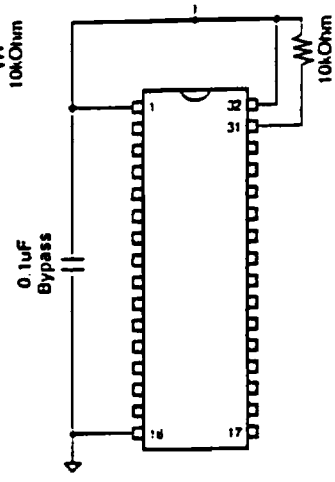


Figure 4: System Power Mode

driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when $\overline{HSB}$ is driven low or after an *AutoStore*™ cycle is requested and $\overline{HSB}$ is pulled low, are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes low, the STK14C88 will continue SRAM operations for t_{DELAY}. During t_{DELAY}, multiple SRAM READ operations may take place. If a WRITE is in progress when $\overline{HSB}$ is pulled low it will be allowed a time, t_{DELAY}, to complete. However, any SRAM WRITE cycles requested after the DUT pulls $\overline{HSB}$ low will be inhibited.

The $\overline{HSB}$ pin can be used to synchronize multiple STK14C88s while using a single larger capacitor. To operate in this mode the $\overline{HSB}$ pin should be connected together to the $\overline{HSB}$ pins from the other STK14C88s. An external pull up resistor to +5V is required since $\overline{HSB}$ acts as an open drain pull down. Do not connect this or any other pull-up to the V_{CAP} pin. The V_{CAP} pins from the other STK14C88 parts can be tied together and share a single capacitor. The capacitor size must be scaled by the number of devices connected to it. When any one of the STK14C88s detects a power loss and asserts $\overline{HSB}$, the common $\overline{HSB}$ pin will cause all parts to request a STORE cycle (a STORE will take place in those STK14C88s that have been written since the last nonvolatile cycle).

During any STORE operation, regardless of how it was initiated, the STK14C88 will continue to drive the $\overline{HSB}$ pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the STK14C88 will remain disabled until the $\overline{HSB}$ pin is brought high.

HARDWARE PROTECT

The STK14C88 offers hardware protection against inadvertent STORE operation during low voltage conditions. When $V_{CAP} < V_{SWITCH}$ all externally initiated STORE operations will be inhibited.

AutoStore™ can be completely disabled by tying V_{CCX} to ground and applying +5V to V_{CAP}. This is the AutoStore™ Inhibit mode; STOREs are only initiated by explicit request using either the software sequence or the $\overline{HSB}$ pin in this mode.

LOW AVERAGE ACTIVE POWER

The STK14C88 will draw significantly less current when it is cycled at times longer than 35ns. Figure 5, below, shows the relationship between I_{CC} and READ cycle time. Worst case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 5.5V, 100% duty cycle on chip enable). Figure 6 shows the same relationship for WRITE cycles. If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled.

The overall average current drawn by the STK14C88 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READ's to WRITE's; 5) the operating temperature; 6) the V_{CC} level and; 7) I/O loading.

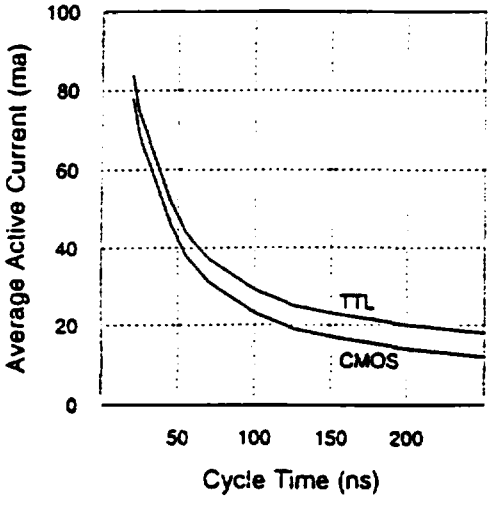


Fig. 5 - Icc (max) Reads

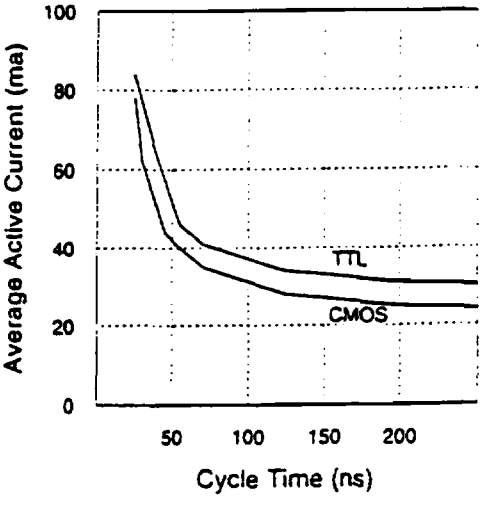
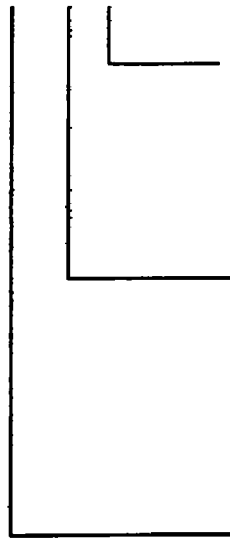


Fig. 6 - Icc (Max) Writes

ORDERING INFORMATION

STK14C88 - P 45 I



Temperature Range

Blank = Commercial (0 to 70 degrees C)

I = Industrial (-40 to 85 degrees C)

Access Time

25 = 25ns

35 = 35ns

45 = 45ns

Package

P = Plastic 32 pin 300 mil DIP

S = Plastic 32 pin 300 mil SOIC