CD54HC166/3A
CD54HCT166/3A

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay Clock to Output	t_{PLH} t_{PHL}	2	—	160	—	—	—	240	—	—	ns
		4.5	—	32•	—	40•	—	48•	—	60•	
		6	—	27	—	—	—	41	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Propagation Delay $\overline{MR}$ to Output	t_{PHL}	2	—	160	—	—	—	240	—	—	
		4.5	—	32	—	40	—	48	—	60	
		6	—	27	—	—	—	41	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I OPEN	GROUND	V_{CC} (6V)	STATIC BURN-IN II OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT166	13	1-12,14,15	16	13	8	1-7,9-12,14-16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**25 kHz**
CD54HC/HCT166	—	2,4,6,8,10,12	13	3,5,9,11, 14-16	7	1

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

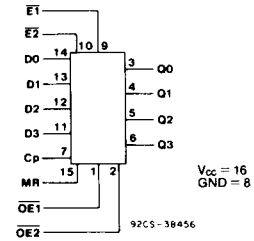
CD54HC173/3A
CD54HCT173/3A

Quad D-Type Flip-Flop, 3-State

The RCA CD54HC173 and CD54HCT173 high-speed three-state quad D-type flip-flops are fabricated with silicon-gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low-power Schottky devices. The buffered outputs can drive 15 LSTTL loads. The large output drive capability and three-state feature make these parts ideally suited for interfacing with bus lines in bus-oriented systems.

The four D-type flip-flops operate synchronously from a common clock. The outputs are in the three-state mode when either of the two output disable pins are at the logic "1" level. The input ENABLES allow the flip-flops to remain in their present states without having to disrupt the clock. If either of the two input ENABLES are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip-flops to remain in the same state. Reset is enabled by taking the MASTER RESET (MR) input to a logic "1" level. The data outputs change state on the positive-going edge of the clock.

The CD54HCT173 logic family is functionally as well as pin compatible with the standard 54LS logic family.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11

CD54HC173/3A
CD54HCT173/3A

Static Electrical Characteristics (Limits with black dots (•) are tested 100%) — Bus Type

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Output High (Source) Current I_{OH} Min. - TTL Load	25°C	4.5	3.98	—	—	0, 4.5	0, 4.5	-6•	—	mA
	-55°C / +125°C	4.5	3.70	—	—	0, 4.5	0, 4.5	-6•	—	
Output Low (Sink) Current I_{OL} Min. - TTL Load	25°C	4.5	0.26	—	—	0, 4.5	0, 4.5	6•	—	
	-55°C / +125°C	4.5	0.40	—	—	0, 4.5	0, 4.5	6•	—	
High Level Output Voltage V_{OH} - TTL Load	25°C	4.5	—	-6	—	1.35, 3.15	0.8, 2.0	3.98•	—	V
	-55°C / +125°C	4.5	—	-6	—	1.35, 3.15	0.8, 2.0	3.70•	—	
Low Level Output Voltage V_{OL} - TTL Load	25°C	4.5	—	6	—	1.35, 3.15	0.8, 2.0	—	0.26•	
	-55°C / +125°C	4.5	—	6	—	1.35, 3.15	0.8, 2.0	—	0.40•	
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
D0-D3	0.15
$\overline{E1}$ & $\overline{E2}$	0.15
CP	0.25
MR	0.2
$\overline{OE1}$ & $\overline{OE2}$	0.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay Clock Output	t_{PLH} t_{PHL}	2	—	200	—	—	—	300	—	—	ns
		4.5	—	40•	—	43•	—	60•	—	65•	
		6	—	34	—	—	—	51	—	—	
Propagation Delay MR to Output	t_{PHL}	2	—	175	—	—	—	265	—	—	
		4.5	—	35•	—	37•	—	53•	—	56•	
		6	—	30	—	—	—	45	—	—	
Propagation Delay, Output Enable to Q	t_{PLZ} t_{PHZ}	2	—	150	—	—	—	225	—	—	
		4.5	—	30•	—	30•	—	45•	—	45•	
		6	—	26	—	—	—	38	—	—	
	t_{PZL} t_{PZH}	2	—	150	—	—	—	225	—	—	
		4.5	—	30•	—	35•	—	45•	—	53•	
		6	—	26	—	—	—	38	—	—	
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	90	—	—	
		4.5	—	12	—	12	—	18	—	18	
		6	—	10	—	—	—	15	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	pF

CD54HC173/3A
CD54HC173/3A

Burn-In Test-Circuit Connections

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT173	3-6	1,2,7-15	16	3-6	8	1,2,7,9-16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT173	—	1,2,8-10,15	3-6	16	7	11-14

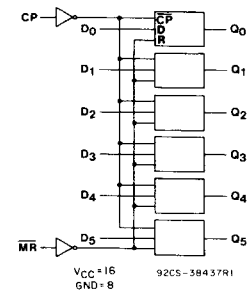
NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54HC174/3A
CD54HCT174/3A

Hex D-Type Flip-Flop w/RESET

The RCA CD54HC174 and CD54HCT174 are edge-triggered flip-flops which utilize silicon-gate CMOS circuitry to implement D-type flip-flops. They possess low power and speeds comparable to low-power Schottky TTL circuits. The devices contain six master-slave flip-flops with a common clock and common reset. Data on the D input having the specified setup and hold times are transferred to the Q output on the low to high transition of the CLOCK input. The $\overline{MR}$ input, when low, sets all outputs to a low state.

Each output can drive 10 low-power Schottky TTL equivalent loads. The CD54HCT174 is functionally as well as pin compatible to the 54LS174.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
CP	0.80
$\overline{MR}$	0.55
D	0.15

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.