

**DESCRIPTION:**

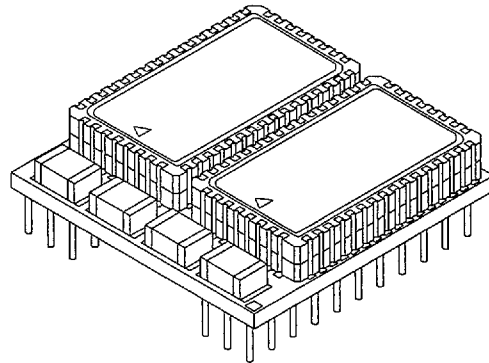
The DPS128X32CV3/DPS128X32BV3 "VERSA-STACK" module is a revolutionary new high speed memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) mounted on a co-fired ceramic substrate. It offers 4 Megabits of SRAM in a package envelope of 1.090 x 1.090 x 0.252 inches.

The DPS128X32CV3/DPS128X32BV3 contains four individual 128K x 8 SRAMs, packaged in their own hermetically sealed SLCCs making the module suitable for commercial, industrial and military applications.

By using SLCCs, the "Versa-Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount, module, or hybrid techniques.

The DPS128X32BV3 has one active low Chip Enable (CE) and while the DPS128X32CV3 an active low Chip Enable (CE) and an active high Select Line (SEL).

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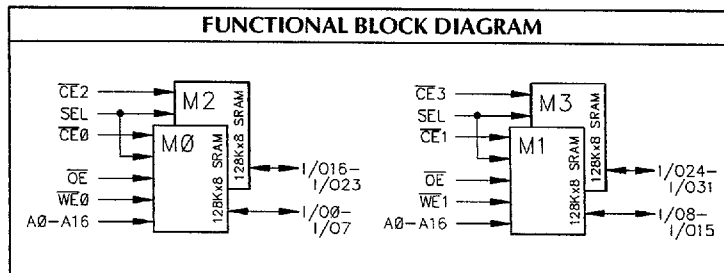


**FEATURES:**

- Organizations Available:  
128K x 32, 256K x 16, or 512K x 8
- Access Times:  
20\*, 25, 30, 35, 45ns
- Fully Static Operation  
- No clock or refresh required
- Low Power Dissipation:  
8.0mW (typ.) Full Standby  
0.8W (typ.) Operating (x8)
- Single +5V Power Supply,  
±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Current:  
140µA typ. (2.0V)
- 66-Pin PGA "VERSA-STACK"  
Package

\* Commercial only.

PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O31	Data Input/Output
CE0 - CE3	Low Chip Enables
SEL	High Chip Enable
WE0 - WE1	Write Enables
OE	Output Enable
VDD	Power (+5V)
Vss	Ground
N.C.	No Connect



**PIN-OUT DIAGRAM**

1/016 1	N.C.	12	1/023 23	11	10	23	34	1/024	45	VDD	56	1/031
1/017 2	CE2	13	1/022 24	○	○	○	35	1/025	46	CE3	57	1/030
1/018 3	VSS	14	1/021 25	○	○	○	36	1/026	47	N.C.	58	1/029
A13 4	1/019	15	1/020 26	○	○	○	37	A6	48	1/027	59	1/028
A14 5	A10	16	OE 27	○	○	○	38	A7	49	A3	60	A0
A15 6	A11	17	N.C.	28	○	○	39	N.C.	50	A4	61	A1
A16 7	A12	18	WE0 29	○	○	○	40	A8	51	A5	62	A2
N.C.	8	VDD	1/07 30	○	○	○	41	A9	52	WE1	63	1/015
1/00 9	CE0	20	1/06 31	○	○	○	42	1/08	53	CE1	64	1/014
1/01 10	SEL	21	1/05 32	○	○	○	43	1/09	54	VSS	65	1/013
1/02 11	1/03	22	1/04 33	11	10	23	44	1/010	55	1/011	66	1/012

TOP VIEW

**NOTE:** SEL applies to the DPS128X32CV3 only, No Connect for the DPS128X32BV3 version.

RECOMMENDED OPERATING RANGE <sup>3</sup>						
Symbol	Characteristic	Min.	Typ.	Max.	Unit	
V <sub>DD</sub>	Supply Voltage	4.5	5.0	5.5	V	
V <sub>IH</sub>	Input HIGH Voltage	2.2		V <sub>DD</sub> +0.3	V	
V <sub>IL</sub>	Input LOW Voltage	-0.5 <sup>2</sup>		0.8	V	
T <sub>A</sub>	Operating Temperature	M	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

TRUTH TABLE						
Mode	SEL	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	L	X	X	X	High-Z	Standby
Not Selected	X	H	X	X	High-Z	Standby
DOUT Disable	H	L	H	H	High-Z	Active
Read	H	L	H	L	DOUT	Active
Write	H	L	L	X	DIN	Active

H = HIGH L = LOW X = Don't Care  
 NOTE: SEL applies to DPS128X32CV3 version only.

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V <sub>OH</sub>	HIGH Voltage	I <sub>OH</sub> = -4.0mA	2.4		V
V <sub>OL</sub>	LOW Voltage	I <sub>OL</sub> = 8.0mA		0.4	V

CAPACITANCE <sup>4</sup> : T <sub>A</sub> = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C <sub>ADR</sub>	Address Input	50	pF	V <sub>IN</sub> <sup>2</sup> = 0V
C <sub>C<math>\overline{CE}</math></sub>	Chip Enable	20		
C <sub>SEL</sub>	Active High Chip Select	50		
C <sub>WE</sub>	Write Enable	25		
C <sub>OE</sub>	Output Enable	50		
C <sub>I/O</sub>	Data Input/Output	20		

NOTE: C<sub>SEL</sub> applies to DPS128X32CV3 version only.

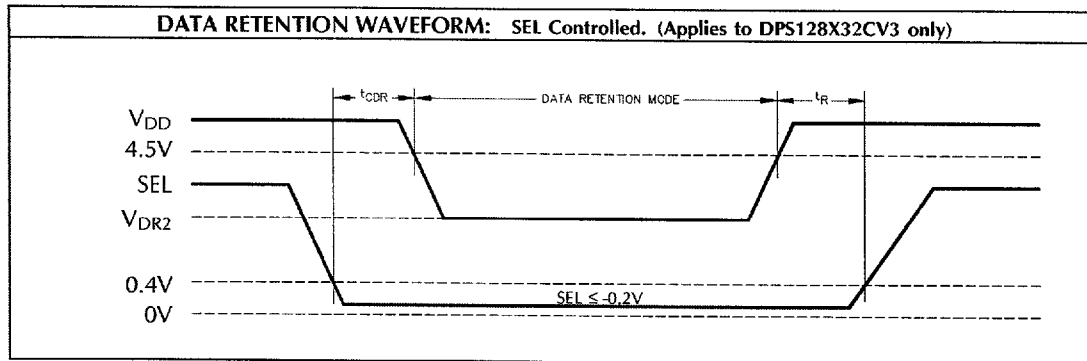
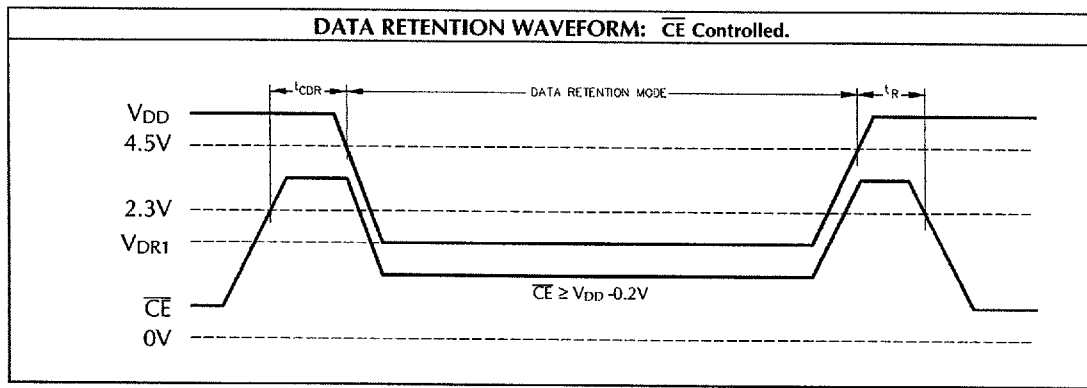
ABSOLUTE MAXIMUM RATINGS <sup>3</sup>			
Symbol	Parameter	Value	Unit
T <sub>STC</sub>	Storage Temperature	-65 to +150	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
V <sub>DD</sub>	Supply Voltage <sup>1</sup>	-0.5 to +7.0	°C
V <sub>I/O</sub>	Input/Output Voltage <sup>1</sup>	-0.5 to V <sub>DD</sub> +0.5	V

DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions	Typ. (†)	C		I		M		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 0V to V <sub>DD</sub>	-	-20	+20	-20	+20	-20	+20	µA	
I <sub>OUT</sub>	Output Leakage Current	V <sub>I/O</sub> = 0V to V <sub>DD</sub> , CE or OE = V <sub>IH</sub> , or WE = V <sub>IL</sub>	-	-10	+10	-10	+10	-10	+10	µA	
I <sub>CC</sub>	Operating Supply Current	Cycle = min., Duty = 100% I <sub>OUT</sub> = 0mA	X8	175		230		245		265	mA
			X16	250		340		350		390	
			X32	400		560		560		640	
I <sub>SB1</sub>	Full Standby Supply Current	V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ V <sub>SS</sub> +0.2V	1.6		20		20		40	mA	
I <sub>SB2</sub>	Standby Current (TTL)	CE = V <sub>IH</sub>	100		120		140		140	mA	
I <sub>DR3</sub>	Data Retention Supply Current (3V)	V <sub>DR</sub> = 3V, CE ≥ V <sub>DR</sub> -0.2V, (or SEL ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ +0.2V)	0.28		1.60		2.40		8.00	mA	
I <sub>DR2</sub>	Data Retention Supply Current (2V)	V <sub>DR</sub> = 2V, CE ≥ V <sub>DR</sub> -0.2V, (or SEL ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>DD</sub> -0.2V or V <sub>IN</sub> ≤ +0.2V)	0.14		1.00		1.60		7.20	mA	
V <sub>OL</sub>	Output Low Voltage	I <sub>OUT</sub> = 8.0mA	-		0.4		0.4		0.4	V	
V <sub>OH</sub>	Output High Voltage	I <sub>OUT</sub> = -4.0mA	-		2.4		2.4		2.4	V	

† Typical measurements made at +25°C, Cycle = min., V<sub>DD</sub> = 5.0V.

Data Retention AC Characteristics <sup>8</sup>						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	V <sub>DD</sub> for Data Retention	$\overline{CE} \geq V_{DR} - 0.2V$ , ( $SEL \geq V_{DR} - 0.2V$ , or $V_{IN} \leq V_{DR} - 0.2V$ or $V_{IN} \leq 0.2V$ )	2.0	-	-	V
V <sub>CDR</sub>	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t <sub>r</sub>	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

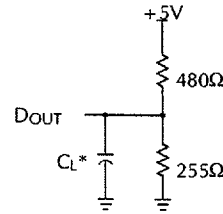
NOTE: Test Conditions in parenthesis apply to DPS128X32CV3 version only.



OUTPUT LOAD		
Load	C <sub>L</sub>	Parameters Measured
1	30pF	except t <sub>LZ1</sub> , t <sub>LZ2</sub> , t <sub>HZ1</sub> , t <sub>HZ2</sub> , t <sub>OHZ</sub> , t <sub>OLZ</sub> , and t <sub>WHZ</sub>
2	5pF	t <sub>LZ1</sub> , t <sub>LZ2</sub> , t <sub>HZ1</sub> , t <sub>HZ2</sub> , t <sub>OHZ</sub> , t <sub>OLZ</sub> , and t <sub>WHZ</sub>

NOTE: t<sub>LZ2</sub> and t<sub>HZ2</sub> apply to DPS128X32CV3 version only.

Figure 1. Output Load  
\* Including Probe and Jig Capacitance.



AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t <sub>RC</sub>	Read Cycle Time	20		25		30		35		45		ns
2	t <sub>AA</sub>	Address Access Time		20		25		30		35		45	ns
3	t <sub>CO1</sub>	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t <sub>CO2</sub>	SEL to Output Valid		20		25		30		35		45	ns
5	t <sub>OE</sub>	Output Enable to Output Valid		8		10		15		20		25	ns
6	t <sub>LZ1</sub>	$\overline{CE}$ to Output in LOW-Z <sup>4,5</sup>	3		3		3		3		3		ns
7	t <sub>LZ2</sub>	SEL to Output in LOW-Z <sup>4,5</sup>	3		3		3		3		3		ns
8	t <sub>OLZ</sub>	Output Enable to Output in LOW-Z <sup>4,5</sup>	0		0		0		0		0		ns
9	t <sub>HZ1</sub>	$\overline{CE}$ to Output in HIGH-Z <sup>4,5</sup>		10		12		15		20		25	ns
10	t <sub>HZ2</sub>	SEL to Output in HIGH-Z <sup>4,5</sup>		10		12		15		20		25	ns
11	t <sub>OHZ</sub>	Output Enable to Output in HIGH-Z <sup>4,5</sup>		8		10		15		20		25	ns
12	t <sub>OH</sub>	Output Hold from Address Change	3		3		3		3		3		ns

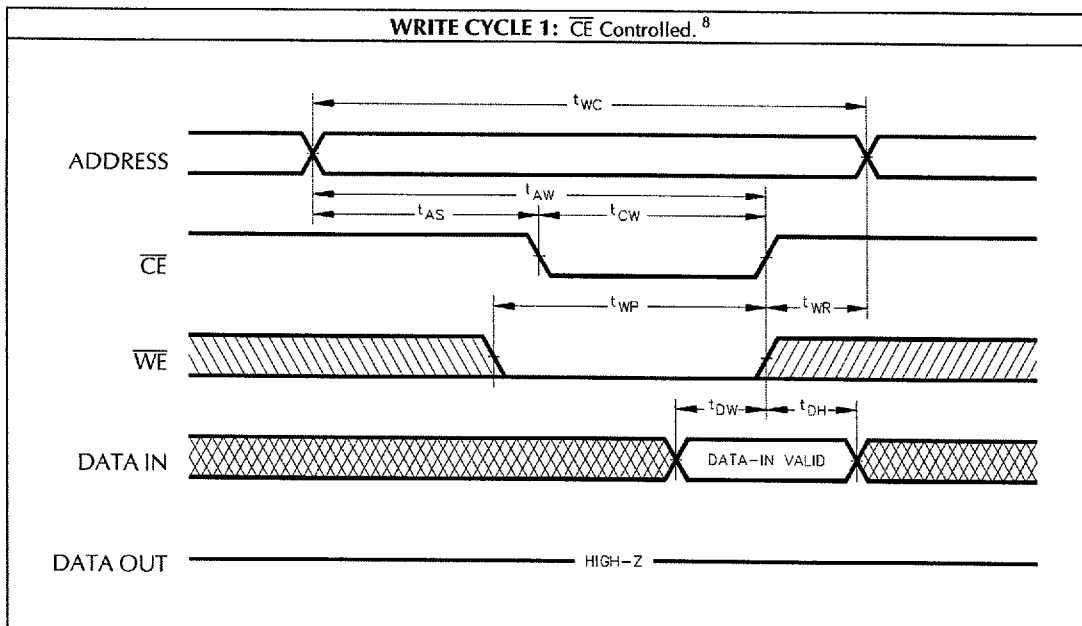
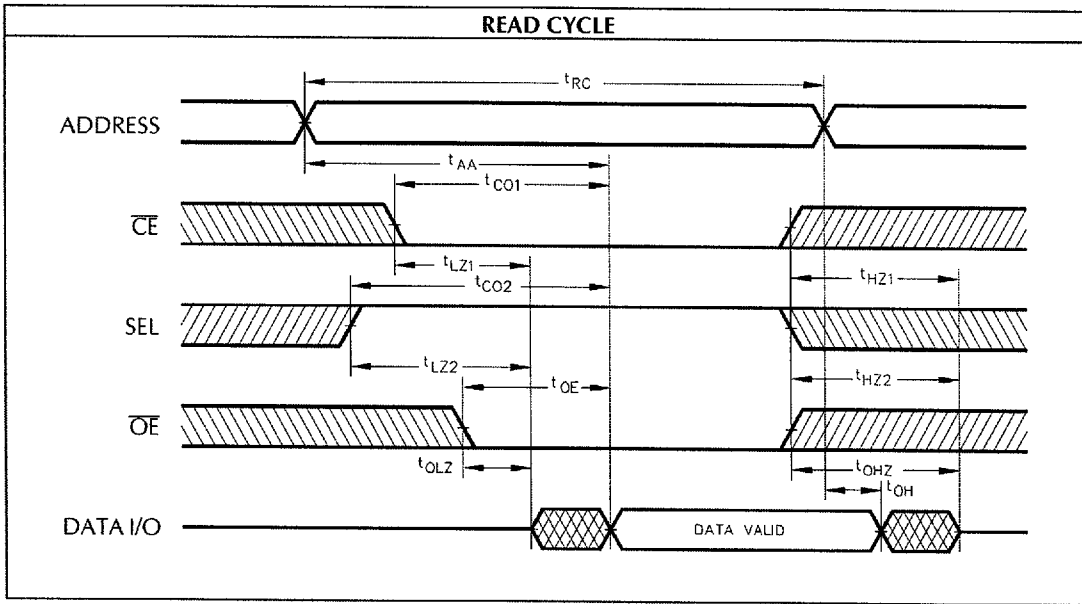
\* Available in Commercial Only.

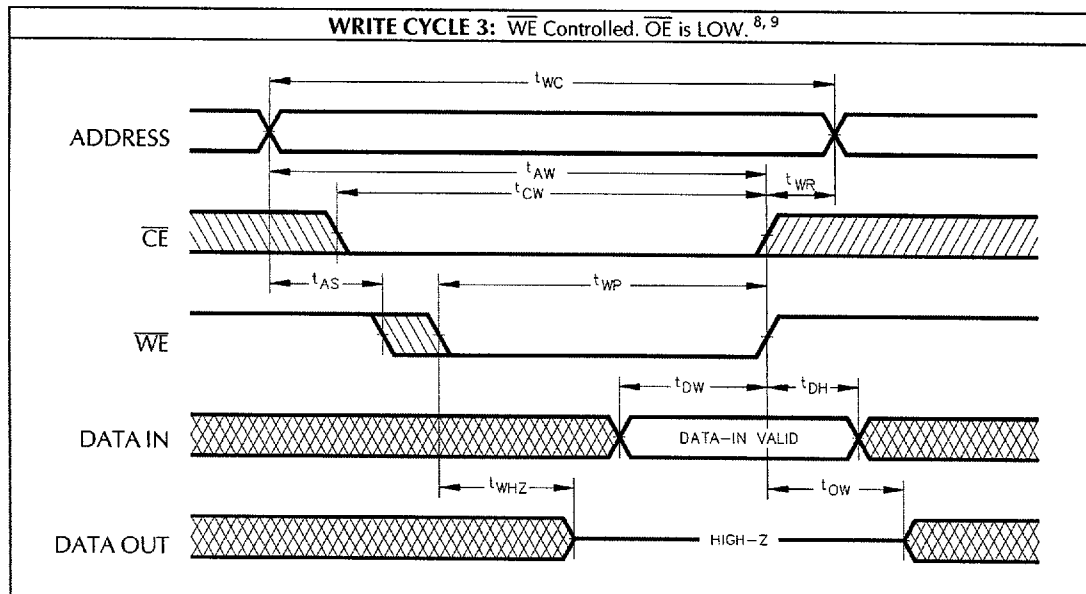
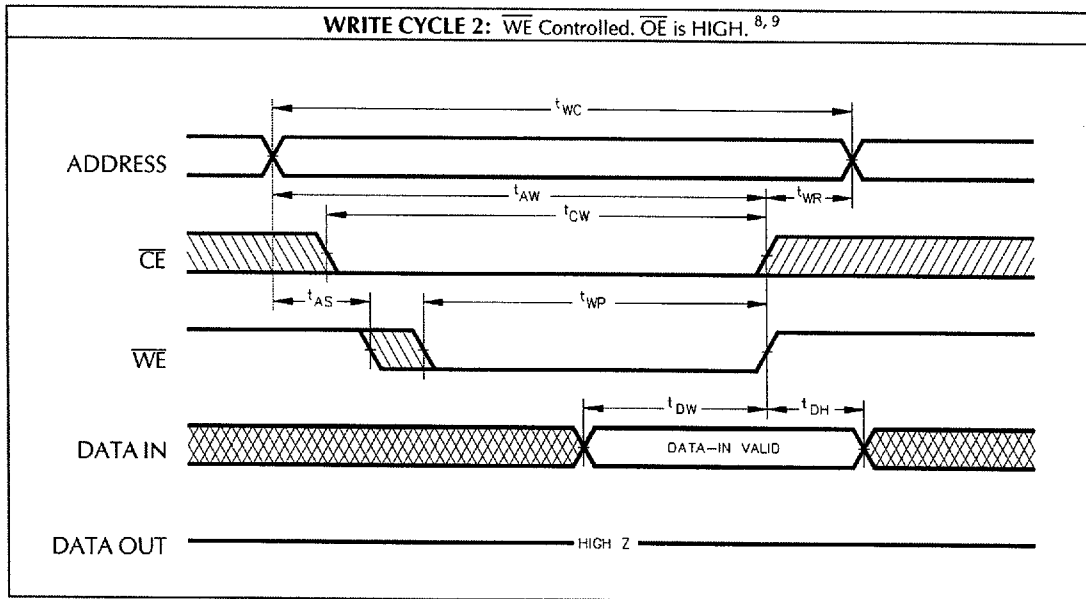
NOTE: t<sub>CO2</sub>, t<sub>LZ2</sub> and t<sub>HZ2</sub> apply to DPS128X32CV3 version only.

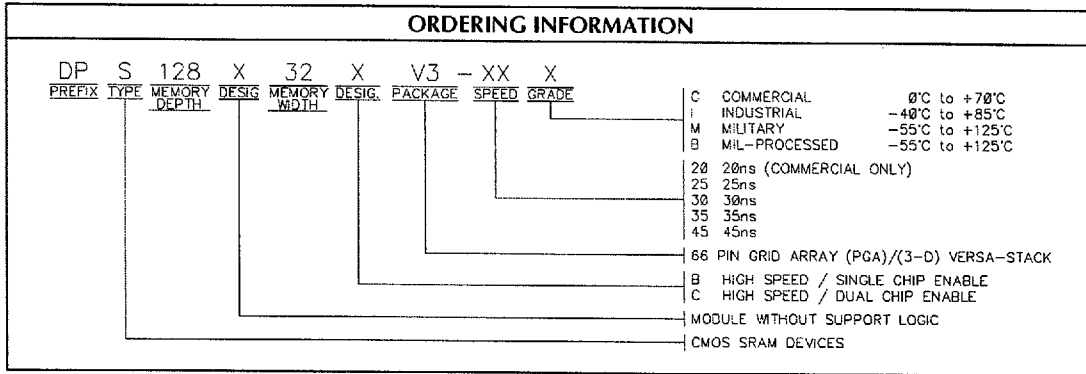
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE <sup>6,7</sup> : Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t <sub>WC</sub>	Write Cycle Time	20		25		30		35		45		ns
14	t <sub>AW</sub>	Address Valid to End of Write	15		20		25		30		40		ns
15	t <sub>CW</sub>	Chip Enable to End of Write	15		20		25		30		40		ns
16	t <sub>AS</sub>	Address Set-Up Time **	0		0		0		0		0		ns
17	t <sub>WP</sub>	Write Pulse Width	15		20		25		30		35		ns
18	t <sub>WR</sub>	Write Recovery Time	0		0		0		0		0		ns
19	t <sub>WHZ</sub>	Write Enable to Output in HIGH-Z <sup>4,5</sup>		8		10		12		15		20	ns
20	t <sub>DW</sub>	Data to Write Time Overlap	12		15		15		20		25		ns
21	t <sub>DH</sub>	Data Hold from Write Time	0		0		0		0		0		ns
22	t <sub>OW</sub>	Output Active from End of Write	3		3		3		3		3		ns

\* Available in Commercial Only.

\*\* Valid for both Read and Write Cycles.

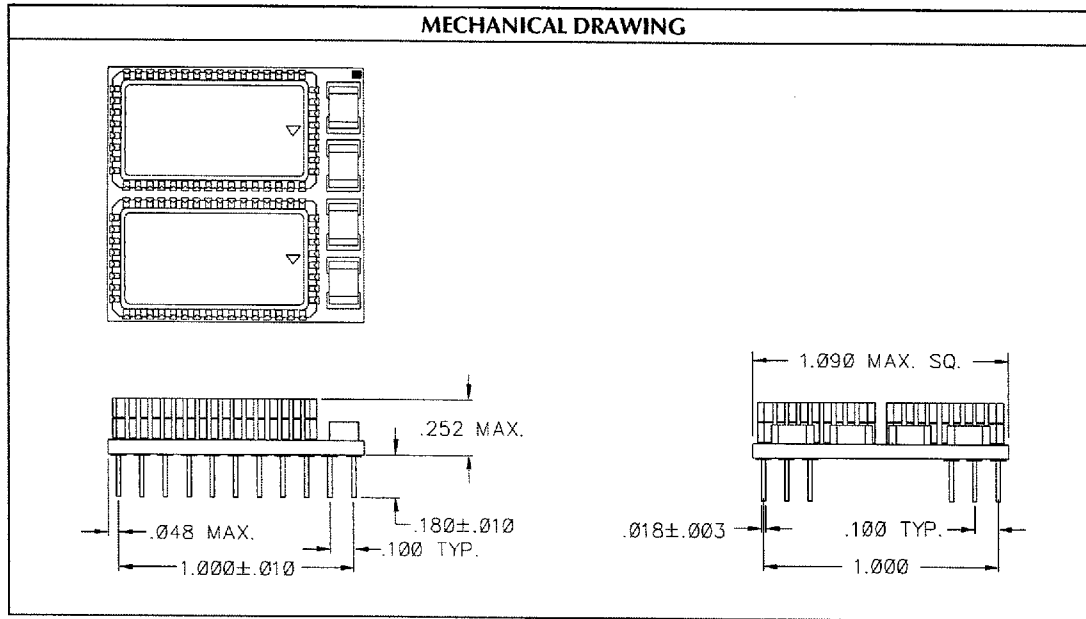






**NOTES:**

- All voltages are with respect to  $V_{SS}$ .
- 2.0V min. for pulse width less than 20ns ( $V_{IL}$  min. = -0.5V at DC level).
- Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This parameter is guaranteed and not 100% tested.
- Transition is measured at the point of  $\pm 500$ mV from steady state voltage.
- When  $\overline{OE}$  and  $\overline{CE}$  are LOW and  $\overline{WE}$  is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
- The outputs are in a high impedance state when  $\overline{WE}$  is LOW.
- SEL timing is the same as  $\overline{CE}$  timing (Valid for DPS128X32CV3 only). The Waveform is inverted.
- $\overline{CE}$  and  $\overline{WE}$  can initiate and terminate WRITE Cycle.



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