



SANYO Semiconductors

DATA SHEET

ECH8505

— PNP Epitaxial Planar Silicon Transistor

Motor Drive Applications

Features

- Composite type, facilitating high-density mounting.
- Mounting height 0.9mm.
- Halogen free compliance.

Specifications

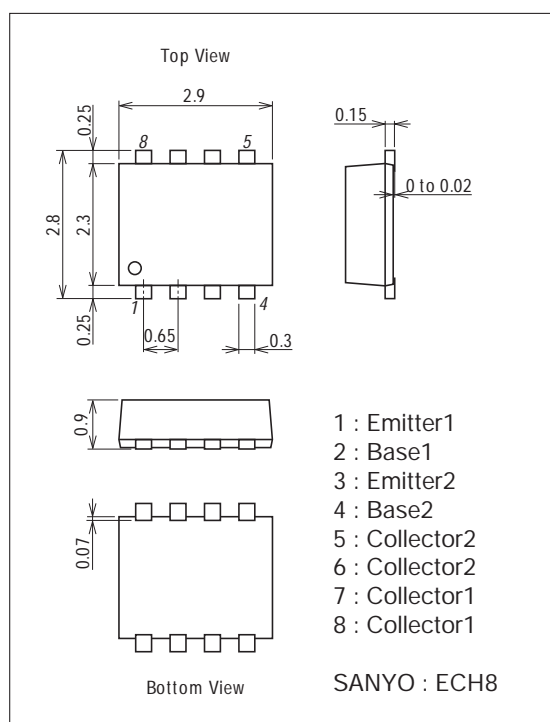
Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V _{CBO}		-180	V
Collector-to-Emitter Voltage	V _{CEO}		-160	V
Emitter-to-Base Voltage	V _{EBO}		-7	V
Collector Current	I _C		-1.5	A
Collector Current (Pulse)	I _{CP}		-3	A
Base Current	I _B		-300	mA
Collector Dissipation	P _C	When mounted on ceramic substrate (900mm ² ×0.8mm) 1unit	1.3	W
Total Dissipation	P _T	When mounted on ceramic substrate (900mm ² ×0.8mm)	1.6	W
Junction Temperature	T _J		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Package Dimensions

unit : mm (typ)

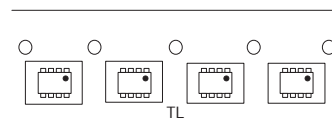
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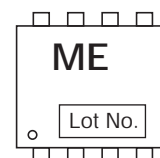
Product & Package Information

- Package : ECH8
- JEITA, JEDEC : -
- Minimum Packing Quantity : 3,000 pcs./reel

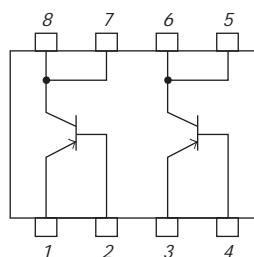
Taping Type : TL



Marking



Electrical Connection

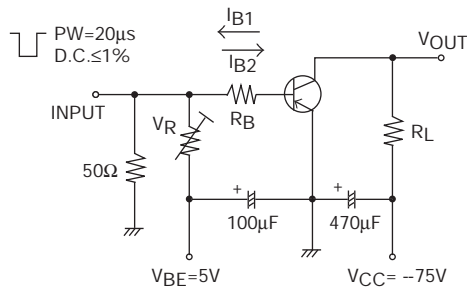


Electrical Characteristics at Ta=25°C

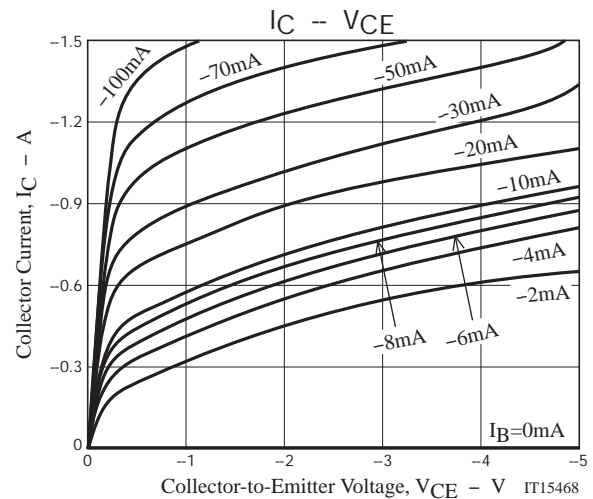
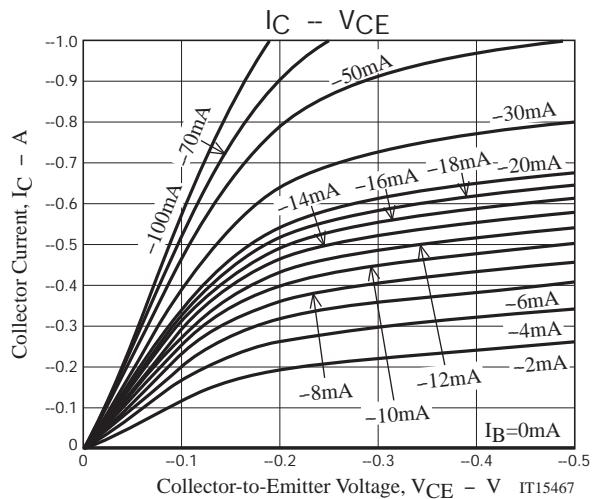
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB} = -80V, I_E = 0A$			-1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -4V, I_C = 0A$			-1	μA
DC Current Gain	h_{FE}	$V_{CE} = -5V, I_C = -100mA$	200		560	
Gain-Bandwidth Product	f_T	$V_{CE} = -10V, I_C = -100mA$		85		MHz
Output Capacitance	C_{ob}	$V_{CB} = -10V, f = 1MHz$		21		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -500mA, I_B = -50mA$		-90	-160	mV
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -500mA, I_B = -50mA$		-0.9	-1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -10\mu A, I_E = 0A$	-180			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -1mA, R_{BE} = \infty$	-160			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -10\mu A, I_C = 0A$	-7			V
Turn-On Time	t_{on}	See specified Test Circuit.		25		ns
Storage Time	t_{stg}	See specified Test Circuit.		970		ns
Fall Time	t_f	See specified Test Circuit.		30		ns

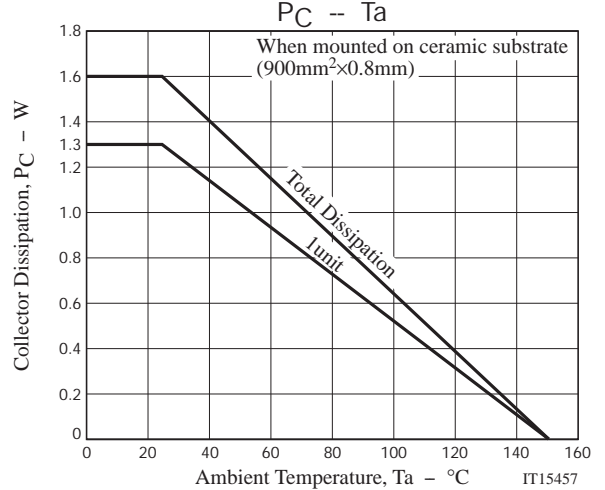
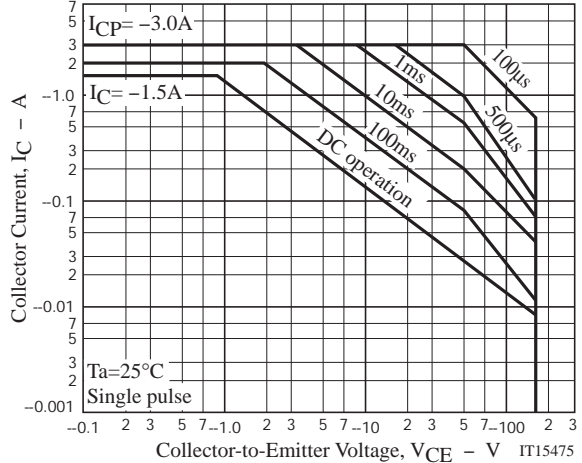
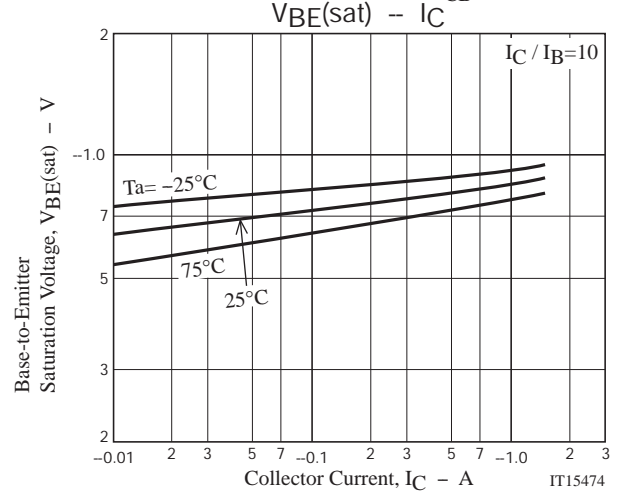
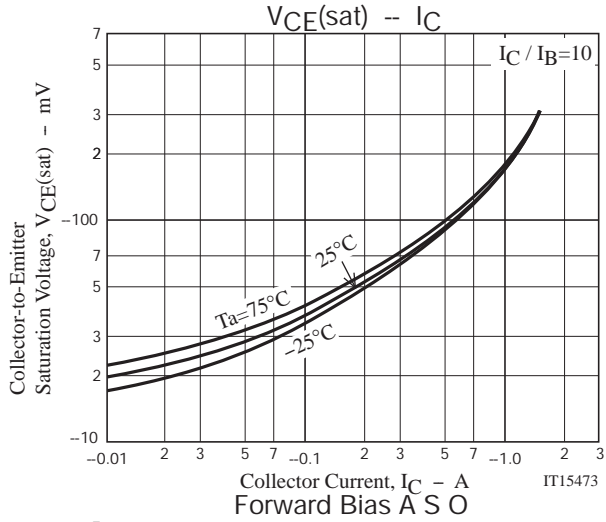
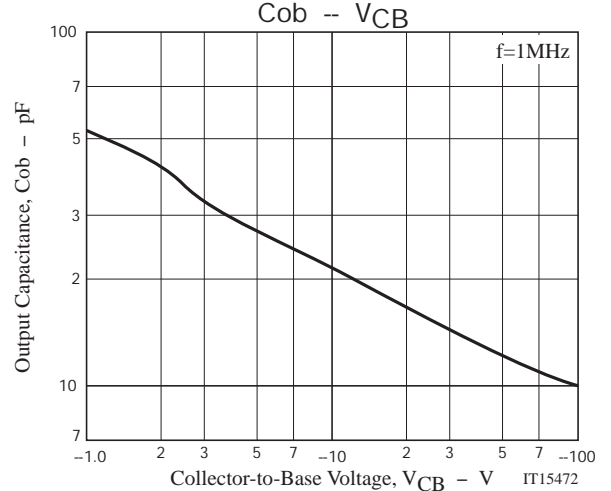
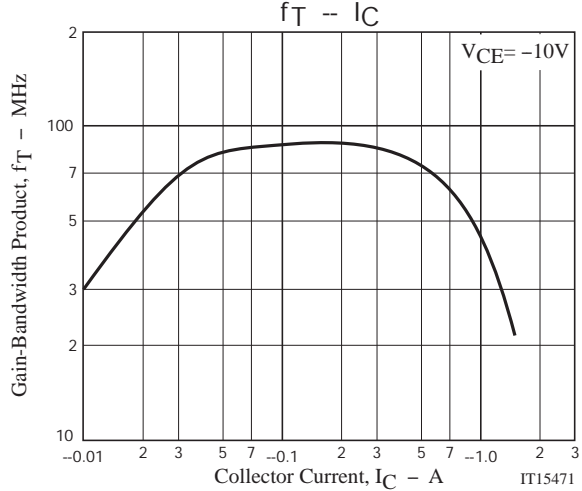
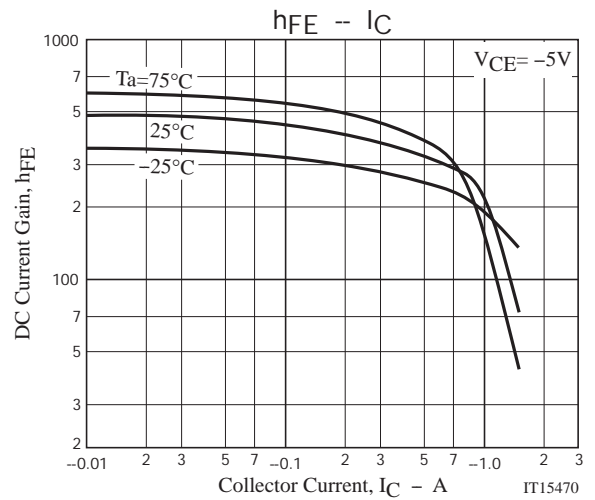
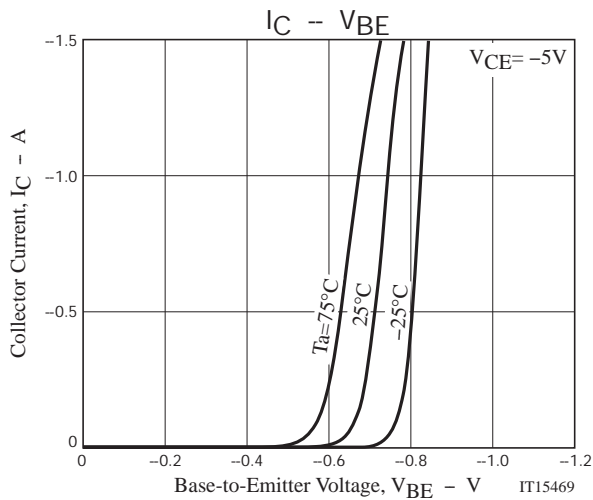
Note) The specifications shown above are for each individual transistor.

Switching Time Test Circuit



$$I_C = -10I_{B1} = 10I_{B2} = -0.7A$$





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