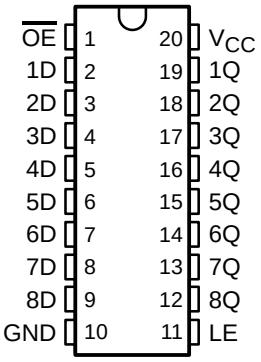
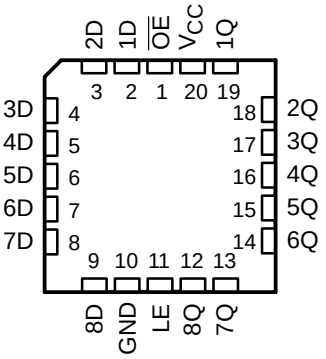
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVTH573 . . . J OR W PACKAGE
SN74LVTH573 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVTH573 . . . FK PACKAGE
(TOP VIEW)



description

These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the 'LVTH573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

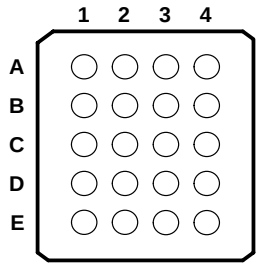
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

GQN PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1D	$\overline{OE}$	V_{CC}	1Q
B	3D	3Q	2D	2Q
C	5D	4D	5Q	4Q
D	7D	7Q	6D	6Q
E	GND	8D	LE	8Q

ORDERING INFORMATION

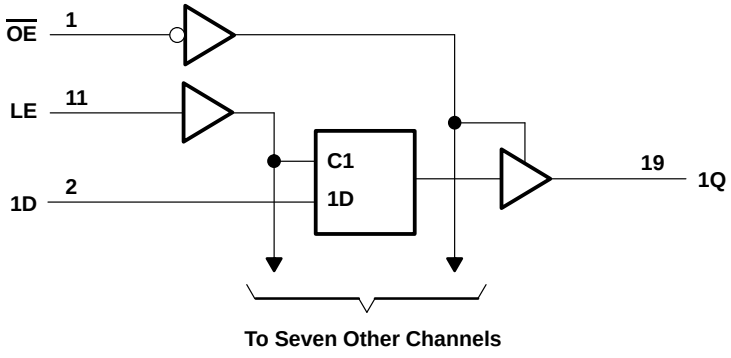
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube	SN74LVTH573DW	LVTH573
		Tape and reel	SN74LVTH573DWR	
	SSOP – DB	Tape and reel	SN74LVTH573DBR	LXH573
	TSSOP – PW	Tape and reel	SN74LVTH573PWR	LXH573
	VFBGA – GQN	Tape and reel	SN74LVTH573GQNR	LXH573
–55°C to 125°C	CDIP – J	Tube	SNJ54LVTH573J	SNJ54LVTH573J
	CFP – W	Tube	SNJ54LVTH573W	SNJ54LVTH573W
	LCCC – FK	Tube	SNJ54LVTH573FK	SNJ54LVTH573FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O: SN54LVTH573 . . . . . 96 mA
SN74LVTH573 . . . . . 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVTH573 . . . . . 48 mA
SN74LVTH573 . . . . . 64 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . . 70°C/W
DW package . . . . . 58°C/W
GQN package . . . . . 76°C/W
PW package . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH573		SN74LVTH573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			–24		–32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH573			SN74LVTH573			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 µA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 µA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	µA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	µA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			µA
			V_I = 2 V	–75			–75			
		V_{CC} = 3.6 V‡,	V_I = 0 to 3.6 V						±500	
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5			5	µA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			–5			–5	µA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100*			±100	µA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}§		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			3			3		pF
C_o		V_O = 3 V or 0			7			7		pF

*On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

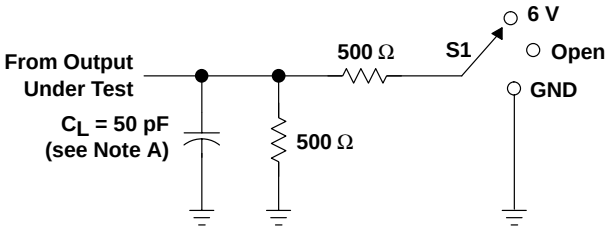
		SN54LVTH573				SN74LVTH573				UNIT
		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		3		3		3		ns
t_{su}	Setup time, data before LE↓	0.7		0.6		0.7		0.6		ns
t_h	Hold time, data after LE↓	1.5		1.7		1.5		1.7		ns

switching characteristics over recommended free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH573				SN74LVTH573					UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	D	Q	1.4	4.1		4.7	1.5	2.6	3.9		4.5	ns
t_{PHL}			1.4	4.5		4.8	1.5	2.9	3.9		4.5	
t_{PLH}	LE	Q	1	4.4		5.4	1.9	2.9	4.2		4.9	ns
t_{PHL}			1.4	4.4		5.1	1.9	2.9	4.2		4.9	
t_{PZH}	$\overline{OE}$	Q	1.4	5.2		6.2	1.5	3.2	5.1		5.9	ns
t_{PZL}			1.4	5.2		6.2	1.5	3.9	5.1		5.9	
t_{PHZ}	$\overline{OE}$	Q	1.2	5.4		5.7	2	3.5	4.9		5.5	ns
t_{PLZ}			1	5.2		5.2	2	3.2	4.6		4.9	

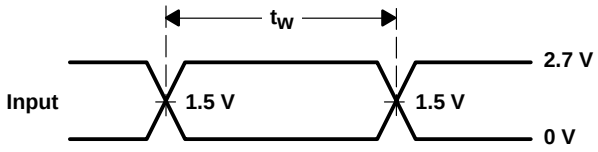
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

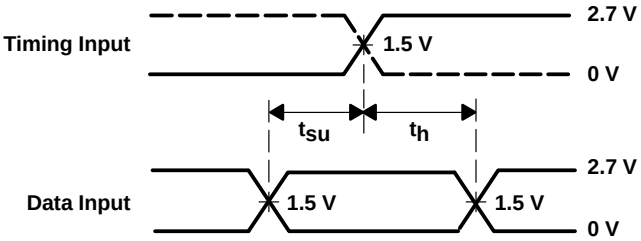


LOAD CIRCUIT

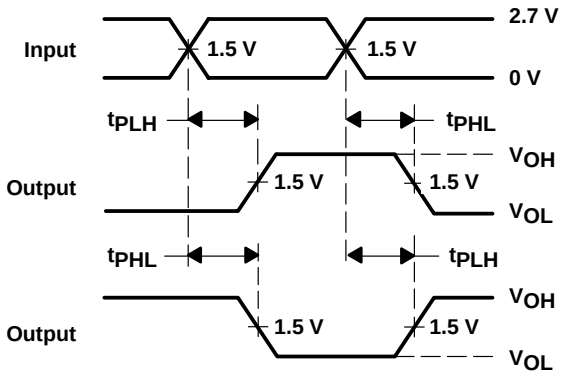
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



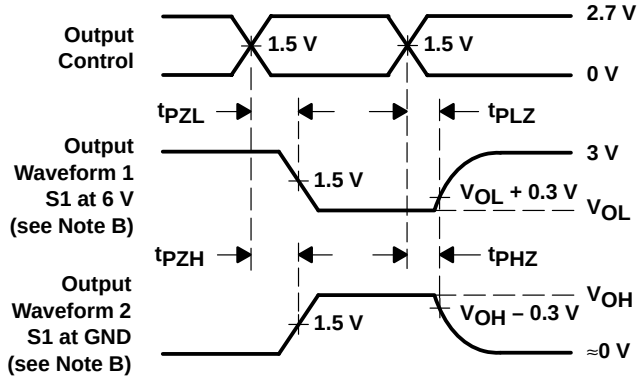
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

SN74LVTH573, 3.3-V ABT Octal Transparent D-Type Latches With 3-State Outputs

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54LVTH573	SN74LVTH573
Voltage Nodes (V)	3.3, 2.7	3.3, 2.7
Vcc range (V)	2.7 to 3.6	
Output Drive (mA)	-24/48	
Static Current	5 mA	
th (ns)	1.5	
tpd max (ns)	4.5	
tsu (ns)	0.7	

FEATURES

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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce)
  <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I off and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

DESCRIPTION

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These octal latches are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The eight latches of the ’LVTH573 devices are transparent D-type latches. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (OE\) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, OE\ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

Back to Top

Full datasheet in Acrobat PDF: sn74lvth573.pdf (102 KB,Rev.F) (Updated: 07/26/2001)

APPLICATION NOTES

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View Application Notes for Digital Logic

- 16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA (Rev. B) (SZZA029B - Updated: 05/22/2002)
- Bus-Interface Devices With Output-Damping Resistors Or Reduced-Drive Outputs (Rev. A) (SCBA012A - Updated: 08/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)
- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- LVT Family Characteristics (Rev. A) (SCEA002A - Updated: 03/01/1998)
- LVT-to-LVTH Conversion (SCEA010 - Updated: 12/08/1998)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- Low Voltage Logic Families (Rev. A) (SCVAE01A - Updated: 06/01/1998)
- Power-Up 3-State (PU3S) Circuits in TI Standard Logic Devices (SZZA033 - Updated: 05/10/2002)
- Quad Flatpack No-Lead Logic Packages (Rev. A) (SCBA017A - Updated: 09/10/2002)
- Understanding Advanced Bus-Interface Products Design Guide (SCAA029, 253 KB - Updated: 05/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Advanced Bus Interface Logic Selection Guide (SCYT126, 453 KB - Updated: 01/09/2001)
- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Low Voltage Solutions (SGYN139, 103 KB - Updated: 04/04/2001)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74LVTH573DBR	SSOP (DB)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74LVTH573DW	SOP (DW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74LVTH573GQNR	VFBGA (GQN)	20		ACTIVE	View Product Content	Request Samples
SN74LVTH573NSR	SOP (NS)	20		ACTIVE	View Product Content	Request Samples
SN74LVTH573PWR	TSSOP (PW)	20	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74LVTH573DBLE	OBSOLETE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74LVTH573DBR	ACTIVE	SSOP (DB) | 20	-40 TO 85	View Contents	1KU | 0.43	2000	N/A*	156 | 30 Sep	4 WKS			
								2000 | 03 Oct				
								>10k | 14 Oct				
SN74LVTH573DW	ACTIVE	SOP (DW) | 20	-40 TO 85	View Contents	1KU | 0.43	25	N/A*	9675 | 19 Sep	4 WKS	DigiKey | AMERICA	865	BUY NOW
								>10k | 11 Oct		Avnet | AMERICA	700	BUY NOW
								>10k | 18 Oct				
SN74LVTH573DWR	ACTIVE	SOP (DW) | 20	-40 TO 85	View Contents	1KU | 0.43	2000	N/A*	1821 | 20 Sep	4 WKS			
								>10k | 11 Oct				
								>10k | 18 Oct				
SN74LVTH573GQNR	ACTIVE	VFBGA (GQN) | 20		View Contents	1KU | 0.48	1000	2000		4 WKS	Avnet | AMERICA	1k	BUY NOW
SN74LVTH573NSR	ACTIVE	SOP (NS) | 20		View Contents	1KU | 0.63	2000	N/A*	480 | 23 Sep	4 WKS			
								>10k | 14 Oct				
								>10k | 21 Oct				
SN74LVTH573PWLE	OBSOLETE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74LVTH573PWR	ACTIVE	TSSOP (PW) | 20	-40 TO 85	View Contents	1KU | 0.43	2000	N/A*	>10k | 10 Oct	4 WKS			

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