

MICRON**256K x 18, 128K x 32/36
3.3V I/O, PIPELINED, SCD SYNCBURST SRAM**

SYNCBURST SRAM

MT58LC256K18D9, MT58LC128K32D9,
MT58LC128K36D9**3.3V Supply, Pipelined, Burst Counter and
Single-Cycle Deselect**

FEATURES

- Fast access times: 3.5ns, 3.8ns, 4.2ns, 4.5ns and 6ns
- Fast OE# access times: 3.5ns, 3.8ns, 4.2ns, 4.5ns and 5ns
- Single +3.3V +0.3V/-0.165V power supply (V_{DD})
- Separate +3.3V +0.3V/-0.165V isolated output buffer supply (V_{DDQ})
- SNOOZE MODE for reduced power standby
- Single-cycle deselect (Pentium® BSRAM compatible)
- Common data inputs and data outputs
- Individual BYTE WRITE control and GLOBAL WRITE
- Three chip enables for simple depth expansion and address pipelining
- Clock-controlled and registered addresses, data I/Os and control signals
- Internally self-timed WRITE cycle
- Burst control pin (interleaved or linear burst)
- Automatic power-down for portable applications
- 100-lead TQFP package for high density, high speed
- 119-bump BGA package
- Low capacitive bus loading
- x18, x32 and x36 versions available

OPTIONS

- Clock Cycle Timing
 - 6ns/166 MHz
 - 6.6ns/150 MHz
 - 7.5ns/133 MHz
 - 8.5ns/117 MHz
 - 11ns/90 MHz
- Configurations
 - 256K x 18
 - 128K x 32
 - 128K x 36
- Packages
 - 100-pin TQFP
 - 119-bump, 14mm x 22mm BGA
- Part Number Example: MT58LC256K18D9LG-11

MARKING

-6
-6.6
-7.5
-8.5
-11

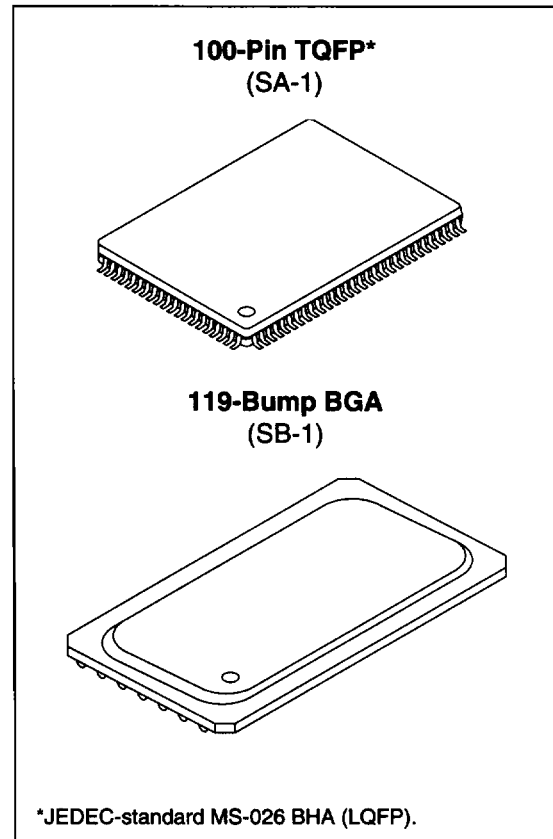
MT58LC256K18D9
MT58LC128K32D9
MT58LC128K36D9

LG
BG

GENERAL DESCRIPTION

The Micron SyncBurst SRAM family employs high-speed, low-power CMOS designs that are fabricated using an advanced CMOS process.

The MT58LC256K18D9 and MT58LC128K32/36D9 SRAMs integrate a 256K x 18, 128K x 32 or 128K x 36 SRAM



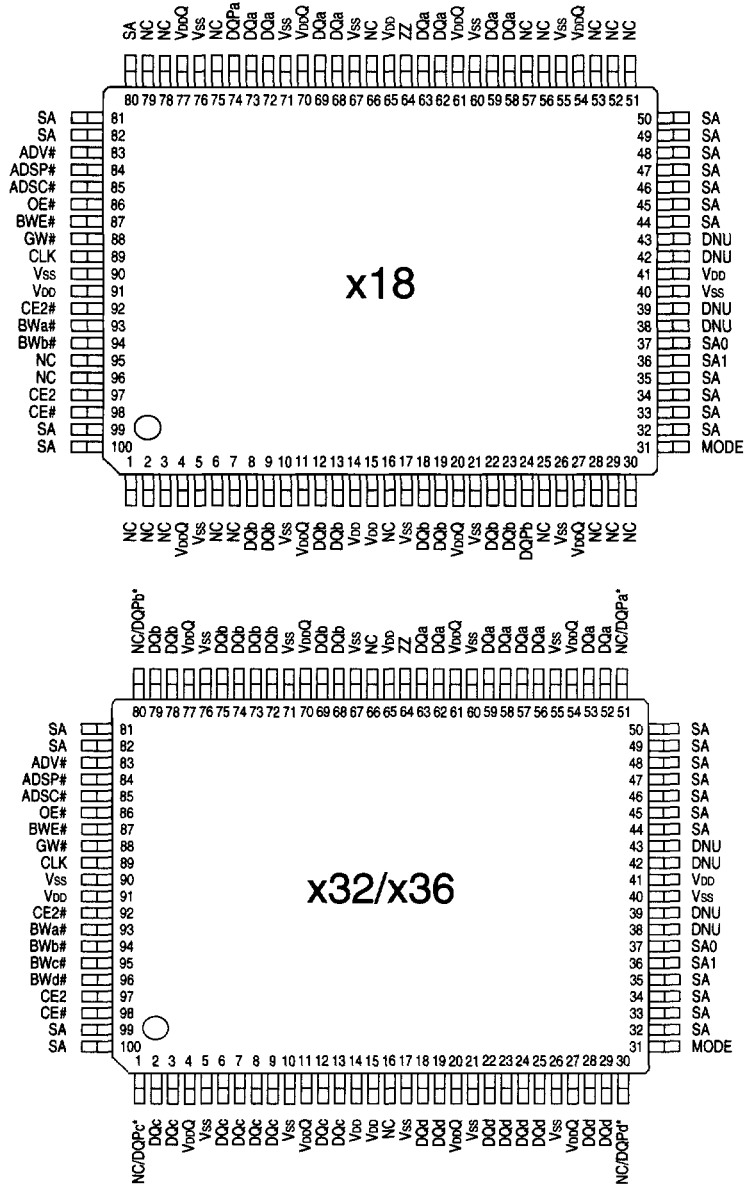
core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable (CE#), two additional chip enables for easy depth expansion (CE2, CE2#), burst control inputs (ADSC#, ADSP#, ADV#), byte write enables (BWx#) and global write (GW#).

Asynchronous inputs include the output enable (OE#), clock (CLK) and snooze enable (ZZ). There is also a burst mode pin (MODE) that selects between interleaved and linear burst modes. The data-out (Q), enabled by OE#, is also asynchronous. WRITE cycles can be from one to two

SYNCBURST SRAM

PIN ASSIGNMENT (Top View)
100-Pin TQFP
(SA-1)

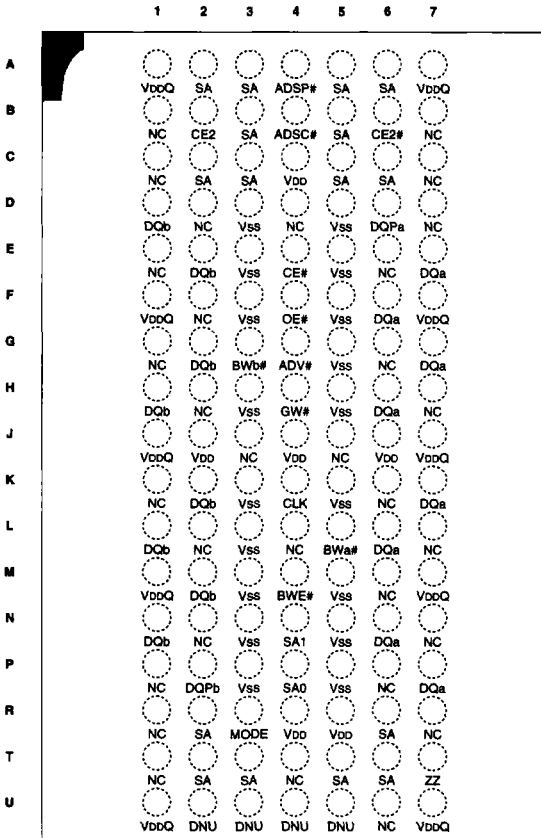
SYNCBURST SRAM



* No Connect (NC) is used in the x32 version. Parity (DQPx) is used in the x36 version.

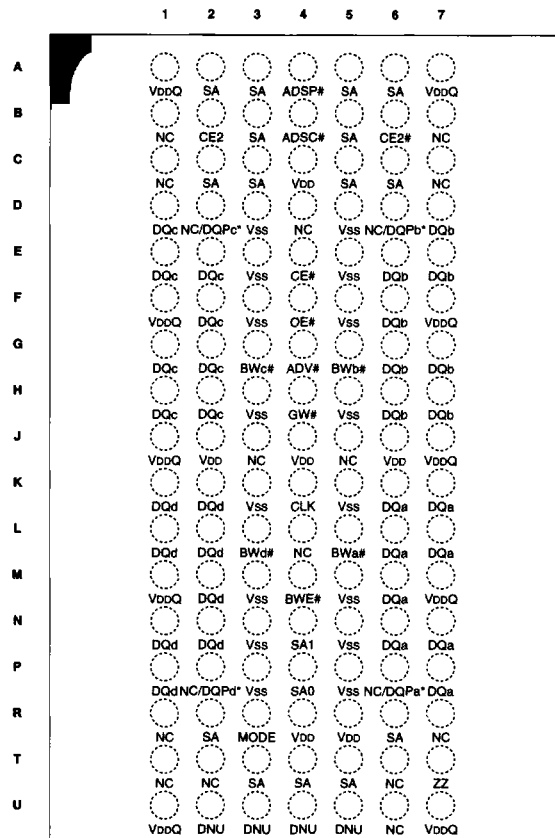
PIN ASSIGNMENT (Top View)
119-Bump BGA

x18



TOP VIEW

x32/x36



TOP VIEW

SYNCBURST SRAM

* No Connect (NC) is used in the x32 version. Parity (DQPx) is used in the x36 version.

MICRON

256K x 18, 128K x 32/36
3.3V I/O, PIPELINED, SCD SYNCBURST SRAM**GENERAL DESCRIPTION (continued)**

bytes wide (x18) or from one to four bytes wide (x32/x36) as controlled by the write control inputs.

Burst operation can be initiated with either address status processor (ADSP#) or address status controller (ADSC#) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin (ADV#).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x18 device, BWA# controls DQa pins and DQP_a; BWB# controls DQb pins and DQP_b. During WRITE cycles on the x32 and x36 devices, BWA# controls DQa pins and DQP_a; BWB# controls DQb pins and DQP_b; BWC# controls DQc pins and DQP_c; BWD# controls DQd pins and DQP_d. GW# LOW causes all bytes to be written. Parity bits are only available on the x18 and x36 versions.

SYNCBURST SRAM

TQFP PIN ASSIGNMENT TABLE

PIN #	x18	x32/x36
1	NC	NC/DQPc*
2	NC	DQc
3	NC	DQc
4	V _{DDQ}	
5	V _{SS}	
6	NC	DQc
7	NC	DQc
8	DQb	DQc
9	DQb	DQc
10	V _{SS}	
11	V _{DDQ}	
12	DQb	DQc
13	DQb	DQc
14	V _{DD}	
15	V _{DD}	
16	NC	
17	V _{SS}	
18	DQb	DQd
19	DQb	DQd
20	V _{DDQ}	
21	V _{SS}	
22	DQb	DQd
23	DQb	DQd
24	DQPb	DQd
25	NC	DQd

PIN #	x18	x32/x36
26	V _{SS}	
27	V _{DDQ}	
28	NC	DQd
29	NC	DQd
30	NC	NC/DQPd*
31	MODE	
32	SA	
33	SA	
34	SA	
35	SA	
36	SA1	
37	SA0	
38	DNU	
39	DNU	
40	V _{SS}	
41	V _{DD}	
42	DNU	
43	DNU	
44	SA	
45	SA	
46	SA	
47	SA	
48	SA	
49	SA	
50	SA	

PIN #	x18	x32/x36
51	NC	NC/DQP _a *
52	NC	DQa
53	NC	DQa
54	V _{DDQ}	
55	V _{SS}	
56	NC	DQa
57	NC	DQa
58	DQa	
59	DQa	
60	V _{SS}	
61	V _{DDQ}	
62	DQa	
63	DQa	
64	ZZ	
65	V _{DD}	
66	NC	
67	V _{SS}	
68	DQa	DQb
69	DQa	DQb
70	V _{DDQ}	
71	V _{SS}	
72	DQa	DQb
73	DQa	DQb
74	DQP _a	DQb
75	NC	DQb

PIN #	x18	x32/x36
76	V _{SS}	
77	V _{DDQ}	
78	NC	DQb
79	NC	DQb
80	SA	NC/DQP _b *
81	SA	
82	SA	
83	ADV#	
84	ADSP#	
85	ADSC#	
86	OE#	
87	BWE#	
88	GW#	
89	CLK	
90	V _{SS}	
91	V _{DD}	
92	CE2#	
93	BWA#	
94	BWB#	
95	NC	BWC#
96	NC	BWD#
97	CE2	
98	CE#	
99	SA	
100	SA	

This device incorporates a single-cycle deselect feature during READ cycles. If the device is immediately deselected after a READ cycle, the output bus goes to a High-Z state 'KQHZ nanoseconds after the rising edge of clock.

The MT58LC256K18D9 and MT58LC128K32/36D9 operate from a +3.3V power supply, and all inputs and outputs are TTL-compatible. The device is ideally suited for Pentium and PowerPC™ pipelined systems and systems that benefit from a very wide, high-speed data bus. The device is also ideal in generic 16-, 18-, 32-, 36-, 64- and 72-bit wide applications.

Please refer to the Micron Web site (www.micron.com./mti/msp/html/sramprod.html) for the latest data sheet revisions.

* No Connect (NC) is used in the x32 version. Parity (DQP_x) is used in the x36 version.

**x18 BGA BUMP LAYOUT
(Top View)**

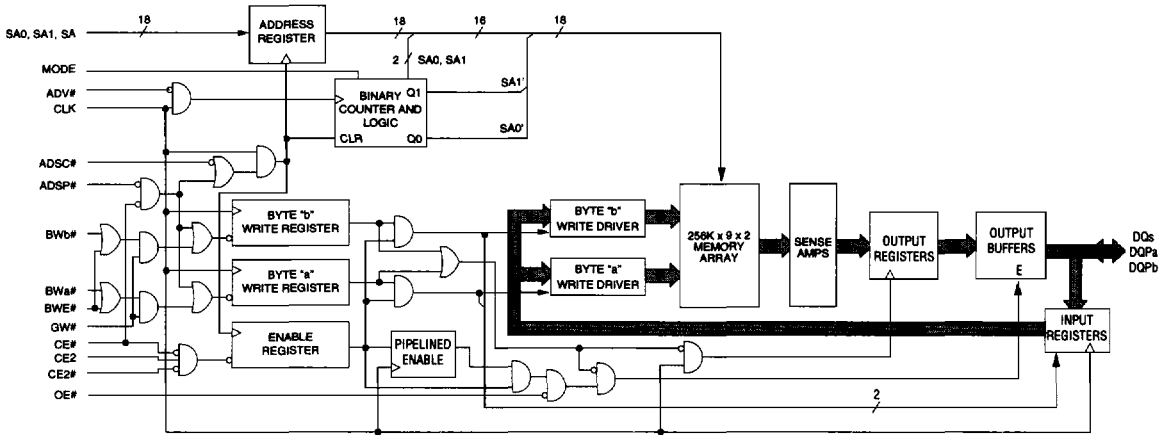
	1	2	3	4	5	6	7
A	V _{DDQ}	SA	SA	ADSP#	SA	SA	V _{DDQ}
B	NC	CE2	SA	ADSC#	SA	CE2#	NC
C	NC	SA	SA	V _{DD}	SA	SA	NC
D	DQb	NC	V _{SS}	NC	V _{SS}	DQP _a	NC
E	NC	DQb	V _{SS}	CE#	V _{SS}	NC	DQ _a
F	V _{DDQ}	NC	V _{SS}	OE#	V _{SS}	DQ _a	V _{DDQ}
G	NC	DQb	BWb#	ADV#	V _{SS}	NC	DQ _a
H	DQb	NC	V _{SS}	GW#	V _{SS}	DQ _a	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQb	V _{SS}	CLK	V _{SS}	NC	DQ _a
L	DQb	NC	V _{SS}	NC	BW _a #	DQ _a	NC
M	V _{DDQ}	DQb	V _{SS}	BWE#	V _{SS}	NC	V _{DDQ}
N	DQb	NC	V _{SS}	SA1	V _{SS}	DQ _a	NC
P	NC	DQP _b	V _{SS}	SA0	V _{SS}	NC	DQ _a
R	NC	SA	MODE	V _{DD}	V _{DD}	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	V _{DDQ}	DNU	DNU	DNU	DNU	NC	V _{DDQ}


SYNCBURST SRAM
**x32/x36 BGA BUMP LAYOUT
(Top View)**

	1	2	3	4	5	6	7
A	V _{DDQ}	SA	SA	ADSP#	SA	SA	V _{DDQ}
B	NC	CE2	SA	ADSC#	SA	CE2#	NC
C	NC	SA	SA	V _{DD}	SA	SA	NC
D	DQ _c	NC/DQP _c *	V _{SS}	NC	V _{SS}	NC/DQP _b *	DQ _b
E	DQ _c	DQ _c	V _{SS}	CE#	V _{SS}	DQ _b	DQ _b
F	V _{DDQ}	DQ _c	V _{SS}	OE#	V _{SS}	DQ _b	V _{DDQ}
G	DQ _c	DQ _c	BW _c #	ADV#	BW _b #	DQ _b	DQ _b
H	DQ _c	DQ _c	V _{SS}	GW#	V _{SS}	DQ _b	DQ _b
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQ _d	DQ _d	V _{SS}	CLK	V _{SS}	DQ _a	DQ _a
L	DQ _d	DQ _d	BW _d #	NC	BW _a #	DQ _a	DQ _a
M	V _{DDQ}	DQ _d	V _{SS}	BWE#	V _{SS}	DQ _a	V _{DDQ}
N	DQ _d	DQ _d	V _{SS}	SA1	V _{SS}	DQ _a	DQ _a
P	DQ _d	NC/DQP _d *	V _{SS}	SA0	V _{SS}	NC/DQP _a *	DQ _a
R	NC	SA	MODE	V _{DD}	V _{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	V _{DDQ}	DNU	DNU	DNU	DNU	NC	V _{DDQ}

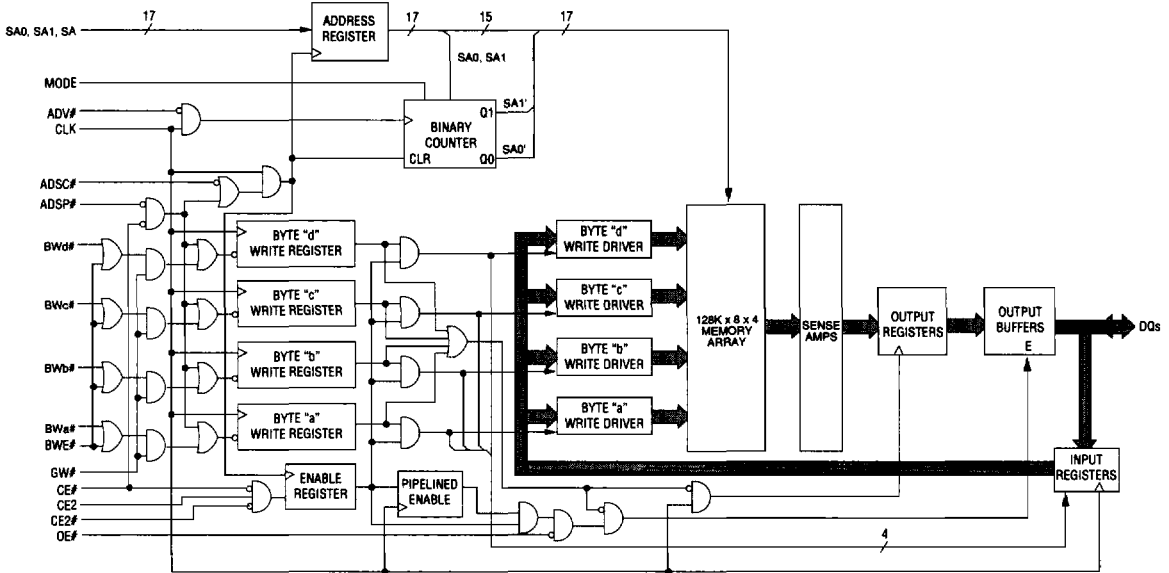
* No Connect (NC) is used in the x32 version. Parity (DQP_x) is used in the x36 version.

**FUNCTIONAL BLOCK DIAGRAM
256K x 18**



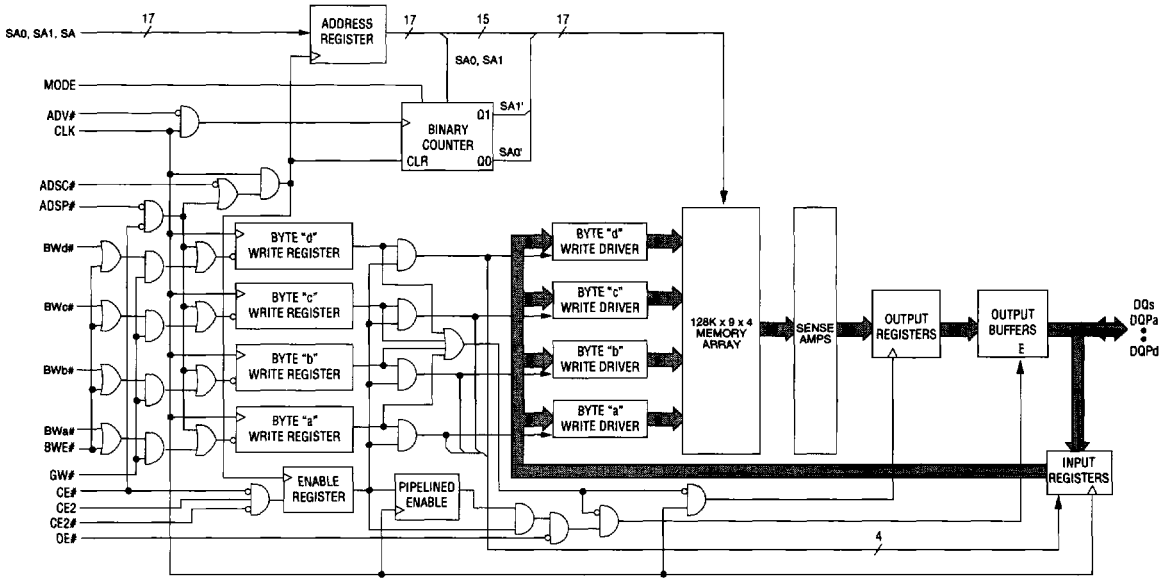
SYNCBURST SRAM

**FUNCTIONAL BLOCK DIAGRAM
128K x 32**



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

FUNCTIONAL BLOCK DIAGRAM
128K x 36



SYNCBURST SRAM

NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
37 36 32-35, 44-50, 80-82, 99, 100	37 36 32-35, 44-50, 81, 82, 99, 100	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93 94 - -	93 94 95 96	BWa# Bwb# Bwc# Bwd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQP _a ; Bwb# controls DQb pins and DQP _b . For the x32 and x36 versions, BWa# controls DQa pins and DQP _a ; Bwb# controls DQb pins and DQP _b ; Bwc# controls DQc pins and DQP _c ; Bwd# controls DQd pins and DQP _d . Parity is only available on the x18 and x36 versions.
87	87	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
88	88	GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
89	89	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	98	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
92	92	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
97	97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
86	86	OE#	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
83	83	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

SYNCBURST SRAM

PIN DESCRIPTIONS (continued)

TQFP (x18)	TQFP (x32/x36)	SYMBOL	TYPE	DESCRIPTION
84	84	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
85	85	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
31	31	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.
64	64	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
(a) 58, 59, 62, 63, 68, 69, 72, 73 (b) 8, 9, 12, 13, 18, 19, 22, 23	(a) 52, 53, 56-59, 62, 63 (b) 68, 69 72-75, 78, 79 (c) 2, 3, 6-9, 12, 13 (d) 18, 19, 22-25, 28, 29	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
74 24 - -	51 80 1 30	NC/DQP a NC/DQP b NC/DQP c NC/DQP d	NC/ I/O	No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" Parity is DQP _a ; Byte "b" Parity is DQP _b . On the x36 version, Byte "a" Parity is DQP _a ; Byte "b" Parity is DQP _b ; Byte "c" Parity is DQP _c ; Byte "d" Parity is DQP _d .
14, 15, 41, 65, 91	14, 15, 41, 65, 91	V _{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
4, 11, 20, 27, 54, 61, 70, 77	4, 11, 20, 27, 54, 61, 70, 77	V _{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	5, 10, 17, 21, 26, 40, 55, 60, 67, 71, 76, 90	V _{SS}	Supply	Ground: GND.
38, 39, 42, 43	38, 39, 42, 43	DNU	-	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1-3, 6, 7, 16, 25, 28-30, 51-53, 56, 57, 66, 75, 78, 79, 95, 96	16, 66	NC	-	No Connect: These signals are not internally connected. These signals may be connected to ground to improve package heat dissipation.

PIN DESCRIPTIONS

SYNCHRONOUS BURST SRAM

BGA (x18)	BGA (x32/x36)	SYMBOL	TYPE	DESCRIPTION
4P 4N 2A, 3A, 5A, 6A, 3B, 5B, 2C, 3C, 5C, 6C, 2R, 6R, 2T, 3T, 5T, 6T	4P 4N 2A, 2C, 2R, 3A, 3B, 3C, 3T, 4T, 5A, 5B, 5C, 5T, 6A, 6C, 6R	SA0 SA1 SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
5L 3G - -	5L 5G 3G 3L	BWa# BWb# BWc# BWd#	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. For the x18 version, BWa# controls DQa pins and DQP _a ; BWb# controls DQb pins and DQP _b . For the x32 and x36 versions, BWa# controls DQa pins and DQP _a ; BWb# controls DQb pins and DQP _b ; BWc# controls DQc pins and DQP _c ; BWd# controls DQd pins and DQP _d . Parity is only available on the x18 and x36 versions.
4M	4M	BWE#	Input	Byte Write Enable: This active LOW input permits BYTE WRITE operations and must meet the setup and hold times around the rising edge of CLK.
4H	4H	GW#	Input	Global Write: This active LOW input allows a full 18-, 32- or 36-bit WRITE to occur independent of the BWE# and BWx# lines and must meet the setup and hold times around the rising edge of CLK.
4K	4K	CLK	Input	Clock: This signal registers the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
4E	4E	CE#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions the internal use of ADSP#. CE# is sampled only when a new external address is loaded.
6B	6B	CE2#	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and is sampled only when a new external address is loaded.
7T	7T	ZZ	Input	Snooze Enable: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored.
2B	2B	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device and is sampled only when a new external address is loaded.
4F	4F	OE#	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers.
4G	4G	ADV#	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). To ensure use of correct address during a WRITE cycle, ADV# must be HIGH at the rising edge of the first clock after an ADSP# cycle is initiated.

MICRON256K x 18, 128K x 32/36
3.3V I/O, PIPELINED, SCD SYNCBURST SRAM**PIN DESCRIPTIONS (continued)**

BGA (x18)	BGA (x32/x36)	SYMBOL	TYPE	DESCRIPTION
4A	4A	ADSP#	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and ADSC#, but dependent upon CE#, CE2 and CE2#. ADSP# is ignored if CE# is HIGH. Power-down state is entered if CE2 is LOW or CE2# is HIGH.
4B	4B	ADSC#	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ or WRITE is performed using the new address if CE# is LOW. ADSC# is also used to place the chip into power-down state when CE# is HIGH.
3R	3R	MODE	Input	Mode: This input selects the burst sequence. A LOW on this pin selects "linear burst." NC or HIGH on this pin selects "interleaved burst." Do not alter input state while device is operating.
(a) 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M	(a) 6K, 6L, 6M, 6N, 7K, 7L, 7N, 7P (b) 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N	DQa DQb DQc DQd	Input/ Output	SRAM Data I/Os: For the x18 version, Byte "a" is DQa pins; Byte "b" is DQb pins. For the x32 and x36 versions, Byte "a" is DQa pins; Byte "b" is DQb pins; Byte "c" is DQc pins; Byte "d" is DQd pins. Input data must meet setup and hold times around the rising edge of CLK.
6D 2P - -	6P 6D 2D 2P	NC/DQP _a NC/DQP _b NC/DQP _c NC/DQP _d	NC/ I/O	No Connect/Parity Data I/Os: On the x32 version, these pins are No Connect (NC). On the x18 version, Byte "a" Parity is DQP _a ; Byte "b" Parity is DQP _b . On the x36 version, Byte "a" Parity is DQP _a ; Byte "b" Parity is DQP _b ; Byte "c" Parity is DQP _c ; Byte "d" Parity is DQP _d .
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	V _{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	V _{DDQ}	Supply	Isolated Output Buffer Supply: See DC Electrical Characteristics and Operating Conditions for range.
3D, 3E, 3F, 3H, 3K, 3L, 3M, 3N, 3P, 5D, 5E, 5F, 5G, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V _{SS}	Supply	Ground: GND.

SYNCBURST SRAM

PIN DESCRIPTIONS (continued)

BGA (x18)	BGA (x32/x36)	SYMBOL	TYPE	DESCRIPTION
2U, 3U, 4U, 5U	2U, 3U, 4U, 5U	DNU	–	Do Not Use: These signals may either be unconnected or wired to GND to improve package heat dissipation.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2D, 2F, 2H, 2L, 2N, 3J, 4D, 4L, 4T, 5J, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2T, 3J, 4D, 4L, 5J, 6T, 6U, 7B, 7C, 7R	NC	–	No Connect: These signals are not internally connected. However, to improve package heat dissipation, these signals may be connected to ground.

SYNCBURST SRAM

INTERLEAVED BURST ADDRESS TABLE (MODE = NC OR HIGH)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE (MODE = LOW)

First Address (External)	Second Address (Internal)	Third Address (Internal)	Fourth Address (Internal)
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x18)

Function	GW#	BWE#	BWa#	BWb#
READ	H	H	X	X
READ	H	L	H	H
WRITE Byte "a"	H	L	L	H
WRITE Byte "b"	H	L	H	L
WRITE All Bytes	H	L	L	L
WRITE All Bytes	L	X	X	X

PARTIAL TRUTH TABLE FOR WRITE COMMANDS (x32/x36)

Function	GW#	BWE#	BWa#	BWb#	BWc#	BWd#
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE Byte "a"	H	L	L	H	H	H
WRITE All Bytes	H	L	L	L	L	L
WRITE All Bytes	L	X	X	X	X	X

NOTE: Using BWE# and BWa# through BWd#, any one or more bytes may be written.

TRUTH TABLE

OPERATION	ADDRESS USED	CE#	CE2#	CE2	ZZ	ADSP#	ADSC#	ADV#	WRITE#	OE#	CLK	DQ
Deselected Cycle, Power-Down	None	H	X	X	L	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	X	L	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	H	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	X	L	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-Down	None	L	H	X	L	H	L	X	X	X	L-H	High-Z
SNOOZE MODE, Power-Down	None	X	X	X	H	X	X	X	X	X	X	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	L	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	L	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	L	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	L	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	L	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	L	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	L	X	H	H	L	X	L-H	D

- NOTE:**
1. X means "Don't Care." # means active LOW. H means logic HIGH. L means logic LOW.
 2. For WRITE#, L means any one or more byte write enable signals (BWa#, BWb#, BWc# or Bwd#) and BWE# are LOW or GW# is LOW. WRITE# = H for all BWx#, BWE#, GW# HIGH.
 3. BWa# enables WRITES to DQa pins, DQP_a. BWb# enables WRITES to DQb pins, DQP_b. BWc# enables WRITES to DQc pins, DQP_c. Bwd# enables WRITES to DQd pins, DQP_d. DQP_a and DQP_b are only available on the x18 and x36 versions. DQP_c and DQP_d are only available on the x36 version.
 4. All inputs except OE# and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
 5. Wait states are inserted by suspending burst.
 6. For a WRITE operation following a READ operation, OE# must be HIGH before the input data setup time and held HIGH throughout the input data hold time.
 7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
 8. ADSP# LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and BWE# LOW or GW# LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V _{DD} Supply Relative to V _{SS}	-0.5V to +4.6V
Voltage on V _{DDQ} Supply Relative to V _{SS}	-0.5V to +4.6V
V _{IN}	-0.5V to V _{DD} + 0.5V
Storage Temperature (plastic)	-55°C to +150°C
Storage Temperature (BGA)	-55°C to +125°C
Junction Temperature**	+150°C
Short Circuit Output Current	100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{DD}, V_{DDQ} = +3.3V +0.3V/-0.165V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.0	V _{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V _{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{DD}	I _{LI}	-1	1	μA	3
Output Leakage Current	Output(s) disabled, 0V ≤ V _{IN} ≤ V _{DD}	I _{LO}	-1	1	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1, 4
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1, 4
Supply Voltage		V _{DD}	3.135	3.6	V	1
Isolated Output Buffer Supply		V _{DDQ}	3.135	3.6	V	1, 5

TQFP THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TQFP TYP	UNITS	NOTES
Thermal Resistance (Junction to Ambient)	Still air, soldered on 4.25 x 1.125 inch,	θ _{JA}	28	°C/W	6
Thermal Resistance (Junction to Case)	4-layer printed circuit board	θ _{JC}	4	°C/W	6

BGA THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch,	θ _{JA}	25	°C/W	6
Junction to Case (Top)	4-layer printed circuit board	θ _{JC}	10	°C/W	6
Junction to Bumps (Bottom)		θ _{JB}	12	°C/W	6

- NOTE:**
- All voltages referenced to V_{SS} (GND).
 - Overshoot: V_{IH} ≤ +4.6V for t ≤ 1KC/2 for I ≤ 20mA
Undershoot: V_{IL} -0.7V for t ≤ 1KC/2 for I ≤ 20mA
Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V for t ≤ 200ms
 - MODE pin has an internal pull-up, and input leakage = ±100μA.
 - The load used for V_{OH}, V_{OL} testing is shown in Figure 2. AC load current is higher than the shown DC values. AC I/O curves are available upon request.
 - V_{DDQ} should never exceed V_{DD}. V_{DD} and V_{DDQ} can be connected together.
 - This parameter is sampled.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{DD}, V_{DDQ} = +3.3V ± 0.3V/-0.165V unless otherwise noted)

SYNCBURST SRAM

DESCRIPTION	CONDITIONS	SYM	TYP	MAX					UNITS	NOTES
				-6	-6.6	-7.5	8.5	-11		
Power Supply Current: Operating	Device selected; All inputs ≤ V _{IL} or ≥ V _{IH} ; Cycle time ≥ 1KC MIN; V _{DD} = MAX; Outputs open	I _{DD}	TBD	450	400	325	275	225	mA	1, 2, 3
Power Supply Current: Idle	Device selected; V _{DD} = MAX; ADSC#, ADSP#, GW#, BWx#, ADV# ≥ V _{IH} ; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ 1KC MIN	I _{DD1}	TBD	110	100	90	90	80	mA	1, 2, 3
CMOS Standby	Device deselected; V _{DD} = MAX; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; All inputs static; CLK frequency = 0	I _{SB2}	TBD	10	10	10	10	10	mA	2, 3
TTL Standby	Device deselected; V _{DD} = MAX; All inputs ≤ V _{IL} or ≥ V _{IH} ; All inputs static; CLK frequency = 0	I _{SB3}	TBD	25	25	25	25	25	mA	2, 3
Clock Running	Device deselected; V _{DD} = MAX; All inputs ≤ V _{SS} + 0.2 or ≥ V _{DD} - 0.2; Cycle time ≥ 1KC MIN	I _{SB4}	TBD	110	100	90	90	80	mA	2, 3

TQFP CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Control Input Capacitance	T _A = 25°C; f = 1 MHz V _{DD} = 3.3V	C _I	3	4	pF	4
Input/Output Capacitance (DQ)		C _O	4	5	pF	4
Address Capacitance		C _A	3	3.5	pF	4
Clock Capacitance		C _{CK}	2.5	3	pF	4

BGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T _A = 25°C; f = 1 MHz	C _I	4	5	pF	4
Input/Output Capacitance (DQ)		C _O	6	7	pF	4
Clock Capacitance		C _{CK}	5	6	pF	4

- NOTE:**
1. I_{DD} is specified with no output current and increases with faster cycle times. I_{DDQ} increases with faster cycle time and greater output loading.
 2. "Device deselected" means device is in power-down mode as defined in the truth table. "Device selected" means device is active (not in power-down mode).
 3. Typical values are measured at 3.3V, 25°C and 11ns cycle time.
 4. This parameter is sampled.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{DD}, V_{DDQ} = +3.3V ±0.3V/-0.165V unless otherwise noted)

DESCRIPTION	SYM	-6		-6.6		-7.5		-8.5		-11		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock													
Clock cycle time	¹ KC	6.0		6.6		7.5		8.5		11		ns	
Clock frequency	¹ KF		166		150		133		117		90	MHz	
Clock HIGH time	¹ KH	1.7		1.8		1.9		2.5		3.8		ns	
Clock LOW time	¹ KL	1.7		1.8		1.9		2.5		3.8		ns	
Output Times													
Clock to output valid	¹ KQ		3.5		3.8		4.2		4.5		6.0	ns	
Clock to output invalid	¹ KQX	1.5		1.5		1.5		1.5		2.0		ns	2
Clock to output in Low-Z	¹ KQLZ	1.5		1.5		1.5		1.5		2.0		ns	2, 3, 4, 5
Clock to output in High-Z	¹ KQHZ		3.5		3.8		4.2		4.5		5.0	ns	2, 3, 4, 5
OE# to output valid	¹ OEQ		3.5		3.8		4.2		4.5		5.0	ns	6
OE# to output in Low-Z	¹ OELZ	0		0		0		0		0		ns	2, 3, 4, 5
OE# to output in High-Z	¹ OEHZ		3.5		3.8		4.2		4.5		5.0	ns	2, 3, 4, 5
Setup Times													
Address	¹ AS	1.7		1.7		2.0		2.2		2.5		ns	7, 8
Address status (ADSC#, ADSP#)	¹ ADSS	1.7		1.7		2.0		2.2		2.5		ns	7, 8
Address advance (ADV#)	¹ AAS	1.7		1.7		2.0		2.2		2.5		ns	7, 8
Write signals (BWA#-BWD#, BWE#, GW#)	¹ WS	1.7		1.7		2.0		2.2		2.5		ns	7, 8
Data-in	¹ DS	1.7		1.7		2.0		2.2		2.5		ns	7, 8
Chip enables (CE#, CE2#, CE2)	¹ CES	1.7		1.7		2.0		2.2		2.5		ns	7, 8
Hold Times													
Address	¹ AH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Address status (ADSC#, ADSP#)	¹ ADSH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Address advance (ADV#)	¹ AAH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Write signals (BWA#-BWD#, BWE#, GW#)	¹ WH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Data-in	¹ DH	0.5		0.5		0.5		0.5		0.5		ns	7, 8
Chip enables (CE#, CE2#, CE2)	¹ CEH	0.5		0.5		0.5		0.5		0.5		ns	7, 8

- NOTE:**
1. Test conditions as specified with the output loading as shown in Figure 1 unless otherwise noted.
 2. This parameter is measured with output load as shown in Figure 2.
 3. This parameter is sampled.
 4. Transition is measured ±500mV from steady state voltage.
 5. Refer to Technical Note TN-58-09, "Synchronous SRAM Bus Contention Design Considerations," for a more thorough discussion on these parameters.
 6. OE# is a "Don't Care" when a byte write enable is sampled LOW.
 7. A WRITE cycle is defined by at least one byte write enable LOW and ADSP# HIGH for the required setup and hold times. A READ cycle is defined by all byte write enables HIGH and ADSC# or ADV# LOW or ADSP# LOW for the required setup and hold times.
 8. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either ADSP# or ADSC# is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when the chip is enabled. Chip enable must be valid at each rising edge of CLK when either ADSP# or ADSC# is LOW to remain enabled.

AC TEST CONDITIONS

Input pulse levels	$V_{IH} = (V_{DD}/2.2) + 1.5V$
.....	$V_{IL} = (V_{DD}/2.2) - 1.5V$
Input rise and fall times	1ns
Input timing reference levels	$V_{DD}/2.2$
Output reference levels	$V_{DD}/2.2$
Output load	See Figures 1 and 2

LOAD DERATING CURVES

Micron 256K x 18, 128K x 32 and 128K x 36 SyncBurst SRAM timing is dependent upon the capacitive loading on the outputs.

Consult the factory for copies of I/O current versus voltage curves.

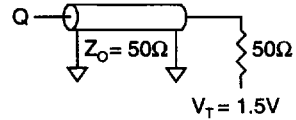


Figure 1
OUTPUT LOAD EQUIVALENT

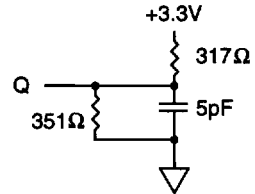


Figure 2
OUTPUT LOAD EQUIVALENT

SNOOZE MODE

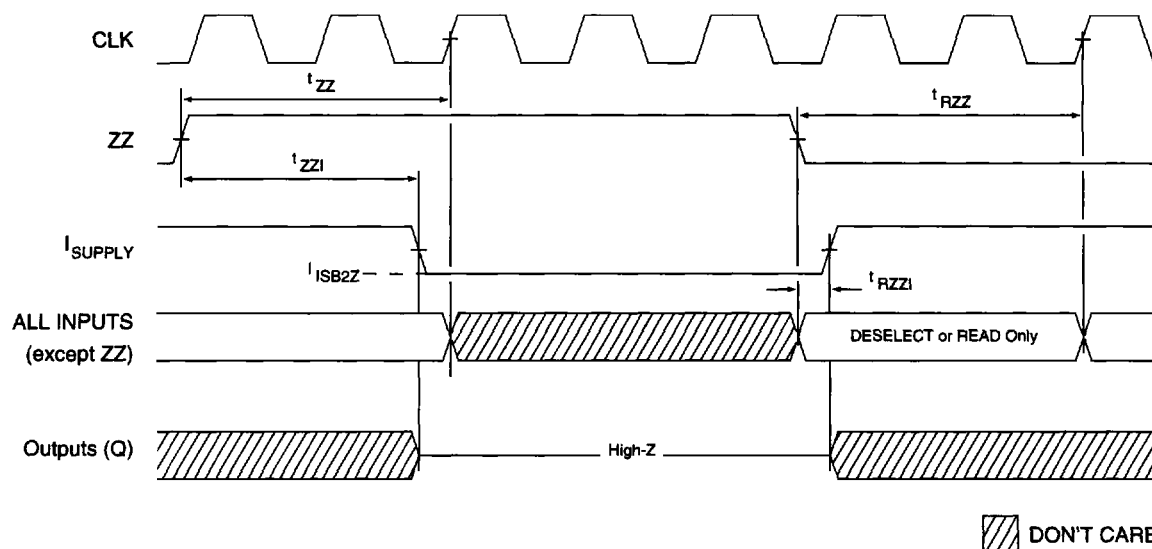
SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z} . The duration of SNOOZE MODE is dictated by the length of time the ZZ pin is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored.

The ZZ pin (pin 64) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the setup time t_{ZZ} is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed.

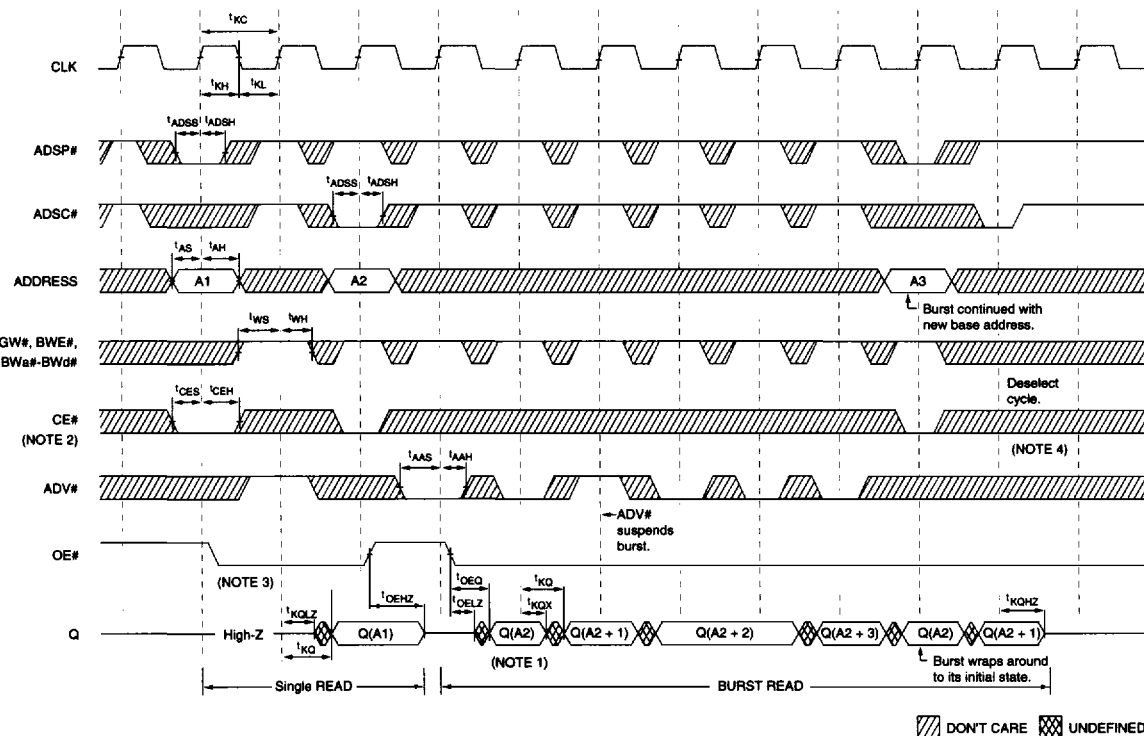
SNOOZE MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	$ZZ \geq V_{IH}$	I_{SB2Z}		10	mA	
ZZ active to input ignored		t_{ZZ}		$2(t_{KC})$	ns	1
ZZ inactive to input sampled		t_{RZZ}	$2(t_{KC})$		ns	1
ZZ active to snooze current		t_{ZZI}		$2(t_{KC})$	ns	1
ZZ inactive to exit snooze current		t_{RZZI}	0		ns	1

NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM

READ TIMING



▨ DON'T CARE ▩ UNDEFINED

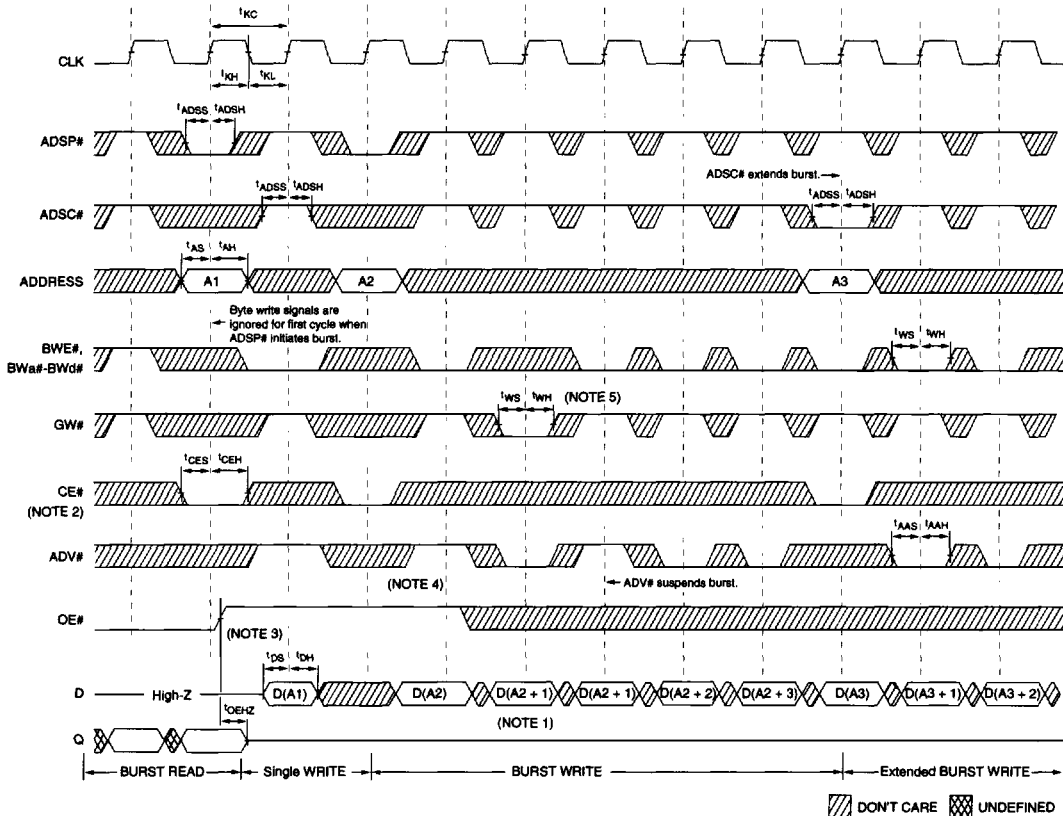
READ TIMING PARAMETERS

SYM	-6		-6.6		-7.5		-8.5		-11		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{KC}	6.0	6.6		7.5	8.5	11					ns
t _{KF}		166	150	133	117	90					MHz
t _{KH}	1.7	1.8	1.9	2.5	3.8						ns
t _{KL}	1.7	1.8	1.9	2.5	3.8						ns
t _{KQ}		3.5	3.8	4.2	4.5	6.0					ns
t _{KQX}	1.5	1.5	1.5	1.5	2.0						ns
t _{KQZ}	1.5	1.5	1.5	1.5	2.0						ns
t _{KQHZ}		3.5	3.8	4.2	4.5	5.0					ns
t _{OEQ}		3.5	3.8	4.2	4.5	5.0					ns
t _{OELZ}	0	0	0	0	0	0					ns
t _{OEZH}		3.5	3.8	4.2	4.5	5.0					ns

SYM	-6		-6.6		-7.5		-8.5		-11		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{AS}	1.7	1.7	2.0	2.2	2.5						ns
t _{ADSS}	1.7	1.7	2.0	2.2	2.5						ns
t _{ADSH}	1.7	1.7	2.0	2.2	2.5						ns
t _{WS}	1.7	1.7	2.0	2.2	2.5						ns
t _{CES}	1.7	1.7	2.0	2.2	2.5						ns
t _{AH}	0.5	0.5	0.5	0.5	0.5						ns
t _{ADSH}	0.5	0.5	0.5	0.5	0.5						ns
t _{AAH}	0.5	0.5	0.5	0.5	0.5						ns
t _{WH}	0.5	0.5	0.5	0.5	0.5						ns
t _{CEH}	0.5	0.5	0.5	0.5	0.5						ns

- NOTE:
- Q(A2) refers to output from address A2. Q(A2 + 1) refers to output from the next internal burst address following A2.
 - CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
 - Timing is shown assuming that the device was not enabled before entering into this sequence. OE# does not cause Q to be driven until after the following clock rising edge.
 - Outputs are disabled within one clock cycle after deselect.

WRITE TIMING



WRITE TIMING PARAMETERS

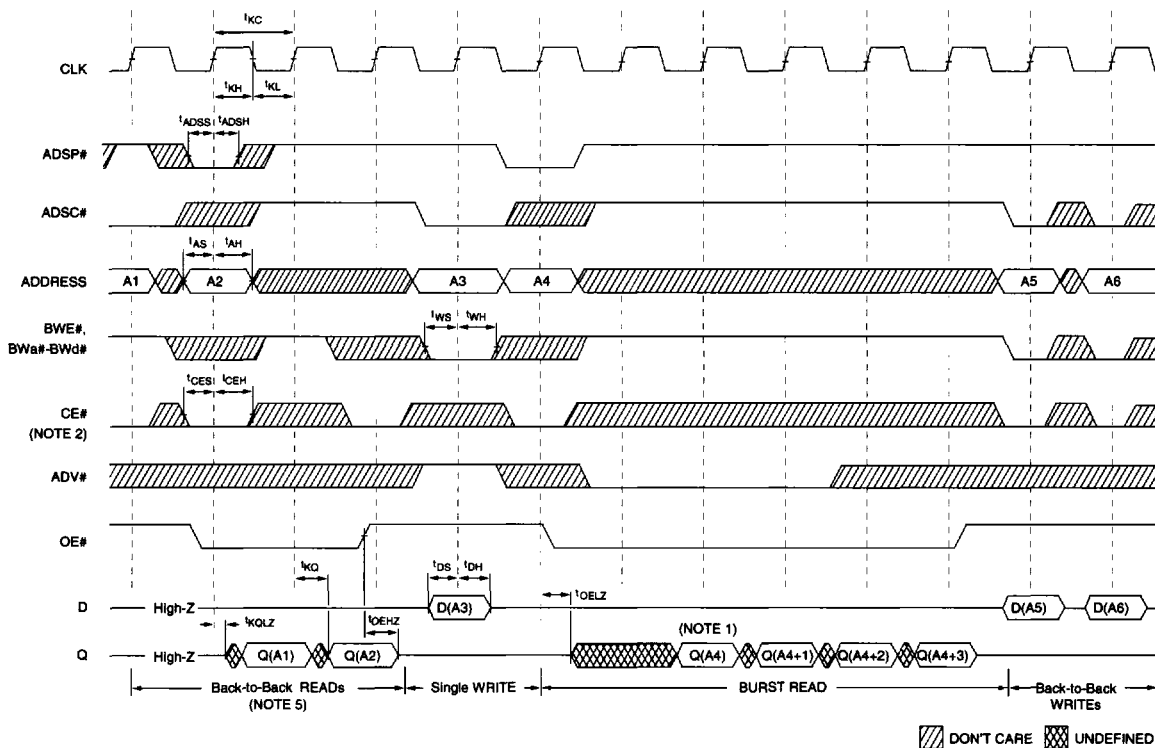
SYM	-6		-6.6		-7.5		-8.5		-11		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{KC}	6.0		6.6		7.5		8.5		11		ns
t _{KF}		166		150		133		117		90	MHz
t _{KH}	1.7		1.8		1.9		2.5		3.8		ns
t _{KL}	1.7		1.8		1.9		2.5		3.8		ns
t _{OEZH}		3.5		3.8		4.2		4.5		5.0	ns
t _{AS}	1.7		1.7		2.0		2.2		2.5		ns
t _{ADSS}	1.7		1.7		2.0		2.2		2.5		ns
t _{AAS}	1.7		1.7		2.0		2.2		2.5		ns
t _{WS}	1.7		1.7		2.0		2.2		2.5		ns

SYM	-6		-6.6		-7.5		-8.5		-11		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{DS}	1.7		1.7		2.0		2.2		2.5		ns
t _{CES}	1.7		1.7		2.0		2.2		2.5		ns
t _{AH}	0.5		0.5		0.5		0.5		0.5		ns
t _{ADSH}	0.5		0.5		0.5		0.5		0.5		ns
t _{AAH}	0.5		0.5		0.5		0.5		0.5		ns
t _{WH}	0.5		0.5		0.5		0.5		0.5		ns
t _{DH}	0.5		0.5		0.5		0.5		0.5		ns
t _{CEH}	0.5		0.5		0.5		0.5		0.5		ns

- NOTE:**
1. D(A2) refers to input for address A2. D(A2 + 1) refers to input for the next internal burst address following A2.
 2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
 3. OE# must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
 4. ADV# must be HIGH to permit a WRITE to the loaded address.
 5. Full-width WRITE can be initiated by GW# LOW; or GW# HIGH and BWE#, BWA# and BWb# LOW for x18 device; or GW# HIGH and BWE#, BWA#-BWD# LOW for x32 and x36 devices.

READ/WRITE TIMING

SYNCBURST SRAM



READ/WRITE TIMING PARAMETERS

SYM	-6		-6.6		-7.5		-8.5		-11		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{KC}	6.0		6.6		7.5		8.5		11		ns
t _{KF}		166		150		133		117		90	MHz
t _{KH}	1.7		1.8		1.9		2.5		3.8		ns
t _{KL}	1.7		1.8		1.9		2.5		3.8		ns
t _{KQ}		3.5		3.8		4.2		4.5		6.0	ns
t _{QLZ}	1.5		1.5		1.5		1.5		2.0		ns
t _{OELZ}	0		0		0		0		0		ns
t _{OEHZ}		3.5		3.8		4.2		4.5		5.0	ns
t _{AS}	1.7		1.7		2.0		2.2		2.5		ns

SYM	-6		-6.6		-7.5		-8.5		-11		UNITS
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{ADSS}	1.7		1.7		2.0		2.2		2.5		ns
t _{WS}	1.7		1.7		2.0		2.2		2.5		ns
t _{DS}	1.7		1.7		2.0		2.2		2.5		ns
t _{CES}	1.7		1.7		2.0		2.2		2.5		ns
t _{AH}	0.5		0.5		0.5		0.5		0.5		ns
t _{ADSH}	0.5		0.5		0.5		0.5		0.5		ns
t _{WH}	0.5		0.5		0.5		0.5		0.5		ns
t _{DH}	0.5		0.5		0.5		0.5		0.5		ns
t _{CEH}	0.5		0.5		0.5		0.5		0.5		ns

- NOTE:**
1. Q(A4) refers to output from address A4. Q(A4 + 1) refers to output from the next internal burst address following A4.
 2. CE2# and CE2 have timing identical to CE#. On this diagram, when CE# is LOW, CE2# is LOW and CE2 is HIGH. When CE# is HIGH, CE2# is HIGH and CE2 is LOW.
 3. The data bus (Q) remains in High-Z following a WRITE cycle unless an ADSP#, ADSC# or ADV# cycle is performed.
 4. GW# is HIGH.
 5. Back-to-back READs may be controlled by either ADSP# or ADSC#.